

OV3630 Color CMOS QXGA (3.2 MPixel) CAMERACHIP™ with OmniPixel® Technology

General Description

The OV3630 (color) CAMERACHIP™ is a high performance 3.2 mega-pixel CMOS image sensors for digital still image and video/still camera products.

The device incorporates a 2048 x 1536 (QXGA) image array and an on-chip 10-bit A/D converter capable of operating at up to 15 frames per second (fps) in full resolution mode. Proprietary sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), eliminate smearing, and drastically reduce blooming. The control registers allow for flexible control of timing, polarity, and CameraChip operation, which, in turn, allows the engineer a great deal of freedom in product design.



Note: The OV3630 uses a lead-free package.

Features

- Optical black level calibration
- Line optical black level output capability
- Video or snapshot operations
- Programmable/Auto Exposure and Gain Control
- Programmable/Auto White Balance Control
- Horizontal and vertical sub-sampling (4:2 and 4:2)
- High frame rate output for auto focus mode
- Programmable image windowing
- Zooming and panning functions
- Variable frame rate control
- On-chip R/G/B Channel and Luminance Average Counter
- Internal/External frame synchronization
- SCCB slave interface
- Power-on reset and power-down modes

Ordering Information

Product	Package
OV03630-VL5A (Color, Lead-free)	36-pin CSP2

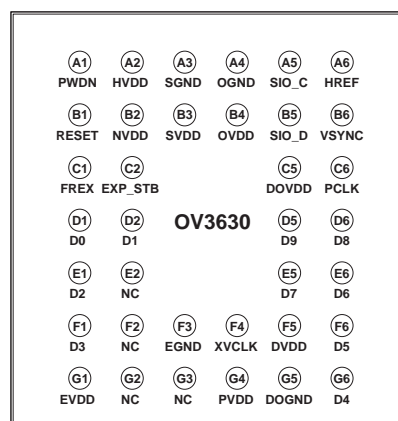
Applications

- Cellular phones
- Digital still cameras
- PC camera/dual mode
- Video conference equipment
- Machine vision
- Security cameras
- Biometrics

Key Specifications

Array Size	QXGA	2048 x 1536
	XGA	1024 x 768
	HF	1024 x 192
Power Supply	Analog	2.8VDC ± 5%
	Core	1.8VDC ± 5%
	I/O	1.7 ~ 3.3V
Power Requirements	Active	TBD
	Standby	TBD
Electronics Exposure	QXGA	Up to 1567:1
	XGA	Up to 799:1
	HF	Up to 223:1
Output Format		10-bit digital RGB Raw data
Lens Size		1/3"
Chief Ray Angle (CRA)		TBD
Maximum Image Transfer Rate	QXGA	15 fps
	XGA	30 fps
	HF	90 fps
Sensitivity		TBD
S/N Ratio		TBD
Dynamic Range		TBD
Scan Mode		Progressive
Pixel Size		2.2 μm x 2.2 μm
Dark Current		TBD
Fixed Pattern Noise		TBD
Image Area		4.54 mm x 3.41 mm
Package Dimensions		6085μm X 6315μm

Figure 1 OV3630 Pin Diagram (Top View)



Functional Description

Figure 2 shows the functional block diagram of the OV3630 image sensor. The OV3630 includes:

- Image Sensor Array (2064 x 1560 active image array)
- Analog Amplifier
 - Gain Control
- 10-Bit A/D Converter
- Channel Balance
 - Balance Control
- Black Level Compensation
- Timing Generator and Control Logic
 - Frame Exposure Mode Timing
 - Frame Rate Timing
 - Frame Rate Adjust
- SCCB Interface
- Channel Average Calculator
- Digital Video Port

Figure 2 Functional Block Diagram

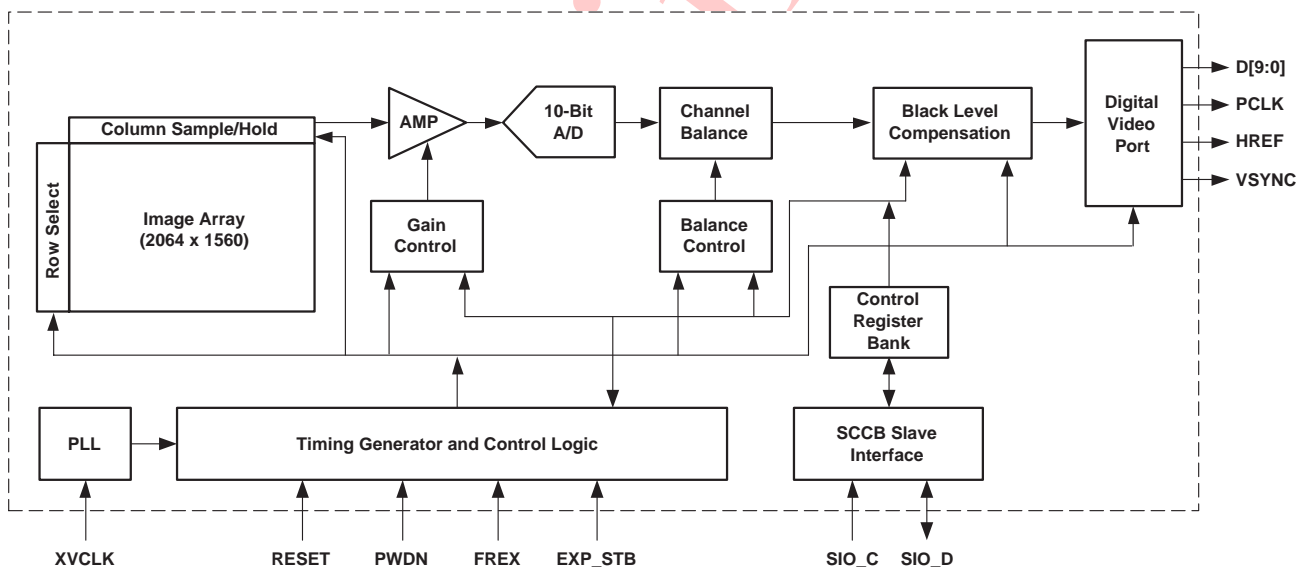
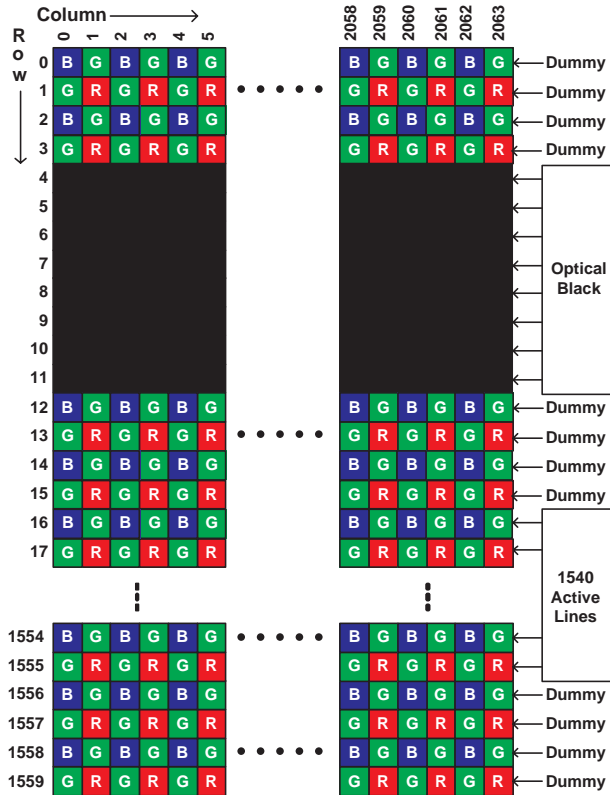


Image Sensor Array

The OV3630 sensor is a 1/3-inch CMOS imaging device. The sensor contains 3,219,840 pixels. Figure 3 shows the color filter layout.

Figure 3 Sensor Array Region Color Filter Layout



The color filters are in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 3,219,840 pixels, 3,170,352 are active. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

Analog Amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

Gain Control

The amplifier gain can either be programmed by the user or controlled by the internal automatic gain control circuit (AGC).

10-Bit A/D Converter

The signal is then digitized by the on-chip 10-bit ADC. It can operate at 28 MHz and is fully synchronous to the pixel clock. The actual conversion rate is determined by the frame rate.

Channel Balance

The digitized signals are then balanced with a channel balance block. In this block, the Red/Blue channel gain is increased or decreased to match Green channel luminance level.

Balance Control

Channel balance can be done manually by the user or by the internal automatic white balance (AWB) controller.

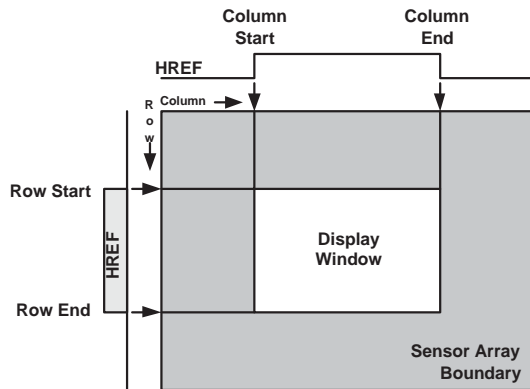
Black Level Compensation

After the pixel data has been channel balanced, black level calibration can be applied before the data is output. The black level calibration block subtracts the average signal level of optical black pixels to compensate for the dark current in the pixel output. Black level calibration can be disabled by the user.

Windowing

The OV3630 allows the user to define window size or region of interest (ROI), as required by the application. Window size setting (in pixels) ranges from 2 x 4 to 2056 x 1542 (QXGA), 2 x 2 to 1028 x 774 (XGA), or 1028 x 192 (HF), and can be anywhere inside the 2056 x 1542 boundary. Note that modifying window size or window position does not alter the frame or pixel rate. The windowing control merely alters the assertion of the HREF signal to be consistent with the programmed horizontal and vertical ROI. The default window size is 2048 x 1536. Refer to Figure 4 and registers HREFST, HREFEND, VSTRT, VEND, COM1, and REG32 for details.

Figure 4 Windowing



Zooming and Panning

The OV3630 provides zooming and panning modes. The user can select this mode under XGA/HF mode timing. Zoom ratio for XGA is 2:1 of QXGA. Zoom ratio for HF is 2:1 of QXGA in the horizontal direction and 8:1 of QXGA in the vertical direction. Register ZOOMSH (0x49) and ZOOMSL[1:0] (0x48) defines the vertical line start point. Register ZOOMW[2:0] (0x34) defines the horizontal start point.

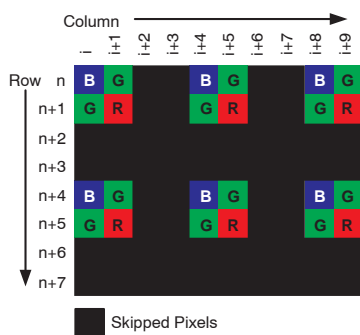
Sub-sampling Mode

The OV3630 supports two sub-sampling modes. Each sub-sampling mode has different resolution and maximum frame rate. These modes are described in the following sections.

XGA Mode

The OV3630 can be programmed to output 1024 x 768 (XGA) sized images for applications where higher resolution image capture is not required. In this mode, both horizontal and vertical pixels will be sub-sampled with an aspect ratio of 4:2 as shown in Figure 5.

Figure 5 XGA Sub-Sampling Mode

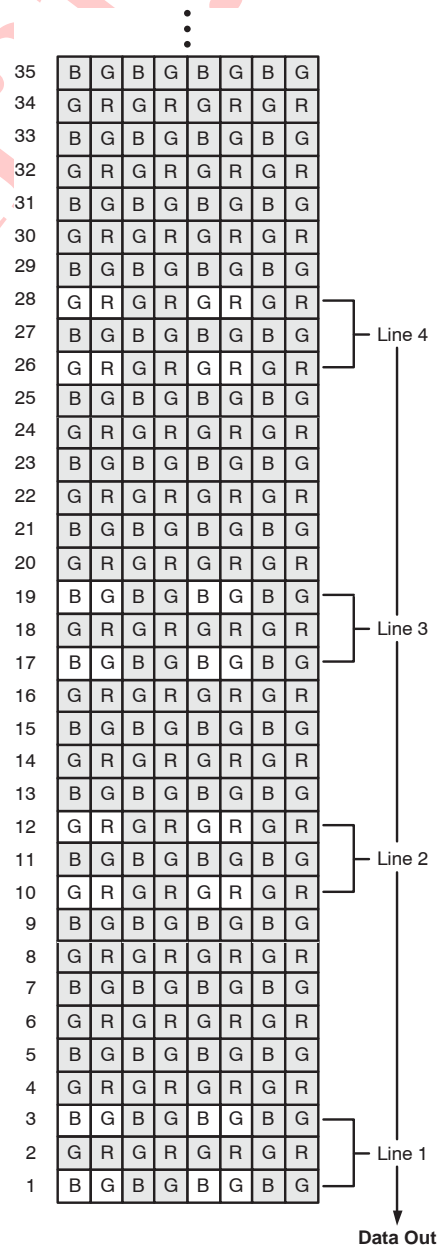


High Frame (HF) Rate Mode

The OV3630 image array sensor can also operate at a High Frame rate (HF) mode. In this mode, the OV3630 averages the B and G pixels (see Figure 6) in lines 1 and 3 to output line 1, G and R pixels of lines 10 and 12 to output line 2, B and G pixels of lines 17 and 19 to output line 3, G and R pixels of lines 26 and 28 to output line 4, etc.

This mode enables up to 90 fps output using a 27.3 MHz system clock so it is effective for high frame rate application.

Figure 6 High Frame Rate Sub-Sampling Mode



Maximum Exposure Line Limits

OV3630 maximum exposure line values are:

- QXGA - 1567 lines
Register setting: $0x61E = \{REG45[5:0] (0x45), AEC[7:0] (0x10), REG04[1:0] (0x04)\}$, meaning $REG45[5:0] (0x45) = 0x01$, $AEC[7:0] (0x10) = 0x87$, $REG04[1:0] (0x04) = 0x03$
- XGA - 799 lines
Register setting: $0x31E = \{REG45[5:0] (0x45), AEC[7:0] (0x10), REG04[1:0] (0x04)\}$, meaning $REG45[5:0] (0x45) = 0x00$, $AEC[7:0] (0x10) = 0xC7$, $REG04[1:0] (0x04) = 0x03$
- HF - 223 lines
Register setting: $0xDE = \{REG45[5:0] (0x45), AEC[7:0] (0x10), REG04[1:0] (0x04)\}$, meaning $REG45[5:0] (0x45) = 0x00$, $AEC[7:0] (0x10) = 0x37$, $REG04[1:0] (0x04) = 0x03$

Timing Generator and Control Logic

In general, the timing generator controls the following:

- [Frame Exposure Mode Timing](#)
- [Frame Rate Timing](#)
- [Frame Rate Adjust](#)

Frame Exposure Mode Timing

The OV3630 supports frame exposure mode. Typically, the frame exposure mode must work with the aid of an external shutter.

The frame exposure pin, [FREX](#) (pin [C1](#)), is the frame exposure mode enable pin and the [EXP_STB](#) pin (pin [C2](#)) serves as the sensor's exposure start trigger. When the external master device asserts the [FREX](#) pin high, the sensor array is quickly pre-charged and stays in reset mode until the [EXP_STB](#) pin goes low (sensor exposure time can be defined as the period between [EXP_STB](#) low and shutter close). After the [FREX](#) pin is pulled low, the video data stream is then clocked to the output port in a line-by-line manner. After completing one frame of data output, the OV3630 will output continuous live video data unless in single frame transfer mode. [Figure 21](#) shows the detailed timing and [Table 11](#) shows the timing specifications for this mode.

Frame Rate Timing

Default frame timing is illustrated in [Figure 14](#), [Figure 15](#) (if [PIDL](#) = 0x30), [Figure 16](#) (if [PIDL](#) ≠ 0x30), [Figure 17](#), [Figure 18](#) (if [PIDL](#) = 0x30), [Figure 19](#) (if [PIDL](#) ≠ 0x30), and [Figure 20](#). Refer to [Table 1](#) for the actual pixel rate at different frame rates.

Table 1 Frame/Pixel Rates in QXGA Mode

Frame Rate (fps)	15	10	5	2.5
PCLK (MHz)	55.2	36.8	18.4	9.2

Frame Rate Adjust

The OV3630 offers three methods for frame rate adjustment:

- Clock prescaler: (see [“CLKRC” on page 20](#))
By changing the system clock divide ratio, the frame rate and pixel rate will change together. This method can be used for dividing the frame/pixel rate by: 1/2, 1/3, 1/4 ... 1/64 of the input clock rate.
- Line adjustment: (see [“REG2A” on page 23](#) and see [“FRARL” on page 23](#))
By adding a dummy pixel timing in each line after active pixel output, the frame rate can be changed while leaving the pixel rate as is.
- Vertical sync adjustment:
By adding dummy line periods to the vertical sync period (see [“ADDVSL” on page 23](#) and see [“ADDVSH” on page 23](#)), the frame rate can be altered while the pixel rate remains the same.

SCCB Interface

The OV3630 provides an on-chip SCCB serial control port that allows access to all internal registers, for complete control and monitoring of OV3630 operation.

Refer to [OmniVision Technologies Serial Camera Control Bus \(SCCB\) Specification](#) for detailed usage of the serial control port.

Slave Operation Mode

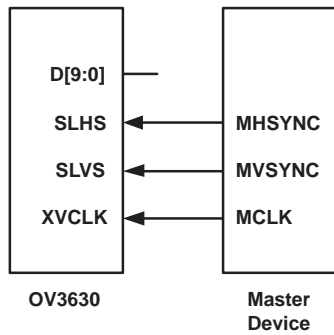
The OV3630 can be programmed to operate in slave mode (default is master mode).

When used as a slave device, [COM7\[3\]](#), [CLKRC\[6\]](#), and [COM2\[2\]](#) register bits should be set to "1" and the OV3630 will use [PWDN](#) and [RESET](#) pins as vertical and horizontal synchronization triggers supplied by a master device. The master device must provide the following signals:

1. System clock MCLK to [XVCLK](#) pin
2. Horizontal sync MHSYNC to [RESET](#) pin
3. Vertical frame sync MVSYSYNC to [PWDN](#) pin

See [Figure 7](#) for slave mode connections and [Figure 8](#) for detailed timing considerations.

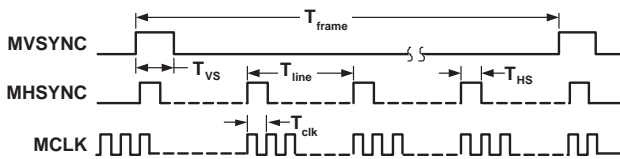
Figure 7 Slave Mode Connection



To initiate hardware power-down, the PWDN pin (pin A1) must be tied to high (+2.8VDC). When this occurs, the OV3630 internal device clock is halted and all internal counters are reset.

Executing a software power-down through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in this mode.

Figure 8 Slave Mode Timing



NOTE:

- 1) $T_{HS} > 6 T_{CLK}$, $T_{VS} > T_{LINE}$
- 2) $T_{LINE} = 2320 \times T_{CLK}$ (QXGA); $T_{LINE} = 1332 \times T_{CLK}$ (XGA);
 $T_{LINE} = 1332 \times T_{CLK}$ (HF)
- 3) $T_{FRAME} = 1568 \times T_{LINE}$ (QXGA); $T_{FRAME} = 800 \times T_{LINE}$ (XGA)
 $T_{FRAME} = 224 \times T_{LINE}$ (HF)

Channel Average Calculator

The OV3630 provides average output level data for the R/G/B channels along with frame-averaged luminance level. Access to the data is provided via the SCCB interface.

Reset

The OV3630 includes a RESET pin (pin B1) that forces a complete hardware reset when it is pulled high (+2.8VDC). The OV3630 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface.

Power Down Mode

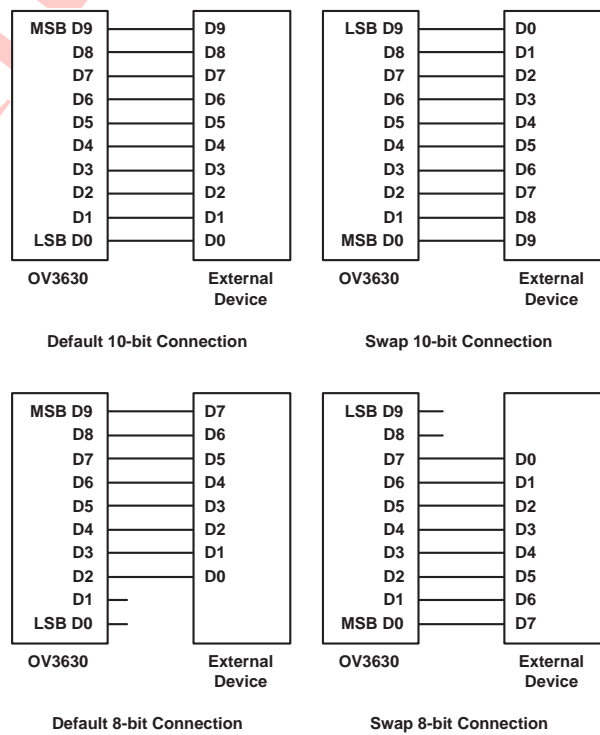
Two methods are available to place the OV3630 into power-down mode: hardware power-down and SCCB software power-down.

Digital Video Port

MSB/LSB Swap

The OV3630 has a 10-bit digital video port. The MSB and LSB can be swapped with the control registers. Figure 9 shows some examples of connections with external devices.

Figure 9 Connection Examples



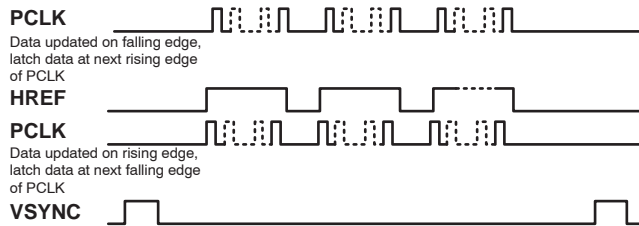
Line/Pixel Timing

The OV3630 digital video port can be programmed to work in either master or slave mode.

In both master and slave modes, pixel data output is synchronous with PCLK (or XVCLK if port is a slave), HREF, and VSYNC. The default PCLK edge for updated data is the negative edge but may be programmed using register COM10[4] for the positive edge. Basic line/pixel output timing and pixel timing specifications are shown in Figure 13 and Table 10.

Also, using register COM10[5] (0x15), PCLK output can be gated by the active video period defined by the HREF signal. See Figure 10 for details.

Figure 10 PCLK Output Only at Valid Pixels



The specifications shown in Table 10 apply for DVDD = +1.8 V, DOVDD = +2.8 V, T_A = 25°C, sensor working at 15 fps in QXGA resolution, external loading = 30 pF.

Pixel Output Pattern

Table 2 shows the output data order from the OV3630. The data output sequence following the first HREF and after VSYNC is: B_{0,0} G_{0,1} B_{0,2} G_{0,3}... B_{0,2046} G_{0,2047}. After the second HREF the output is G_{1,0} R_{1,1} G_{1,2} R_{1,3}... G_{1,2046} R_{1,2047}... etc.

Table 2 Data Pattern

R/C	0	1	2	3	...	2046	2047
0	B _{0,0}	G _{0,1}	B _{0,2}	G _{0,3}	...	B _{0,2046}	G _{0,2047}
1	G _{1,0}	R _{1,1}	G _{1,2}	R _{1,3}	...	G _{1,2046}	R _{1,2047}
2	B _{2,0}	G _{2,1}	B _{2,2}	G _{2,3}	...	B _{2,2046}	G _{2,2047}
3	G _{3,0}	R _{3,1}	G _{3,2}	R _{3,3}	...	G _{3,2046}	R _{3,2047}
.
1534	B _{1534,0}	G _{1534,1}	B _{1534,2}	G _{1534,3}		B _{1534,2046}	G _{1534,2047}
1535	G _{1535,0}	R _{1535,1}	G _{1535,2}	R _{1535,3}		G _{1535,2046}	R _{1535,2047}

Pin Description

Table 3 Pin Description

Pin Number (see Table 4)	Name	Pin Type	Function/Description
A1	PWDN	Input (0) ^a	Power down mode enable, active high
A2	HVDD	Analog	Sensor high reference - connect to ground using a 0.1 μ F capacitor
A3	SGND	Power	Ground for sensor array
A4	OGND	Power	Ground for internal regulator
A5	SIO_C	Input	SCCB serial interface clock input
A6	HREF	Output	Horizontal reference output
B1	RESET	Input (0)	Chip reset, active high
B2	NVDD	Analog	Sensor low reference - connect to ground using a 0.1 μ F capacitor
B3	SVDD	Analog	Sensor internal reference - connect to ground using a 0.1 μ F capacitor
B4	OVDD	Power	2.8 V supply for the internal regulator
B5	SIO_D	I/O	SCCB serial interface data I/O
B6	VSYNC	Output	Vertical synchronization output
C1	FREX	Input (0)	Snapshot trigger - use to activate a snapshot sequence
C2	EXP_STB	Input (0)	Snapshot Exposure Start Trigger 0: Sensor starts exposure (only effective in snapshot mode) 1: Sensor stays in reset mode
C5	DOVDD	Power	2.8 V supply ^b for digital video port
C6	PCLK	Output	Pixel clock output
D1	D0	Output	Video port output bit[0]
D2	D1	Output	Video port output bit[1]
D5	D9	Output	Video port output bit[9]
D6	D8	Output	Video port output bit[8]
E1	D2	Output	Video port output bit[2]
E2	NC	–	No connect
E5	D7	Output	Video port output bit[7]
E6	D6	Output	Video port output bit[6]
F1	D3	Output	Video port output bit[3]
F2	NC	–	No connect
F3	EGND	Power	Ground
F4	XVCLK	Input	System clock input
F5	DVDD	Analog	Digital internal reference - connect to ground using a 0.1 μ F capacitor
F6	D5	Output	Video port output bit[5]
G1	EVDD	Power	1.8 V supply
G2	NC	–	No connect
G3	NC	–	No connect
G4	PVDD	Analog	PLL internal reference - connect to ground using a 0.1 μ F capacitor
G5	DOGND	Power	Ground for digital video port
G6	D4	Output	Video port output bit[4]

a. Input (0) represents an internal pull-down resistor.

b. Contact your local OmniVision FAE for 1.8V I/O support.

Figure 11 Pinout Diagram

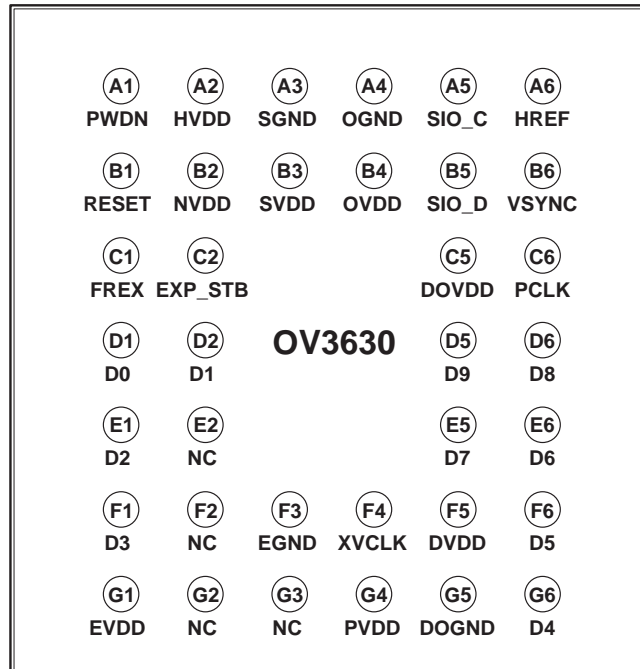


Table 4 Ball Matrix

	1	2	3	4	5	6
A	PWDN	HVDD	SGND	OGND	SIO_C	HREF
B	RESET	NVDD	SVDD	OVDD	SIO_D	VSYNC
C	FREX	EXP_STB			DOVDD	PCLK
D	D0	D1			D9	D8
E	D2	NC			D7	D6
F	D3	NC	EGND	XVCLK	DVDD	D5
G	EVDD	NC	NC	PVDD	DOGND	D4

Electrical Characteristics

Table 5 Absolute Maximum Ratings

Ambient Storage Temperature		-40°C to +95°C
Supply Voltages (with respect to Ground)	V_{DD-A}	4.5V
	V_{DD-C}	3V
	V_{DD-IO}	4.5V
All Input/Output Voltages (with respect to Ground)		-0.3V to V _{DD-IO} +0.5V
Lead-free Temperature, Surface-mount process		245°C
ESD Rating, Human Body model		2000V

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 6 DC Characteristics (-20°C < T_A < 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
V _{DD-A}	Supply voltage (OVDD)	2.66	2.8	2.94	V
V _{DD-C}	Supply voltage (EVDD)	1.71	1.8	1.89	V
V _{DD-IO}	Supply voltage (DOVDD) ^a	1.7	2.8	3.3	V
I _{DDA-A}	Active (Operating) Current (OVDD) ^b		TBD		mA
I _{DDA-C}	Active (Operating) Current (EVDD) ^b		TBD		mA
I _{DDA-IO}	Active (Operating) Current (DOVDD) ^b		TBD		mA
I _{DDS-SCCB}	Standby Current ^b		TBD		mA
I _{DDS-PWDN}			TBD	TBD	μA
Digital Inputs					
V _{IL}	Input voltage LOW			0.8	V
V _{IH}	Input voltage HIGH	2			V
C _{IN}	Input capacitor			10	pF
Digital Outputs (standard loading 25 pF, 1.2 KΩ to 2.8 V)					
V _{OH}	Output voltage HIGH	2.2			V
V _{OL}	Output voltage LOW			0.6	V
Serial Interface Inputs					
V _{IL}	SIO_C and SIO_D	-0.5	0	1	V
V _{IH}	SIO_C and SIO_D	2.5	2.8	V _{DD-IO} + 0.5	V

a. 1.8V I/O is supported. Contact your OmniVision FAE for further details.

b. V_{DD-A} = 2.8V, V_{DD-C} = 1.8V, and V_{DD-IO} = 2.8V

I_{DDS-SCCB} refers to a SCCB-initiated Standby, while I_{DDS-PWDN} refers to a PWDN pin-initiated Standby

Table 7 AC Characteristics ($T_A = 25^\circ\text{C}$, $V_{DD-A} = 2.8\text{V}$)

Symbol	Parameter	Min	Typ	Max	Unit
ADC Parameters					
B	Analog bandwidth		28		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	Settling time for hardware reset			<1	ms
	Settling time for software reset			<1	ms
	Settling time for XGA/QXGA mode change			<1	ms
	Settling time for register setting			<300	ms

Table 8 Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Oscillator and Clock Input					
f_{OSC}	Frequency (XVCLK)	6	24		MHz
t_r, t_f	Clock input rise/fall time			5	ns
	Clock input duty cycle	45	50	55	%

Timing Specifications

Figure 12 SCCB Timing Diagram

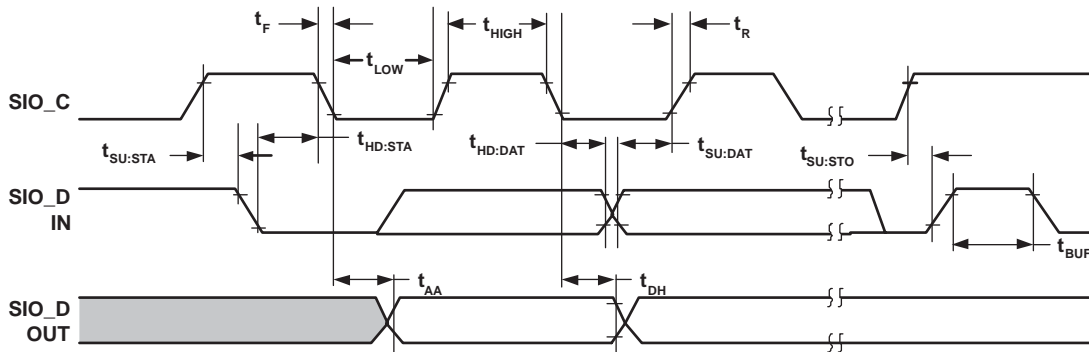


Table 9 SCCB Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			μ s
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			μ s
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			μ s
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns

Figure 13 QXGA, XGA, and HF Mode Line/Pixel Output Timing

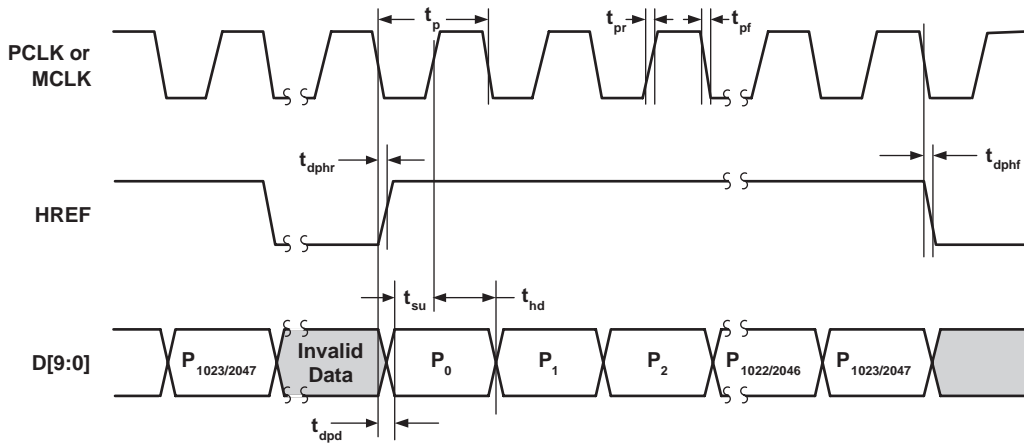


Table 10 Pixel Timing Specification

Symbol	Parameter	Min	Typ	Max	Unit
t_p	PCLK period		18.3		ns
t_{pr}	PCLK rising time		3.5		ns
t_{pf}	PCLK falling time		2.2		ns
t_{dphr}	PCLK negative edge to HREF rising edge	0		5	ns
t_{dphf}	PCLK negative edge to HREF negative edge	0		5	ns
t_{dpd}	PCLK negative edge to data output delay	0		5	ns
t_{su}	Data bus setup time	15			ns
t_{hd}	Data bus hold time	8			ns

Figure 14 QXGA Frame Timing

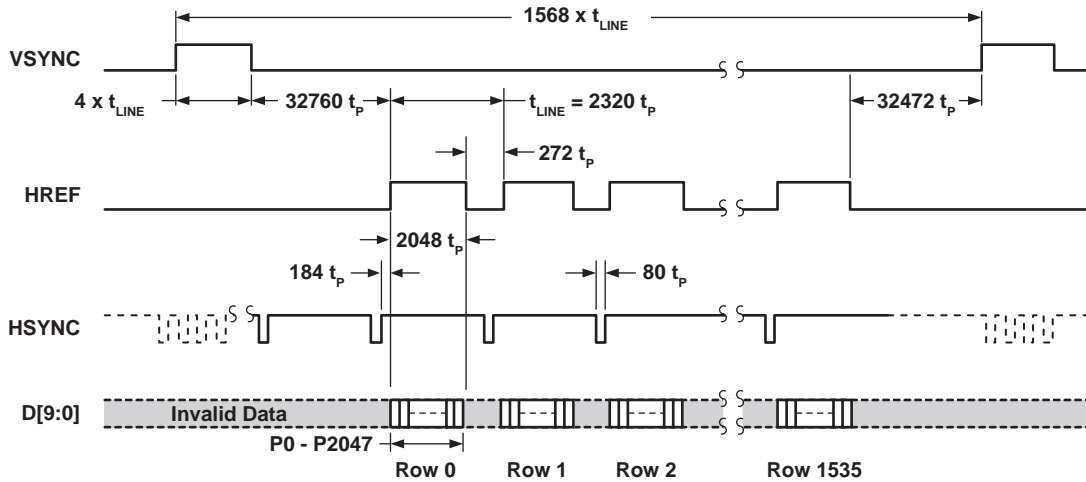


Figure 15 XGA Frame Timing (if PIDL = 0x30)

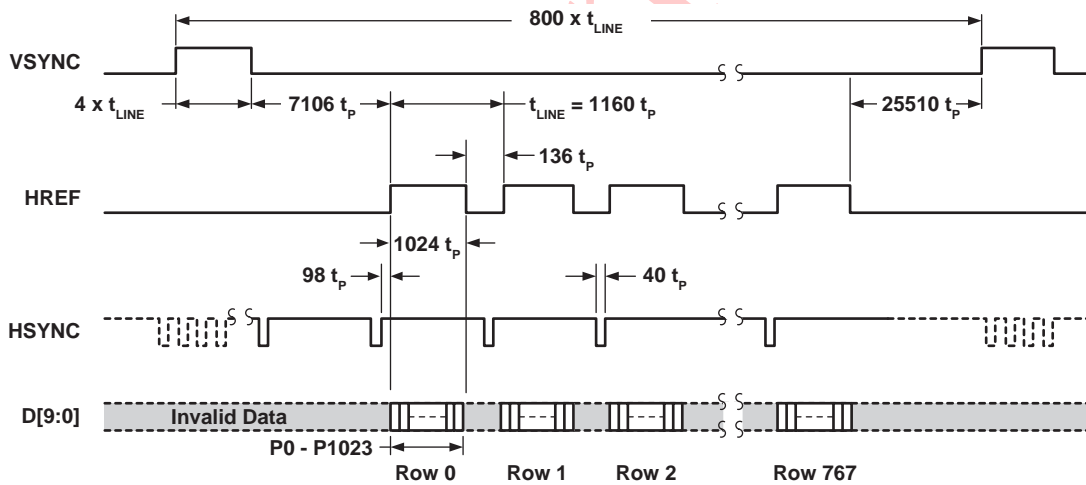


Figure 16 XGA Frame Timing (if PIDL ≠ 0x30)

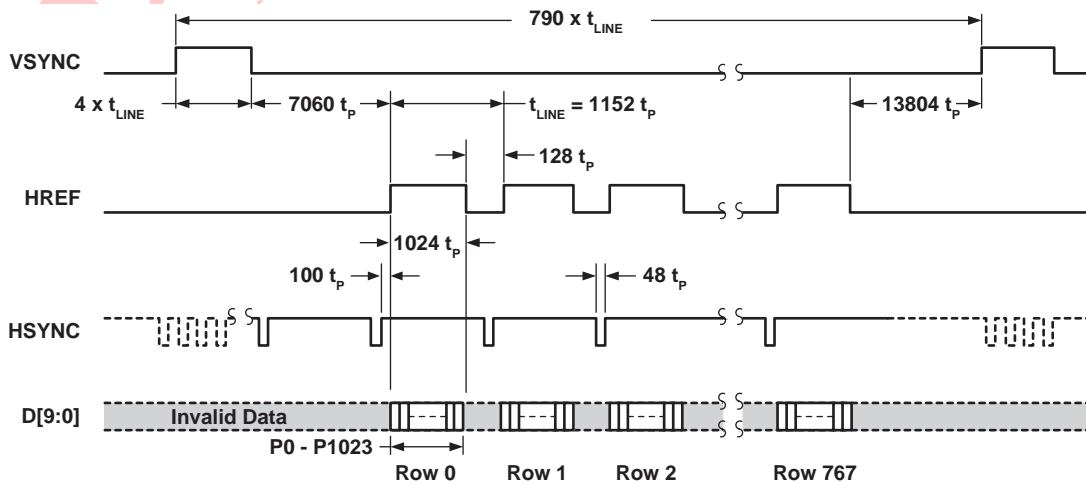


Figure 17 XGA Zoom Frame Timing

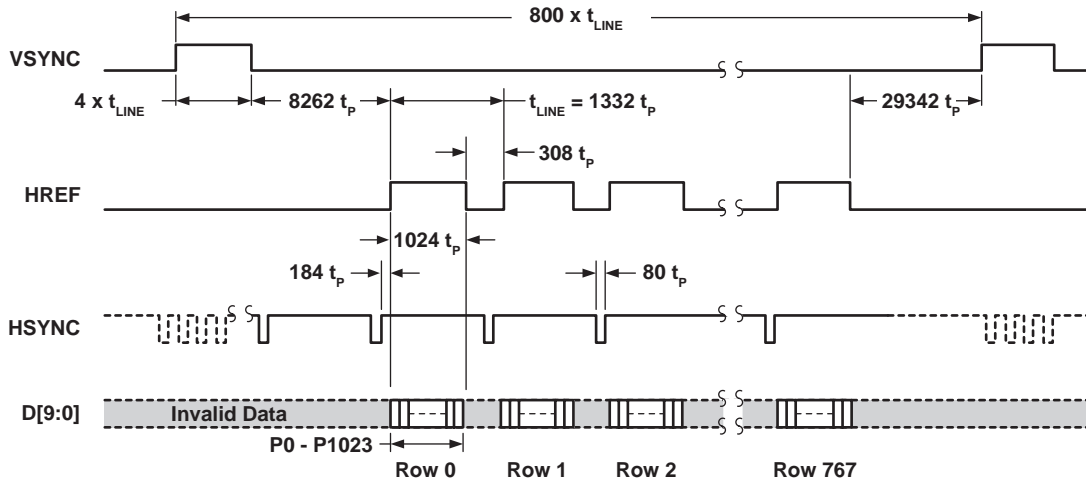


Figure 18 HF Mode Frame Timing (if PIDL = 0x30)

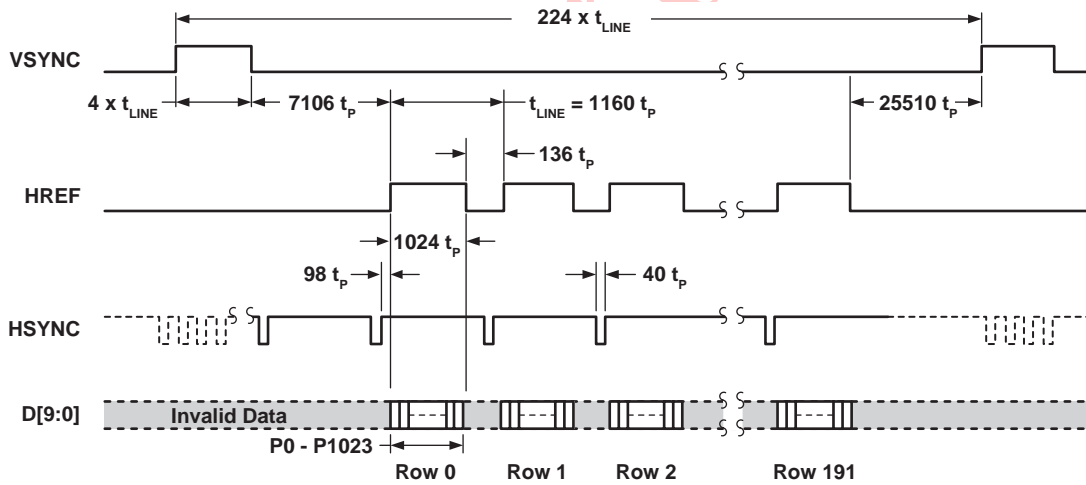


Figure 19 HF Mode Frame Timing (if PIDL ≠ 0x30)

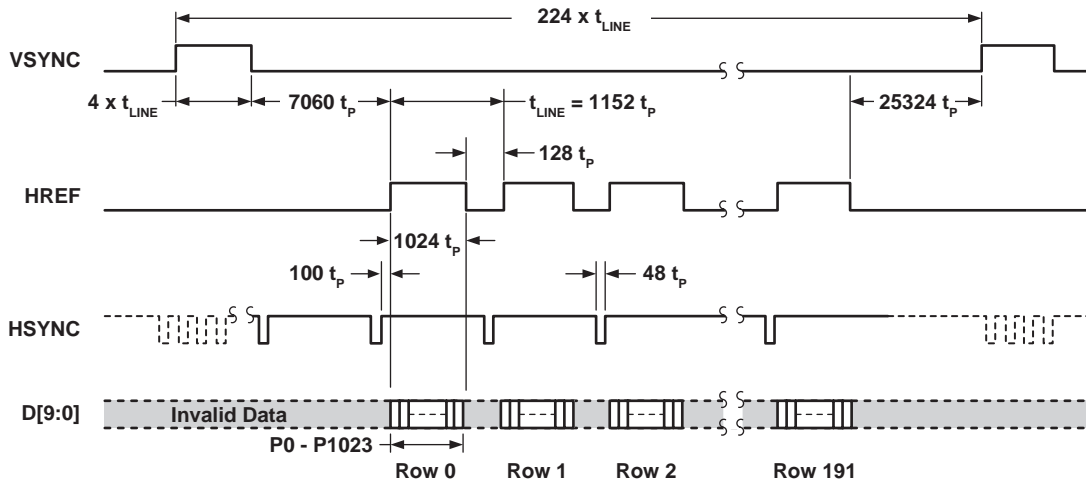


Figure 20 HF Mode Zoom Frame Timing

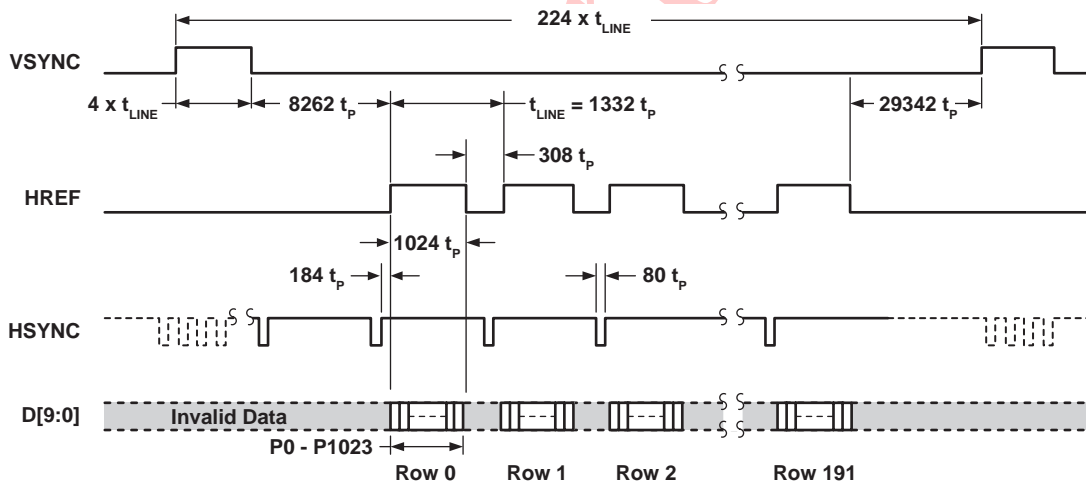


Figure 21 Frame Exposure Mode Timing with EXP_STB Asserted

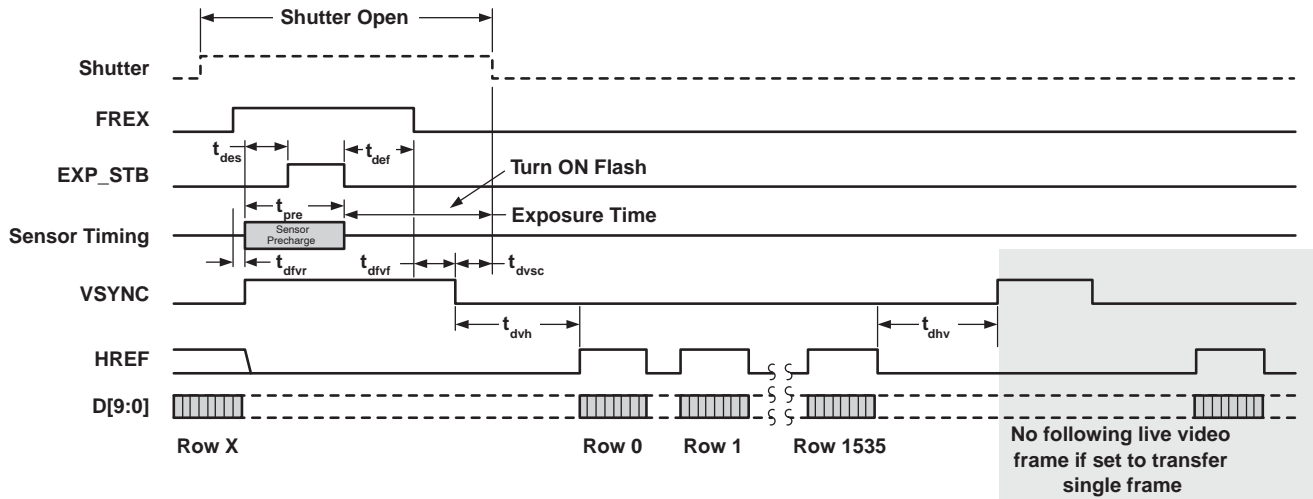


Table 11 Frame Exposure Timing Specifications

Symbol	Min	Typ	Max	Unit
tline		2320 (QXGA)		tp
		1160 (XGA) (if PIDL = 0x30) 1152 (XGA) (if PIDL ≠ 0x30)		tp
tv		4		tline
tdfvr	8		9	tp
tdfvf			4	tline
tdvsc			2	tline
tdhv		32472 (QXGA)		tp
		29342 (XGA)		tp
tdvh		32760 (QXGA)		tp
		8262 (XGA)		tp
tdhso	0			ns
tdef	20			tp
tdes			2300 (QXGA)	tp
			1300 (XGA)	tp

NOTE 1) FREX must stay high long enough to ensure the entire sensor has been reset.
 2) Shutter must be closed no later than 4640 tp (2664 tp for XGA) after VSYNC falling edge.

Register Set

Table 12 provides a list and description of the Device Control registers contained in the OV3630. The device slave addresses for the OV3630 are 60 for write and 61 for read.

Table 12 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC Gain Control Bit[7:0]: Gain setting • Range: 1x to 32x $\text{Gain} = (\text{Bit}[7]+1) \times (\text{Bit}[6]+1) \times (\text{Bit}[5]+1) \times (\text{Bit}[4]+1) \times (1+\text{Bit}[3:0]/16)$ <i>Note: Set COM8[2] = 0 to disable AGC.</i>
01	BLUE	80	RW	Digital AWB Blue Gain Control • Range: 0 to 2x ([00] to [FF])
02	RED	80	RW	Digital AWB Red Gain Control • Range: 0 to 2x ([00] to [FF])
03	COM1	0F (0A in XGA, 06 in HF)	RW	Common Control 1 Bit[7:6]: Dummy frame control 00: Not used 01: Allow 1 dummy frame 10: Allow 3 dummy frames 11: Allow 7 dummy frames Bit[5:4]: Reserved Bit[3:2]: Vertical window end line control 2 LSBs Bit[1:0]: Vertical window start line control 2 LSBs
04	REG04	00	RW	Register 04 Bit[7]: Horizontal mirror Bit[6]: Vertical flip Bit[5]: Reserved Bit[4]: VREF[0] Bit[3]: HREF[0] Bit[2]: Reserved Bit[1:0]: AEC lower 2 bits – AEC[1:0]
05	BAVG	00	RW	B Channel Average
06	GbAVG	00	RW	G Channel Average - Picked G pixels in the same line with B pixels.
07	GrAVG	00	RW	G Channel Average - Picked G pixels in the same line with R pixels.
08	RAVG	00	RW	R Channel Average

Table 12 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
09	COM2	01	RW	Common Control 2 Bit[7:5]: Reserved Bit[4]: Sleep mode enable 0: Normal mode 1: Sleep mode Bit[3]: Reserved Bit[2]: Pin PWDN/RESET used as SLVS/SLHS Bit[1:0]: Output drive current select 00: Weakest 01: Double capability 10: Double capability 11: Triple drive current
0A	PIDH	36	R	Product ID Number MSB (Read only)
0B	PIDL	30	R	Product ID Number LSB (Read only)
0C	COM3	38	RW	Common Control 3 Bit[7]: Reserved Bit[6]: Swap MSB and LSB at the output port Bit[5:1]: Reserved Bit[0]: Snapshot option 0: Enable live video output after snapshot sequence 1: Output single frame only
0D	COM4	06	RW	Common Control 4 Bit[7:3]: Reserved Bit[2]: Clock output power-down pin status 0: Tri-state data output pin at power-down 1: Data output pin hold at last status before power-down Bit[1]: Data output pin status selection at power-down 0: Tri-state VSYNC, PCLK, HREF and HSYNC pins upon power-down 1: VSYNC, PCLK, HREF and HSYNC hold on last states before power-down Bit[0]: Reserved
0E	COM5	01	RW	Common Control 5 Bit[7]: Reserved - always set to "1" Bit[6:0]: Reserved

Table 12 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0F	COM6	43	RW	Common Control 6 Bit[7:4]: Reserved Bit[3]: Night mode enable 0: Disable 1: Enable Bit[2]: Reserved Bit[1]: Reset enable/disable when sensor working mode changes 0: Sensor timing not reset when mode changes 1: Sensor timing resets when mode changes Bit[0]: Reserved
10	AEC	43	RW	Automatic Exposure Control - AEC[9:2] MSB 6 bits, AEC[15:10], is in REG45[5:0] and LSB 2 bits, AEC[1:0], is in register REG04[1:0]. AEC[15:0]:Exposure time $T_{EX} = t_{LINE} \times AEC[15:0]$ <i>Note: The maximum exposure time is 1 frame period even if T_{EX} is longer than 1 frame period.</i>
11	CLKRC	00	RW	Clock Rate Control Bit[7:6]: Reserved Bit[5:0]: Clock divider $CLK = XVCLK / (\text{decimal value of } CLKRC[5:0] + 1)$
12	COM7	00	RW	Common Control 7 Bit[7]: SRST 1: Initiates soft reset. All register are set to factory default values after which the chip resumes normal operation Bit[6:4]: Resolution selection 000: QXGA (full size) mode 001: High Frame rate (HF) mode 100: XGA mode Bit[3]: Master/Slave mode selection 0: Master mode 1: Slave mode Bit[2]: Zoom mode Bit[1:0]: Reserved

Table 12 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
13	COM8	C7	RW	Common Control 8 Bit[7]: AEC speed selection 0: Normal 1: Faster AEC correction Bit[6:3]: Reserved Bit[2]: AGC auto/manual control selection 0: Manual 1: Auto Bit[1]: AWB auto/manual control selection 0: Manual 1: Auto Bit[0]: Exposure control 0: Manual 1: Auto
14	COM9	40	RW	Common Control 9 Bit[7:5]: AGC gain ceiling 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101: Reserved 110: Reserved 111: Reserved Bit[4:3]: Reserved Bit[2]: VSYNC drop option 0: VSYNC is always output 1: VSYNC is dropped if frame data is dropped Bit[1]: Frame data drop 0: Disable data drop 1: Drop frame data if exposure is not within tolerance. In AEC mode, data is normally dropped when data is out of range. Bit[0]: Reserved

Table 12 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
15	COM10	00	RW	<p>Common Control 10</p> <p>Bit[7]: Reserved</p> <p>Bit[6]: HREF pin output swap 0: HREF 1: HSYNC</p> <p>Bit[5]: PCLK output selection 0: PCLK always output 1: PCLK output qualified by HREF</p> <p>Bit[4]: PCLK edge selection 0: Data is updated at the falling edge of PCLK (user can latch data at the next rising edge of PCLK) 1: Data is updated at the rising edge of PCLK (user can latch data at the next falling edge of PCLK)</p> <p>Bit[3]: HREF output polarity 0: Output positive HREF 1: Output negative HREF, HREF negative for valid data</p> <p>Bit[2]: Reserved</p> <p>Bit[1]: VSYNC polarity 0: Positive 1: Negative</p> <p>Bit[0]: HSYNC polarity 0: Positive 1: Negative</p>
16	GREEN	80	RW	<p>Digital AWB Green Gain Control</p> <ul style="list-style-type: none"> Range: 0 to 2x ([00] to [FF])
17	HREFST	10	RW	<p>Horizontal Window Start 8 MSBs (3 LSBs in REG32[2:0])</p> <p>Bit[10:0]: Select beginning of horizontal window, each LSB represents two pixels</p>
18	HREFEND	90 (50 in XGA, HF)	RW	<p>Horizontal Window End 8 MSBs (3 LSBs in REG32[5:3])</p> <p>Bit[10:0]: Select end of horizontal window, each LSB represents two pixels</p>
19	VSTRT	01 (00 in XGA, HF)	RW	<p>Vertical Window Line Start 8 MSBs (2 LSBs in register COM1[1:0])</p> <p>Bit[9:0]: Selects the start of the vertical window, each LSB represents two scan lines.</p>
1A	VEND	C1 (60 in XGA, 18 in HF)	RW	<p>Vertical Window Line End 8 MSBs (2 LSBs in register COM1[3:2])</p> <p>Bit[9:0]: Selects the end of the vertical window, each LSB represents two scan lines.</p>
1B	PSHFT	00	RW	<p>Pixel Shift</p> <p>Bit[7:0]: Pixel delay count - provides a method to fine tune the output timing of the pixel data relative to the HREF pulse. It physically shifts the video data output time in units of pixel clock counts. The largest delay count is [FF] and is equal to 255 x PCLK.</p>
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)

Table 12 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E-23	RSVD	XX	–	Reserved
24	AEW	78	RW	Luminance Signal High Range for AEC/AGC operation AEC/AGC value decreases in auto mode when average luminance is greater than AEW[7:0]
25	AEB	68	RW	Luminance Signal Low Range for AEC/AGC operation AEC/AGC value increases in auto mode when average luminance is less than AEB[7:0]
26	VV	D4	RW	Fast Mode Large Step Range Thresholds - effective only in AEC/AGC fast mode Bit[7:4]: 4 MSBs of high threshold Bit[3:0]: 4 MSBs of low threshold AEC/AGC may change in larger steps when the luminance average is greater than the high threshold or less than the low threshold.
27-29	RSVD	XX	–	Reserved
2A	REG2A	00	RW	Register 2A Bit[7:4]: Line interval adjust value MSB 4 bits, LSBs in register FRARL[7:0] Bit[3:2]: HSYNC timing end point adjustment MSB 2 bits Bit[1:0]: HSYNC timing start point adjustment MSB 2 bits
2B	FRARL	00	RW	Line Interval Adjustment Value LSB 8 bits The frame rate will be adjusted by changing the line interval. Each LSB will add $1/2320 T_{frame}$ in QXGA. Each 2 LSBs will add $1/1160 T_{frame}$ in XGA and HF modes (if $PIDL = 0x30$) or $1/1152 T_{frame}$ in XGA and HF modes (if $PIDL \neq 0x30$) to the frame period.
2C	RSVD	XX	–	Reserved
2D	ADDVSL	00	RW	VSYNC Pulse Width LSB 8 bits Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is $4 \times t_{line}$. Each LSB count will add $1 \times t_{line}$ to the VSYNC active period.
2E	ADDVSH	00	RW	VSYNC Pulse width MSB 8 bits Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is $4 \times t_{line}$. Each MSB count will add $256 \times t_{line}$ to the VSYNC active period.
2F	YAVG	00	RW	Luminance Average - this register will auto update Average luminance is calculated from the B/Gb/Gr/R channel average as follows: B/Gb/Gr/R channel average = $(BAVG[7:0] + GbAVG[7:0] + GrAVG[7:0] + RAVG[7:0]) \times 0.25$
30	HSDY	08	RW	HSYNC Position and Width Start LSB 8 bits This register and REG2A[1:0] define the HSYNC start position. Each LSB will shift HSYNC starting point by a 2 pixel period.

Table 12 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
31	HEDY	30	RW	HSYNC Position and Width End LSB 8 bits This register and REG2A[3:2] define the HSYNC end position. Each LSB will shift HSYNC end point by a 2 pixel period.
32	REG32	36 (09 in XGA, HF)	RW	Register 32 Bit[7:6]: Pixel clock divide option 00: No effect on PCLK 01: No effect on PCLK 10: PCLK frequency divide by 2 11: PCLK frequency divide by 4 Bit[5:3]: Horizontal window end position LSBs Bit[2:0]: Horizontal window start position LSBs
33	RSVD	XX	–	Reserved
34	ZOOMW	00	RW	Zoom Horizontal Start Point Bit[7:3]: Reserved Bit[2:0]: Zoom horizontal start point
35-44	RSVD	XX	–	Reserved
45	REG45	00	RW	REG45 Bit[7:6]: Reserved Bit[5:0]: AEC[15:10], AEC MSBs
46	FLL	00	RW	Frame Length Adjustment LSBs Each bit will add 1 horizontal line timing in frame
47	FLH	00	RW	Frame Length Adjustment MSBs Each bit will add 256 horizontal line timing in frame
48	ZOOMSL	00	–	Common Control 19 Bit[7:2]: Reserved Bit[1:0]: Zoom mode vertical start window 2 LSBs (see register ZOOMSH[7:0] (0x49) for 8 MSBs)
49	ZOOMSH	00	RW	Zoom Mode Vertical Window Start Point 8 MSBs
4A-74	RSVD	00	–	Reserved

NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.

Package Specifications

The OV3630 uses a 36-pin Chip Scale Package 2 (CSP2). Refer to [Figure 22](#) for package information, [Table 13](#) for package dimensions and [Figure 23](#) for the array center on the chip.



Note: For OVT devices that are lead-free, all part marking letters are lower case. Underlining the last digit of the lot number indicates CSP2 is used.

Figure 22 OV3630 Package Specifications

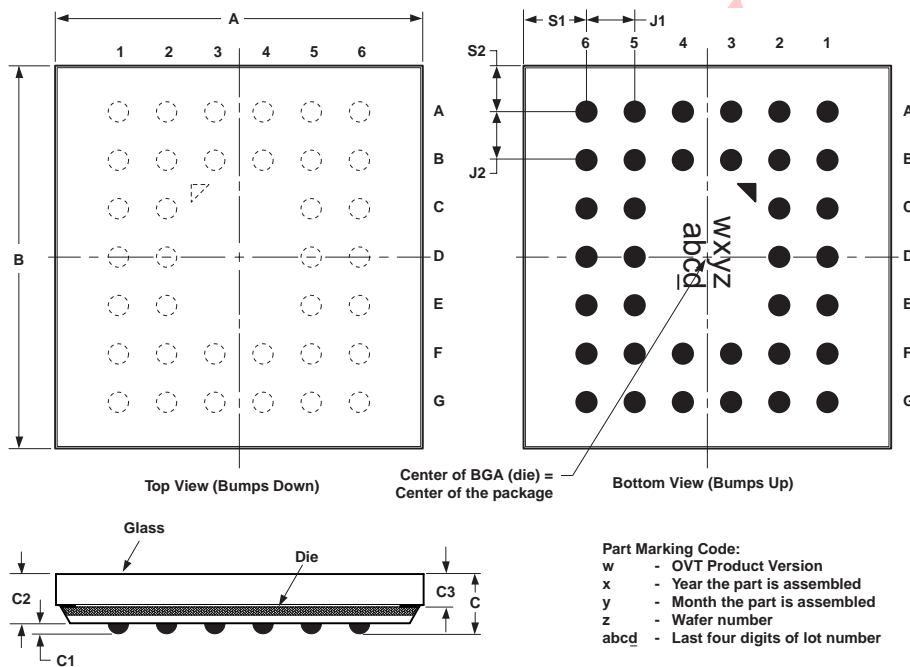
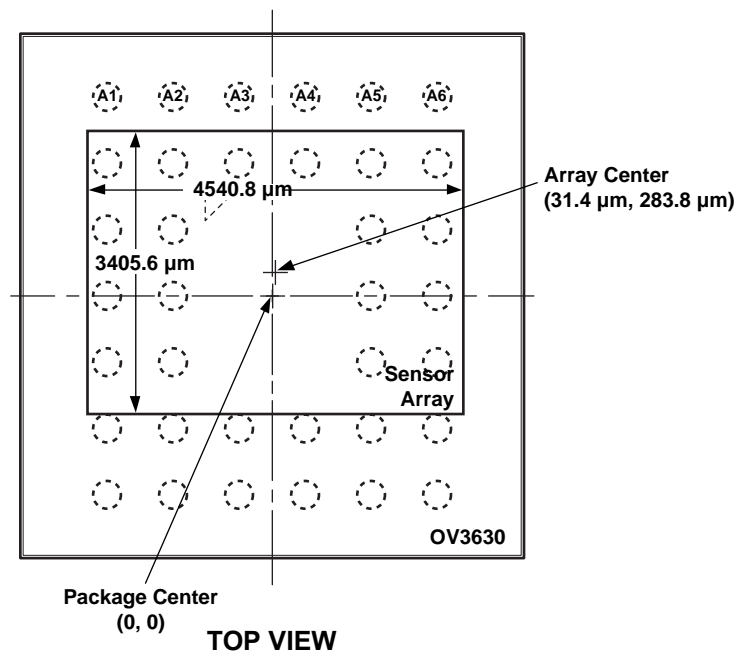


Table 13 CSP2 Package Dimensions

Parameter	Symbol	Min	Nominal	Max	Unit
Package Body Dimension X	A	6060	6085	6110	µm
Package Body Dimension Y	B	6290	6315	6340	µm
Package Height	C	845	905	965	µm
Ball Height	C1	150	180	210	µm
Package Body Thickness	C2	680	725	770	µm
Thickness of Glass Surface to Wafer	C3	425	445	465	µm
Ball Diameter	D	320	350	380	µm
Total Pin Count	N		36 (4 NC)		
Pin Count X-axis	N1		6		
Pin Count Y-axis	N2		7		
Pins Pitch X-axis	J1		800		µm
Pins Pitch Y-axis	J2		800		µm
Edge-to-Pin Center Distance Analog X	S1	1013	1043	1073	µm
Edge-to-Pin Center Distance Analog Y	S2	728	758	788	µm

Sensor Array Center

Figure 23 OV3630 Sensor Array Center



- NOTES:**
1. This drawing is not to scale and is for reference only.
 2. As most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A6 oriented down on the PCB.

Pre-release

IR Reflow Ramp Rate Requirements

OV3630 Lead-Free Packaged Devices



Note: For OVT devices that are lead-free, all part marking letters are lower case

Figure 24 IR Reflow Ramp Rate Requirements

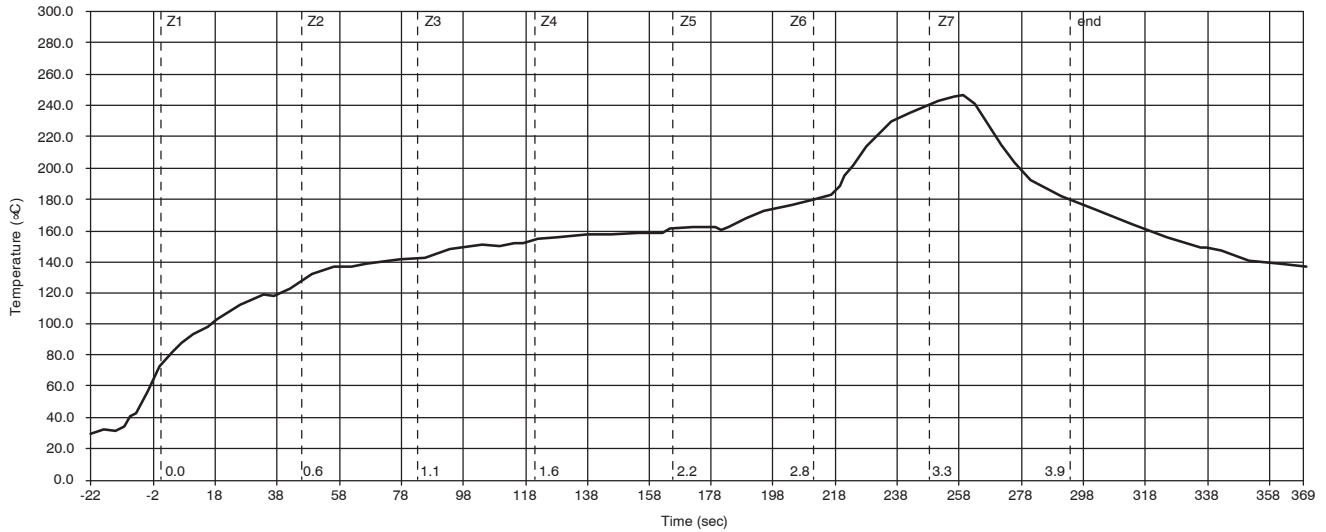


Table 14 Reflow Conditions

Condition	Exposure
Average Ramp-up Rate (30°C to 217°C)	Less than 3°C per second
> 100°C	Between 330 - 600 seconds
> 150°C	At least 210 seconds
> 217°C	At least 30 seconds (30 ~ 120 seconds)
Peak Temperature	Greater than or equal to 245°C
Cool-down Rate (Peak to 50°C)	Less than 6°C per second
Time from 30°C to 255°C	No greater than 390 seconds

Note:

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REVISION CHANGE LIST

Document Title: OV3630 Datasheet

Version: 1.0

DESCRIPTION OF CHANGES

Initial Release



REVISION CHANGE LIST

Document Title: OV3630 Datasheet

Version: 1.1

DESCRIPTION OF CHANGES

The glass of the CSP2 package used was changed from 500 μ m to 400 μ m. As a result, the following changes were made to version 1.0:

- In Table 13 on page 23, changed Min, Nominal, and Max specifications for the Package Height (C) parameter to “845”, “905”, and “965”, respectively.
- In Table 13 on page 23, changed Min, Nominal, and Max specifications for the Package Body Thickness (C2) parameter to “680”, “725”, and “770”, respectively.
- In Table 13 on page 23, changed Min, Nominal, and Max specifications for the Thickness of Glass Surface to Wafer (C3) parameter to “425”, “445”, and “465”, respectively.
- In Table 6 on page 10, changed Min and Max specifications for Supply Voltage (DOVDD)^a parameter from “2.5” and “VDD-A+0.3V” to “1.7” and “3.3”, respectively.
- In the table under Key Specifications on page 1, changed the specification for Power Supply (I/O) from “2.8VDC \pm 5%” to “1.7 ~ 3.3V”



REVISION CHANGE LIST

Document Title: OV3630 Datasheet

Version: 1.2

DESCRIPTION OF CHANGES

The following changes were made to version 1.1:

- In the Channel Balance section on page 3, changed the first line from “The amplified signals are then ...” to “The digitized signals are then ...”
- In the Channel Balance section on page 3, deleted “and gamma correction is performed” from the last line of the paragraph.
- In the Black Level Compensation section on page 3, changed the first line from “After the pixel data has been digitized, black level ...” to “After the pixel data has been channel balanced, black level ...”
- Under Power Down Mode section (2nd column) on page 6, changed the last line of the last paragraph of the section from “... All register content is maintained in mode” to “... All register content is maintained in this mode”
- In Table 12 on page 19, changed description of register bit COM4[1] from:
Bit[1]: Data output pin status selection at power-down
0: Tri-state VSYNC, PCLK, HREF and CHSYNC pins upon power-down
1: VSYNC, PCLK, HREF and CHSYNC hold on last states before power-down
to:
Bit[1]: Data output pin status selection at power-down
0: Tri-state VSYNC, PCLK, HREF and HSYNC pins upon power-down
1: VSYNC, PCLK, HREF and HSYNC hold on last states before power-down
- In Table 12 on page 23, changed description for register VV (0x26) from:
Fast Mode Large Step Range Thresholds - effective only in AEC/AGC fast mode
Bit[7:4]: High threshold
Bit[3:0]: Low threshold
to:
Fast Mode Large Step Range Thresholds - effective only in AEC/AGC fast mode
Bit[7:4]: 4 MSBs of high threshold
Bit[3:0]: 4 MSBs of low threshold
- In Table 12 on page 22, changed description for register bit COM10[6] (0x15) from Reserved to:
Bit[6]: HREF pin output swap
0: HREF
1: HSYNC
- On page 14, changed title of Figure 15 from “XGA Frame Timing” to “XGA Frame Timing (if PIDL = 0x30)”



DESCRIPTION OF CHANGES (CONTINUED)

- On page 14, changed the following callouts in Figure 15: “8262 t_p” to “7106 t_p”, “1332 t_p” to “1160 t_p”, “29342 t_p” to “25510 t_p”, “184 t_p” to “98 t_p”, “308 t_p” to “136 t_p”, and “80 t_p” to “40 t_p”
- On page 14, added Figure 16, XGA Frame Timing (if PIDL ≠ 0x30)
- On page 15, added Figure 17, XGA Zoom Frame Timing
- On page 15, changed title of Figure 18 (previously Figure 16) from “HF Frame Timing” to “HF Frame Timing (if PIDL = 0x30)”
- On page 15, changed the following callouts in Figure 18: “8262 t_p” to “7106 t_p”, “1332 t_p” to “1160 t_p”, “29342 t_p” to “25510 t_p”, “184 t_p” to “98 t_p”, “308 t_p” to “136 t_p”, and “80 t_p” to “40 t_p”
- On page 16, added Figure 19, HF Mode Frame Timing (if PIDL ≠ 0x30)”
- On page 16, added Figure 20, HF Mode Zoom Frame Timing
- Under Frame Rate Timing subsection in column 1 on page 5, changed the first sentence from “Default frame timing is illustrated in Figure 14, Figure 15, and Figure 16” to “Default frame timing is illustrated in Figure 14, Figure 15 (if PIDL = 0x30), Figure 16 (if PIDL ≠ 0x30), Figure 17, Figure 18 (if PIDL = 0x30), Figure 19 (if PIDL ≠ 0x30), and Figure 20”
- In Table 12 on page 22, changed last line in the description of register VV (0x26) from “AEC/AGC may change in larger steps when luminance average is greater than VV[7:4] or less than VV[3:0]” to “AEC/AGC may change in larger steps when the luminance average is greater than the high threshold or less than the low threshold.”
- Under Windowing section on page 3, changed text from “... Window size setting (in pixels) ranges from 2 x 4 to 2064 x 1540 (QXGA), 2 x 2 to 1032 x 772 (XGA), or 1032 x 192 (HF), and can be anywhere inside the 2064 x 1540 boundary” to “Window size setting (in pixels) ranges from 2 x 4 to 2056 x 1542 (QXGA), 2 x 2 to 1028 x 774 (XGA), or 1028 x 192 (HF), and can be anywhere inside the 2056 x 1542 boundary”
- In Table 12 on page 20, changed description for register CLKRC (0x11) from:

Bit[7]: Reserved
Bit[6]: Digital video port master/slave selection
0: Master mode, sensor provides PCLK
1: Slave mode, external PCLK input from XCLK1 pin

to:

Bit[7:6]: Reserved



DESCRIPTION OF CHANGES (CONTINUED)

- In Table 12 on page 23, changed description for register FRAFL (0x2B) from:
The frame rate will be adjusted by changing the line interval. Each LSB will add $1/2320 T_{\text{frame}}$ in QXGA and $1/1332 T_{\text{frame}}$ in XGA mode to the frame period.
to:
The frame rate will be adjusted by changing the line interval. Each LSB will add $1/2320 T_{\text{frame}}$ in QXGA. Each 2 LSBs will add $1/1160 T_{\text{frame}}$ in XGA and HF modes (if PIDL = 0x30) or $1/1152 T_{\text{frame}}$ in XGA and HF modes (if PIDL \neq 0x30) to the frame period.
- In Table 11 on page 17, changed Typ specification for tline from “1332 (XGA)” to “1160 (XGA) (if PIDL = 0x30) 1152 (XGA) (if PIDL \neq 30)”
- Under Key Specifications on page 1, changed specifications for Active Power Requirements from “< 110 mW^a” to “TBD”
- Under Key Specifications on page 1, changed specifications for Standby Power Requirements from “10 μ A” to “TBD”
- Under Key Specifications on page 1, deleted table footnote “@ 15 fps, QXGA, without I/O power consumption - needs to be verified”
- In Power Down Mode subsection on page 6 (second column), deleted “The current draw is less than 10 μ A in this mode” and “The current requirements drop to less than 1 mA in this mode.”
- In Table 6 on page 10, changed Typ specifications for Active Operating Current ($I_{\text{DDA-A}}$), Active Operating Current ($I_{\text{DDA-C}}$), Active Operating Current ($I_{\text{DDA-IO}}$), and Standby Current ($I_{\text{DDS-SCCB}}$ and $I_{\text{DDS-PWDN}}$) to “TBD”
- In Table 6 on page 10, changed Max specification for Standby Current ($I_{\text{DDS-SCCB}}$ and $I_{\text{DDS-PWDN}}$) to “TBD”