



S5K3H1GX

Application note

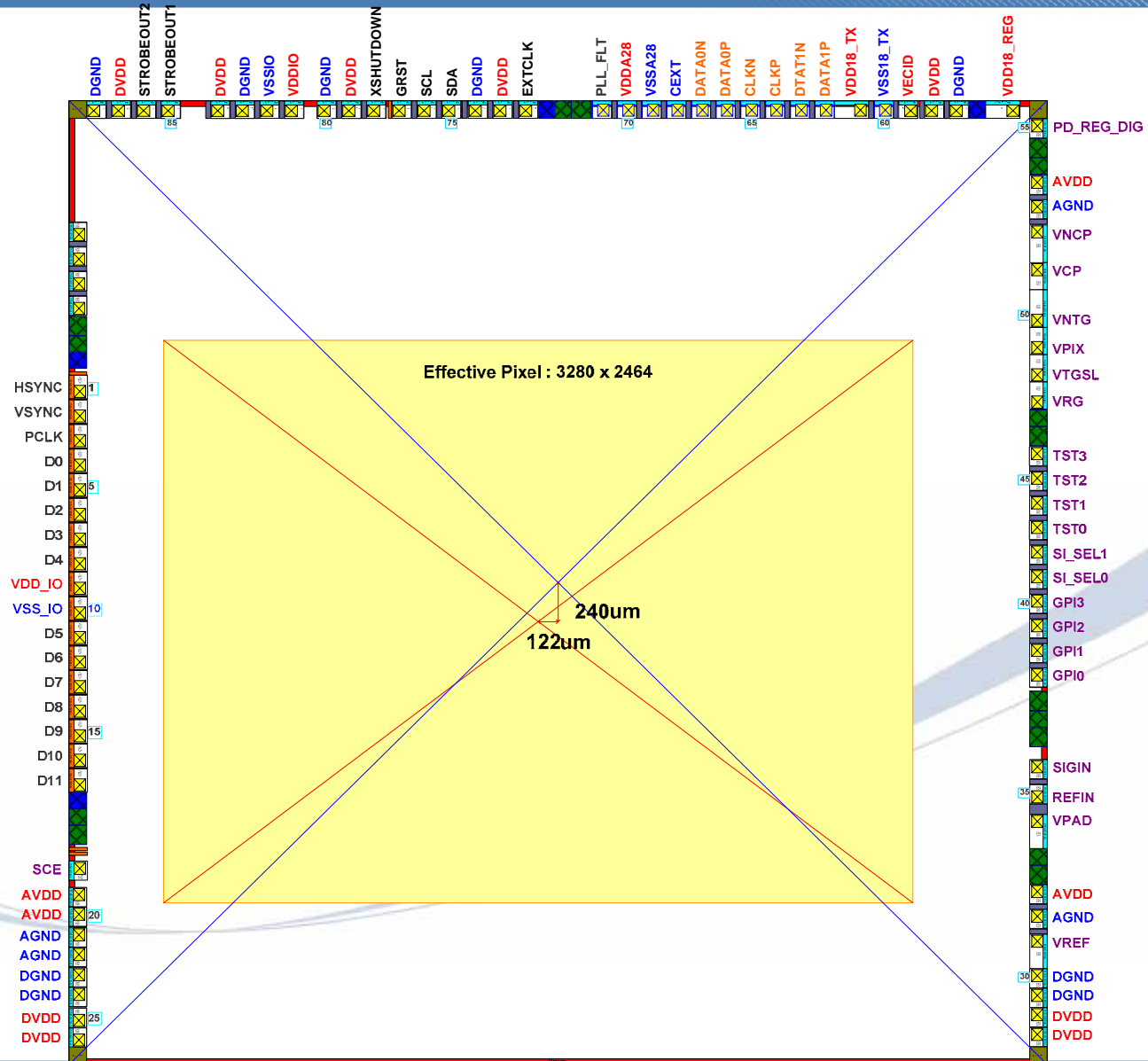
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Document revision history

Date	Amendment
2008.12.15	Initial draft
2009.01.21	Added 12-17page
2009.04.23	Added shutter forbidden area on 8 page
2009.05.15	Modified 7, 8, 12 page
2009.05.20	Modified 7 page
2009.06.15	Modified 7 page
2009.06.29	Modified 16 page
2009.08.13	Modified 7, 11 page
2009.08.28	Modified 8, 12 page
2009.09.14	Added channel gain on 9 page
2009.09.22	Added mode change on 19 page
2009.09.24	Modified 14 ~ 17 page
2009.10.26	Modified 13 page
2009.12.07	Modified 17 page
2009.12.17	Removed channel gain, Modified 11, 12 page
2009.12.21	Modified 15 page

Pin configuration



Operation mode

HW standby

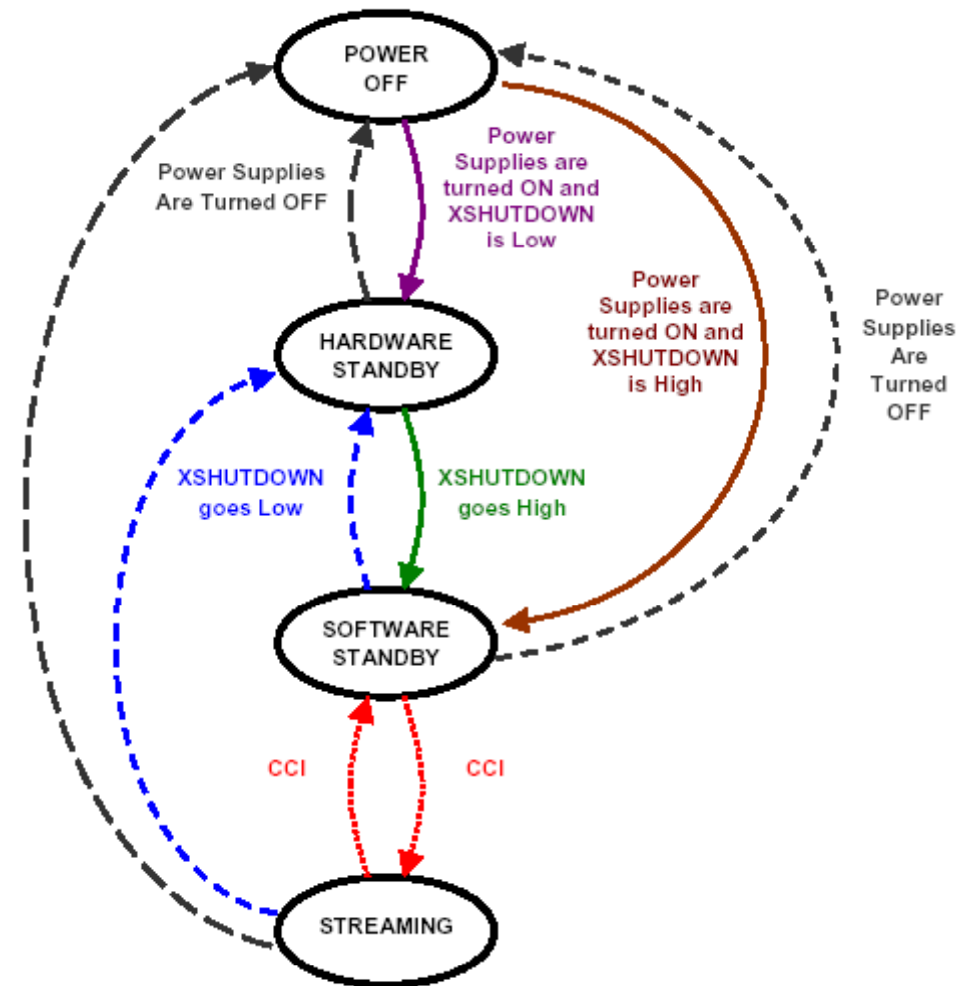
- CCI doesn't work.
- The Registers have default setting values.

SW standby

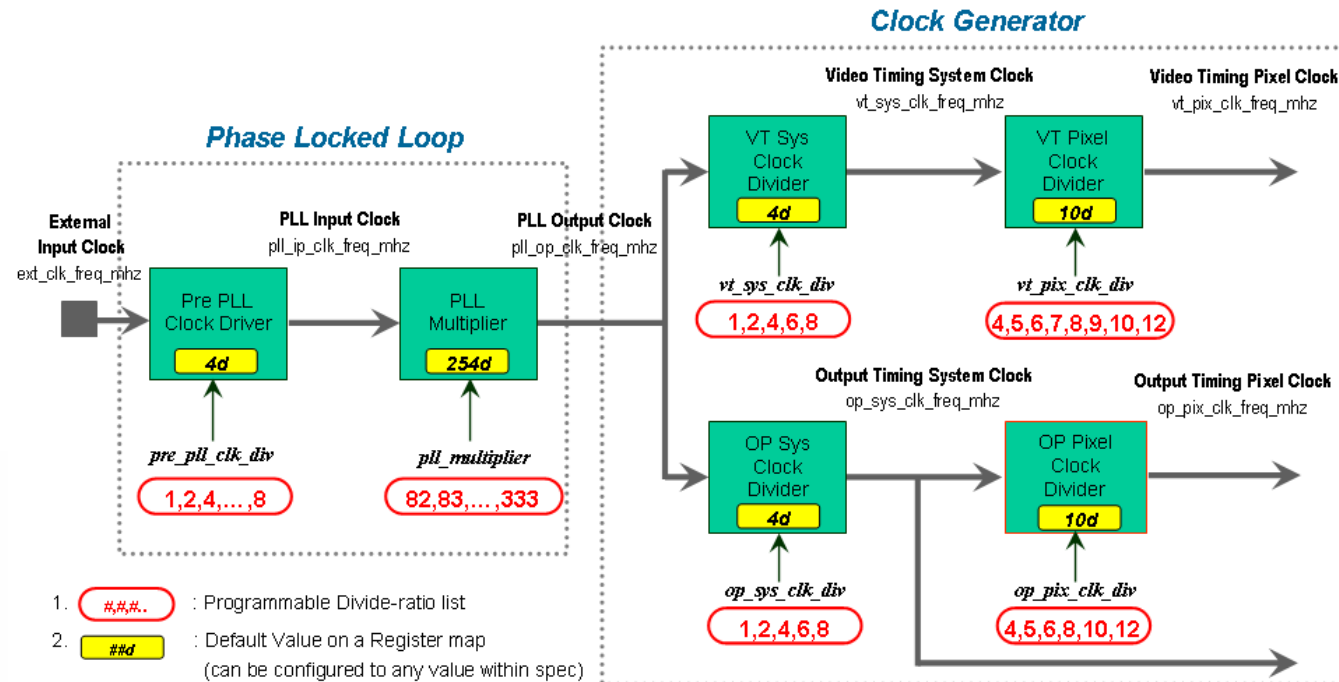
- Addr<0x0100h> [0] is 0b.
- The Registers can be controlled CCI.

Streaming ON (=operation mode)

- Addr<0x0100h> [0] is 1b.
- Output is activated.



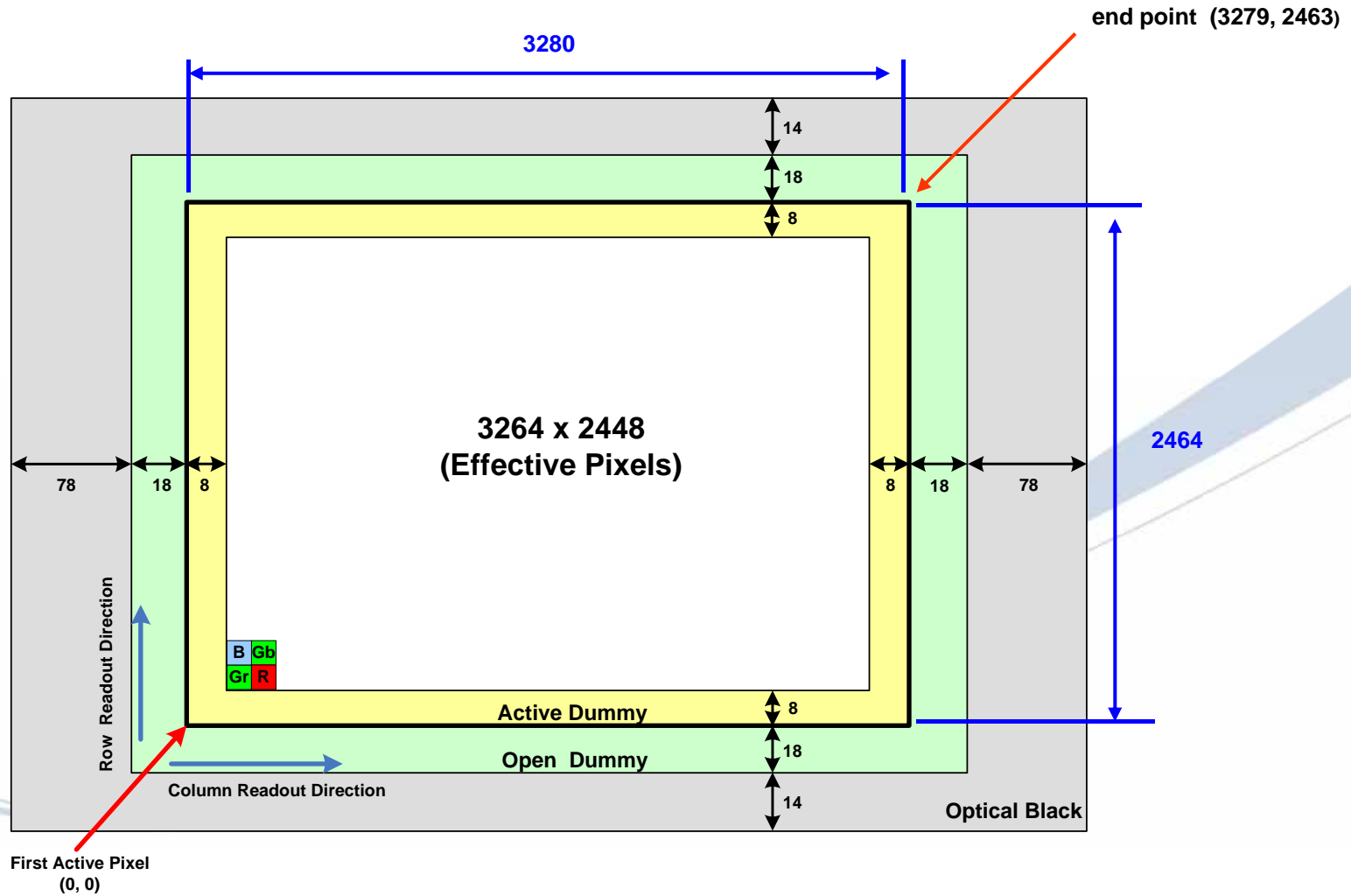
PLL setting : clock tree structure



$pll_ip_clk_freq_mhz = ext_clk_freq_mhz / pre_pll_clk_div$ ($pll_ip_clk_freq_mhz$: 3 MHz ~ 6 MHz)
 $pll_op_clk_freq_mhz = pll_ip_clk_freq_mhz * pll_multiplier$ ($pll_op_clk_freq_mhz$: 490 MHz ~ 1000 MHz)
 $vt_sys_clk_freq_mhz = pll_op_clk_freq_mhz / vt_sys_clk_div$
 $vt_pix_clk_freq_mhz = pll_op_clk_freq_mhz / (vt_sys_clk_div * vt_pix_clk_div)$ (max. freq. : 194MHz)
 $op_sys_clk_freq_mhz = pll_op_clk_freq_mhz / op_sys_clk_div$
 $op_pix_clk_freq_mhz = pll_op_clk_freq_mhz / (op_sys_clk_div * op_pix_clk_div)$ (max. freq. : 194MHz)

Pixel array

(Top view on chip. Displayed image will be flipped.)



Integration time

$$\text{Integration time} = \frac{(\text{line_length_pck} \times \text{coarse_integration_time}) + \text{fine_integration_time}}{\text{PCLK}}$$

	Fine_integration_time	Coarse_integration_time
Minimum shutter value	0d	3d (0x0003)
Maximum shutter value	Line length pck	Frame length lines – 4d

Ex) The minimum shutter (@ full size, 1300Mbps) = $((3470 \times 3) + 0) / (130 \times 10^6)$
= 0.080[ms]

The maximum shutter (@ full size, 1300Mbps) = $((3470 \times 2476) + 3470) / (130 \times 10^6)$
= 66 [ms]

* It can be changed as sensor MSR setting changed.

Analog Gain

$$\text{Analog gain} = \text{Analog_gain_code}[15:0] / 32$$

- Analog gain is controlled by two registers.
(Address 0x0204h, 0x0205h)
- Address 0x0204h is MSB and 0x0205h is LSB.
- The value of analog gain x1 is 0x0020h.
(**Using the value under 0x0020h is not allowed.**)
- Max gain is 31 times, but the sensor guarantees Linearity by 16 times.

Addr 0x0204h	Addr 0x0205h	Analog gain
0x00	0x20	x 1
0x00	0x40	x 2
0x00	0x80	x 4
0x01	0x00	x 8
0x02	0x00	x 16
0x03	0xE0	x 31

Sub-sampling (1)

Sub-sampling control register

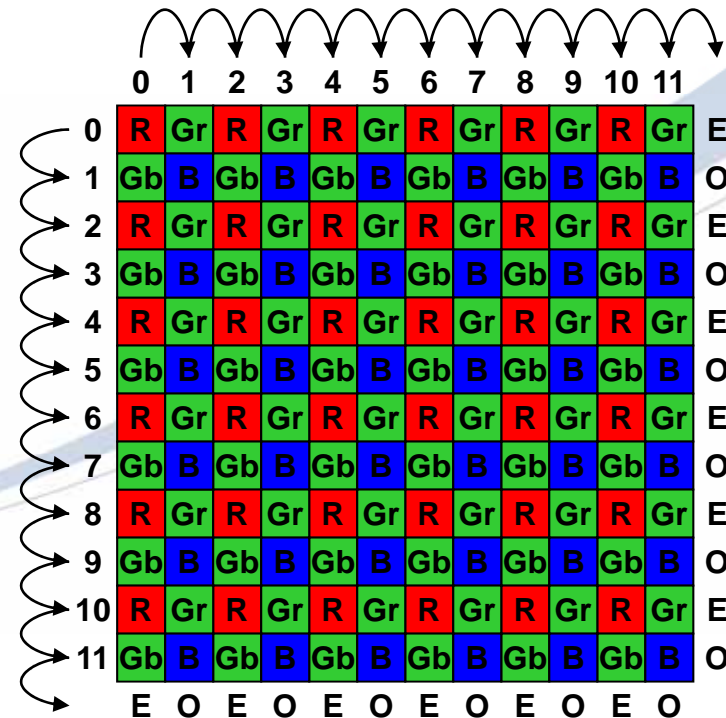
H_EVEN_INC : Increment for horizontal even pixels in the readout order
H_ODD_INC : Increment for horizontal odd pixels in the readout order
V_EVEN_INC : Increment for vertical even pixels in the readout order
V_ODD_INC : Increment for vertical odd pixels in the readout order

Normal readout register setting

FRAME_H_WIDTH : fixed frame rate **FRAME_V_DEPTH** : fixed frame rate
H_ADDR_START : 0 **H_ADDR_END** : 3279
V_ADDR_START : 0 **V_ADDR_END** : 2463

Normal readout increment register

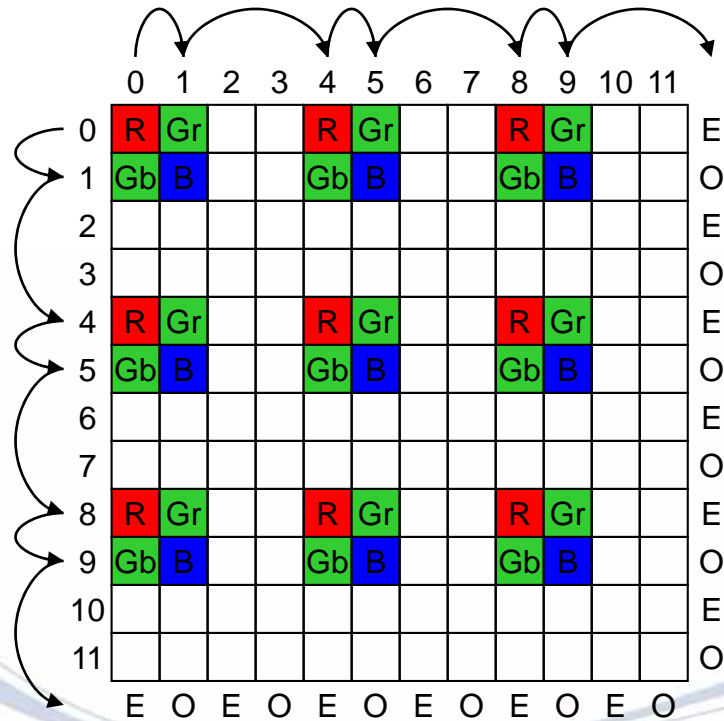
H_EVEN_INC : 1
H_ODD_INC : 1
V_EVEN_INC : 1
V_ODD_INC : 1



Sub-sampling (2)

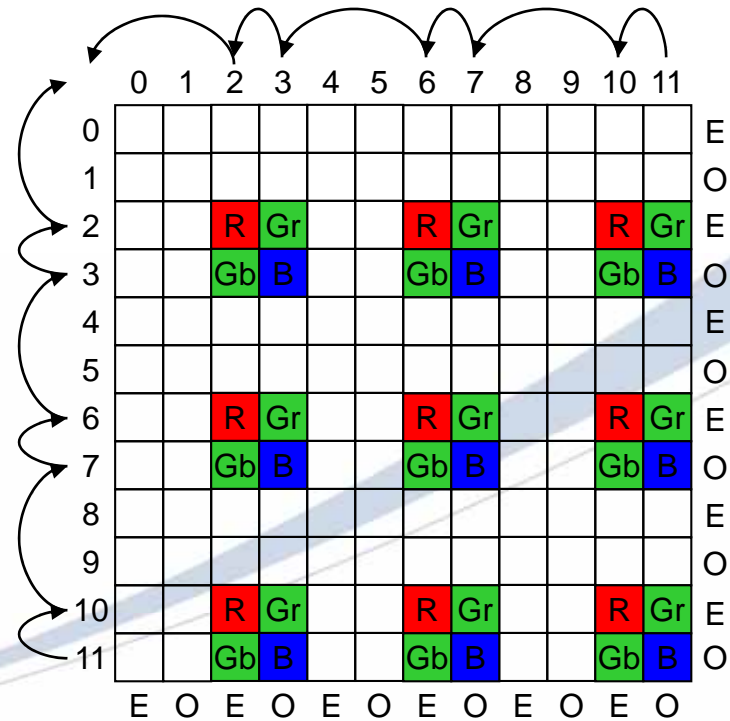
Normal H/2 x V/2 sub-sampling

H_EVEN_INC : 1,
 H_ODD_INC : 3,
 V_EVEN_INC : 1,
 V_ODD_INC : 3



V-flip & H-mirror H/2 x V/2 sub-sampling

H_EVEN_INC : 1,
 H_ODD_INC : 3,
 V_EVEN_INC : 1,
 V_ODD_INC : 3



Binning mode

By programming the x and y odd and even increment register (x_even_inc, x_odd_inc, y_even_inc, y_odd_inc). the sensor can be configured to readout sub-sampled pixel data. Only 1/2 H-binning is available and X-directional sub-sampling is not permitted at one time. In this case some register should be controlled as below.

REGISTER NAME	MNEMONIC	CODING	COMMENT
0X300E	H_bin_EN	[2]	0 : DISABLE, 1 : ENABLE
	Reserved	[1]	Reserved
	AVG_mode	[0]	0 : DISABLE, 1 : ENABLE
0x301D	V_bin_EN	[7]	0 : DISABLE, 1 : ENABLE
0x3085	H_wb_bypass	[0]	0 : ENABLE , 1 : DISABLE

Example : 2x2 binning setting

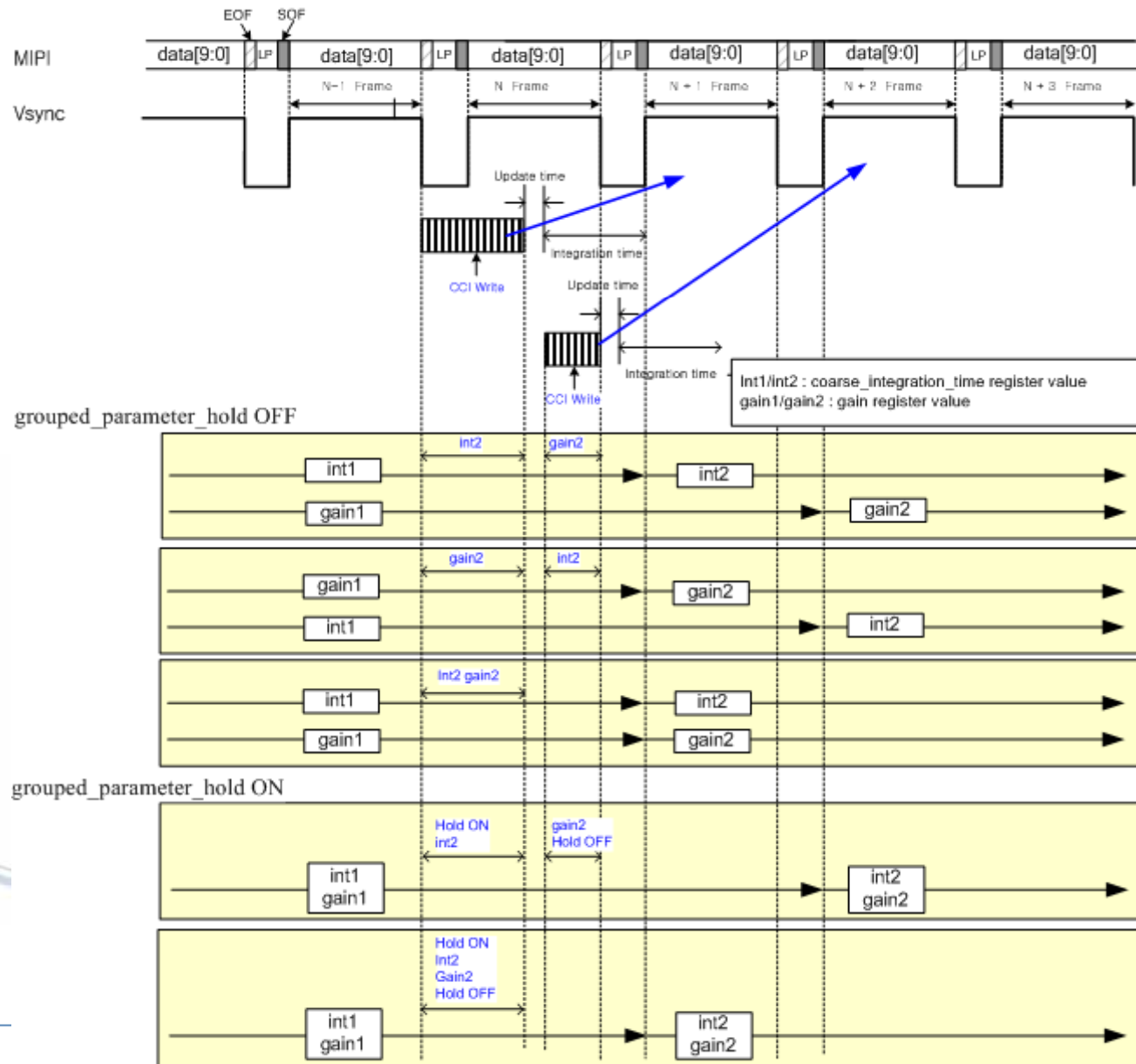
Address	Setting	Description
0x0380 0x0381	0x0001	x_even_inc
0x0382 0x0383	0x0001	x_odd_inc
0x0384 0x0385	0x0001	y_even_inc
0x0386 0x0387	0x0003	y_odd_inc
0x300E	0xED	Binning mode
0x3085	0x00	Binning mode
0x301D	0x81	Binning mode

Output size on each resolution

- 3H1 sensor do NOT support a Scaler function, so B/E should make a size which they want.

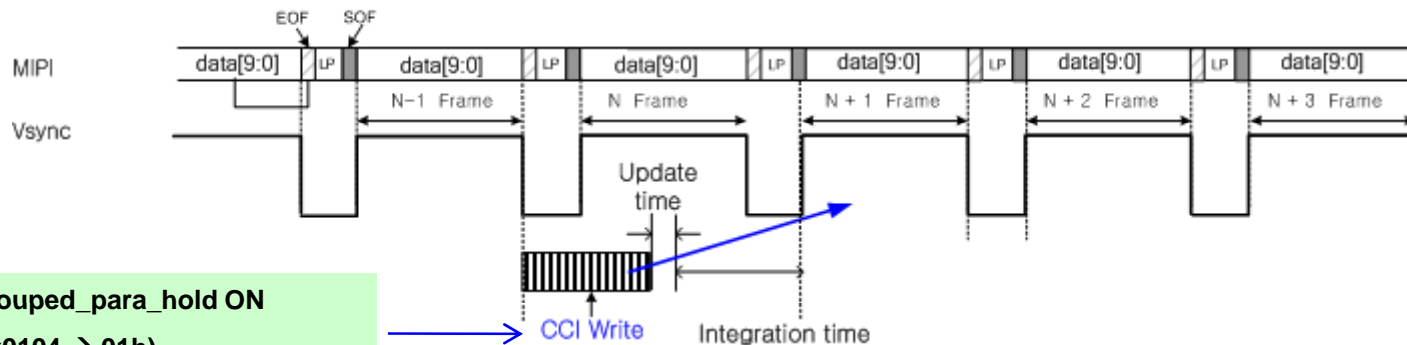
Resolution	Sensor output size	B/E scaler function supporting	Frame rate MIPI 2lane @ 970Mbps per lane
Full size	3280 x 2464	X	22fps
Full HD	3280x 1848	O	30fps
HD (Binning mode)	1640 x 916	O	60fps
Preview (Binning mode)	1640 x 1232	O	45fps
QVGA (Binning mode)	1640 x 308	O	172fps

Update sequence of shutter and analog gain



Register update time

- If you use “Grouped_para_hold” register (Addr. 0x0104), you should set “Grouped_para_hold” off (0x0104 → 0x00) on below “CCI write” time.

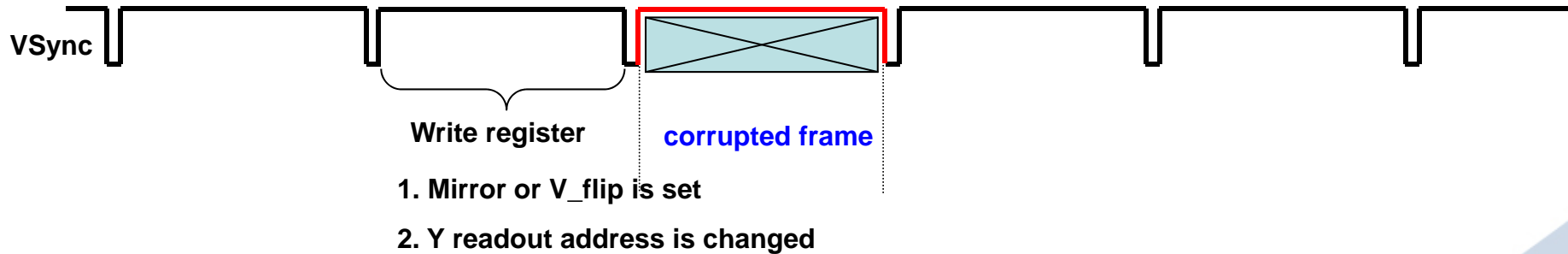


- 1> Grouped_para_hold ON (0x0104 → 01h)
- 2> Write shutter1
- 3> Write analog gain1
- 4> Grouped_para_hold OFF (0x0104 → 00h)

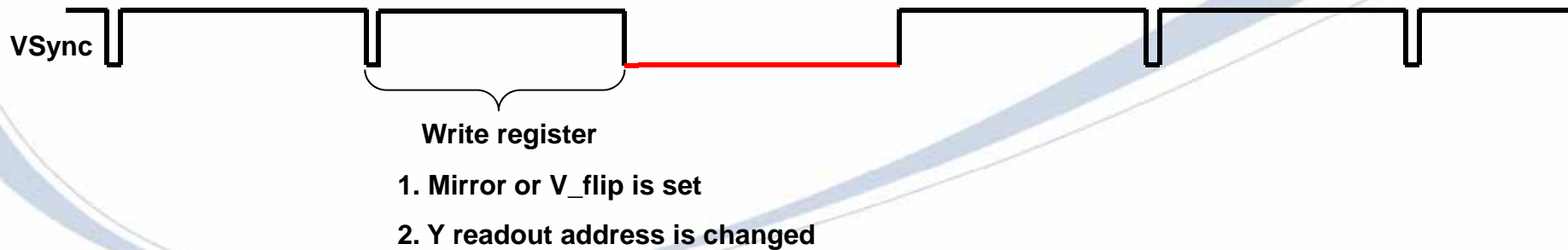
- CCI write time : $\text{MIN}(A, B) \times \text{line_length_pck} \times 1 / \text{vt_pix_clk_freq_mhz}$
 $A : \text{frame_length_lines (N frame)} - \text{coarse_integration_time (N frame)} - 2d$
 $B : \text{frame_length_lines (N frame)} - \text{coarse_integration_time (N+1 frame)} - 2d$
- Update time : $2d \times \text{line_length_pck} \times 1 / \text{vt_pix_clk_freq_mhz}$

Register update exception : Mirror or V-flip

Corrupted frame could be happened when Mirror or V-flip is set or Y_readout_address is changed



If mask corrupted frame (address 0x0105) is set to '0x01' before Mirror, V-flip or Y_readout_address is set, then the corrupted frame can be masking



* Y readout address : y_addr_start, y_addr_end, y_even_inc, y_odd_inc

Recommended mode change

* Recommended capture frame is 2nd frame after streaming on

