



DATA SHEET

S5K3H1GX(EVT3)

1/3.2" 8M CMOS Image Sensor Supporting SMIA 1.0

**March 2010
Revision 3.01**

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Samsung Electronics Co., Ltd.
San #24 Nongseo-Dong, Giheung-Gu
Yongin-City, Gyeonggi-Do, Korea
C.P.O. Box #37, Suwon 446-711

TEL: (82)-(31)-209-8302

FAX: (82)-(31)-209-8309

Home Page: <http://www.samsung.com/globak/business/semiconductor/index.html>

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		Table11 Page 43. ccp_data_format register is changed at 11.3 section Page 44. SEL_CCP register name and description are changed at 11.5 section Page 56. Analogue Gain Capability changed : 1 → 0	
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1 OVERVIEW

The S5K3H1GX is a highly integrated 8-Mega pixels camera chip which includes CMOS image sensor (CIS) and CSI-2 -compliant image data interface. It is fabricated by SAMSUNG CMOS image sensor process developed for imaging application to realize high-efficiency and low-power photo sensor. The sensor consists of 3264 x 2448(3280 x 2464 including border pixels) active pixels which meet with 1/3.2 inch optical format. The CIS has on-chip 10-bit/12-bit(12-bit is for test) ADC arrays to digitize the pixel output and also on-chip Correlated Double Sampling (CDS) function to reduce Fixed Pattern Noise (FPN) drastically. It incorporates on-chip camera functions such as data formatting, image compression, shading correction and serial transmission using Sub-LVDS. It is programmable through a CCI serial interface. The S5K3H1GX is suitable for low power camera module with 2.8V/1.8V power supply.

2 FEATURES

- SMIA 1.0 compliant (profile 0)
- Optical size: 1/3.2 inch
- Pixel size: 1.4 x 1.4 μm
- Active Pixels : 3264 (H) x 2448 (V)
- Line progressive read out
- Vertical and horizontal flip mode
- Continuous frame capture mode
- Sub-sampled readout : 1/2 ~ 1/8
- Output format: RAW 10-Bit and 8-Bit mode using DPCM/PCM compression,
- RAW Bayer 8/10/12-bit (10bit is default, 12bit is for test) parallel and CSI-2
- Max. frame rate: 15fps (RAW10 at CSI-2, 1300Mbps), 11fps (at parallel 97Mbps)
- Digital gain control (X1~X8, 1/256 step)
- Color / Lens shading correction
- Built-in test pattern generation
- Standby mode for power saving
- CCI (I²C-compatible) bus control interface
- Operating temperature: -30°C to +70°C
- Supply core voltage: 2.8V for analog / 1.8V for digital
- Internal voltage regulator for 1.5V generation
- Internal PLL for high speed clock generation
- High speed Sub-LVDS data/clock or data/strobe signaling
- Support Mechanical shutter
- Support Full HD, HD by cropping and binning



3 BLOCK DIAGRAM

The S5K3H1GX is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) to generate all internal clocks from a single master input clock running between 6 MHz and 64 MHz. The maximum pixel rate is 1940 Mbps at CSI-2 2-lane, corresponding to the pixel clock rate of 194 MHz at CSI-2 RAW10.

The block diagram of the sensor is shown in Figure 1.

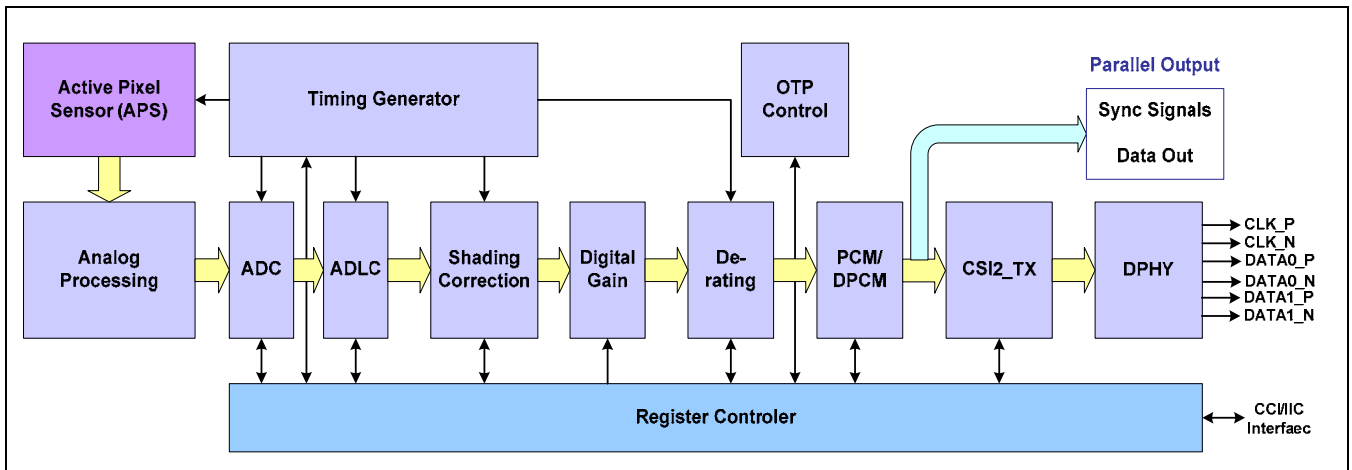


Figure 1. Function Block Diagram

The image sensor has an on-chip ADC. Column parallel ADC scheme is used for low power analog processing.

The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action and some fixed pattern noise caused by the in-pixel amplifier offset deviation. To eliminate those noise components, a Correlated Double Sampling (CDS) circuit is used before converting to digital.

The output from the ADC is a 10-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain which provides further data path corrections and applies digital gain. A shading correction block is used to compensate for color/brightness shading introduced by the lens or CRA curve mismatch. Additional functionality is provided to support the SMIA standard. This includes a PCM/DPCM compressor, and a serializer.

The sensor contains a set of control and status registers that can be used to control many aspects of the sensor behavior including the frame size, exposure, and gain setting. These registers can be accessed through a CCI interface.

3.1 DEVICE OPERATING MODES

The Sensor module has 4 operating modes (Table 1). Moving from one mode to another is achieved by issuing the appropriate mode command via the CCI serial control interface, the XSHUTDOWN signal changing state and the power supplies. By default, S5K3H1GX powers up as a SMIA-compatible sensor with the CSI-2 serial data interface enabled. Figure 2 defines the valid mode changes for the sensor module.

Table 1 : Operating Mode Summary

Power State	Description
Power-off	Power supplies are turned off.
Hardware Standby	No communication with the sensor is possible.
Software Standby	CCI communication with sensor is possible.
Streaming	The sensor module is fully powered and is streaming image data on the CSI-2 bus.

The activation of a sensor can be by **mode_select** register. The parallel data interface is disabled by default at power up and reset. It can be enabled by PIN settings: {TST3,TST2,TST1,TST0} = {0,0,0,1}

Name	Address	Bits	Description
mode_select	0x0100	[0]	Mode Select 0 – Software Standby, 1- Streaming

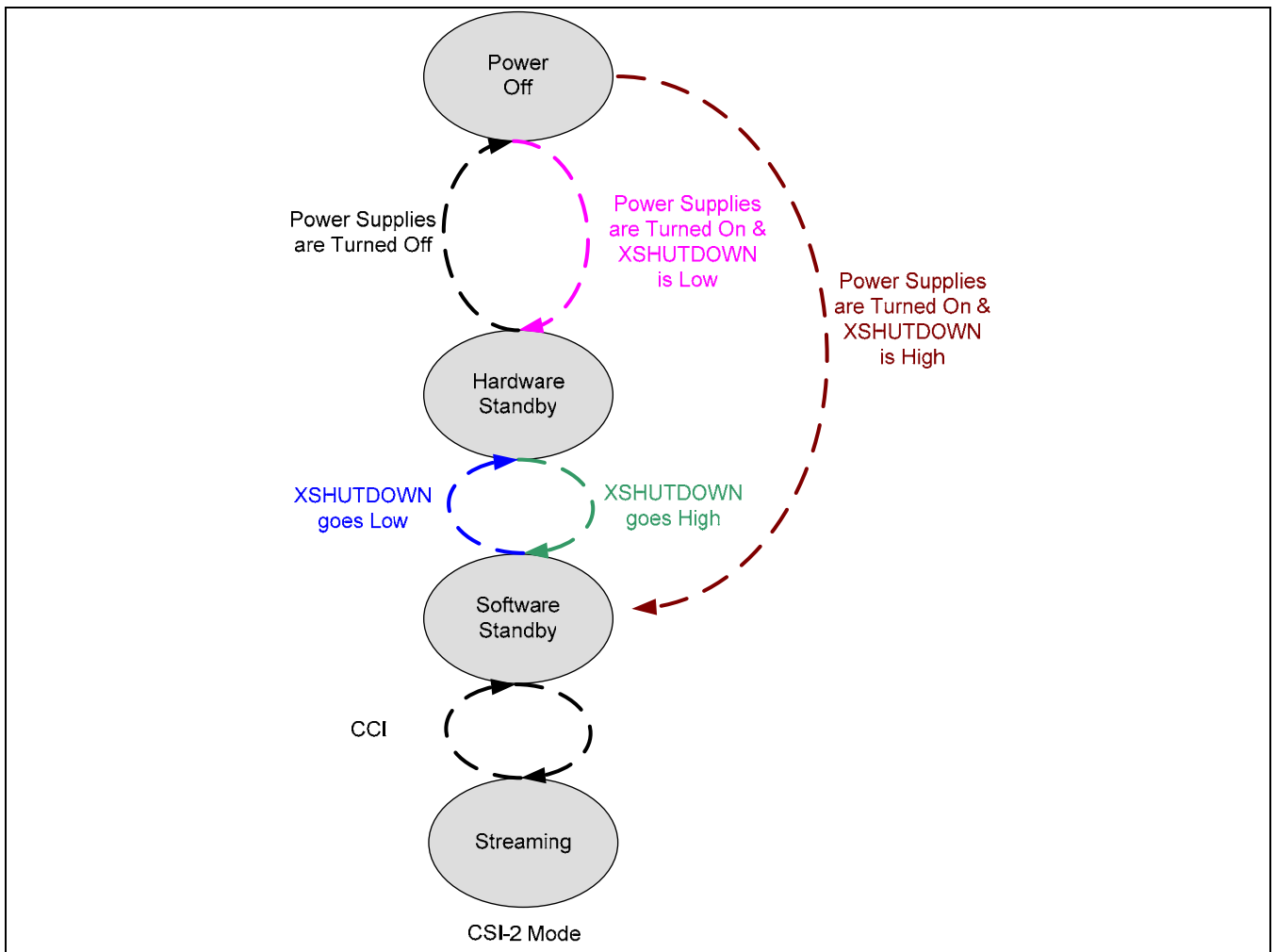


Figure 2. System State Diagram

4 PAD CONFIGURATION

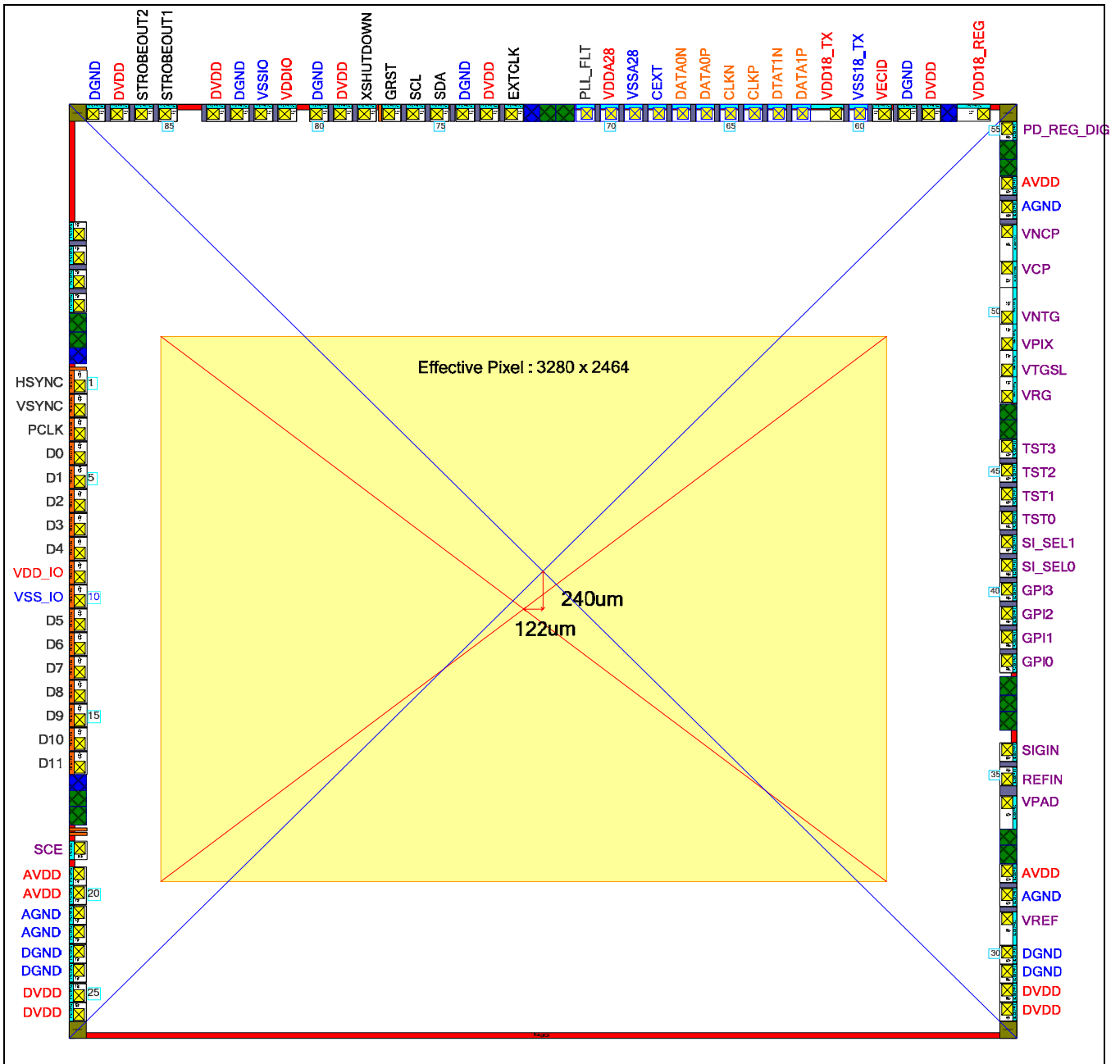


Figure 3. Pad Configuration

5 PAD DESCRIPTION

Table 2 : Pad Description

PAD#	Name	Description	PAD#	Name	Description
1	HSYNC	Horizontal SYNC	47	VRG	Analog Test
2	VSYNC	Vertical SYNC	48	VTGSL	Analog Test
3	PCLK	Pixel Output Clock	49	VPIX	External Capacitor --> 0.1uF
4	D0	Parallel Output Data 0	50	VNTG	Analog Test
5	D1	Parallel Output Data 1	51	VCP	External Capacitor --> 0.1uF
6	D2	Parallel Output Data 2	52	VNCP	Analog Test
7	D3	Parallel Output Data 3	53	AGND	Analog Ground
8	D4	Parallel Output Data 4	54	AVDD	2.8V Analog Power
9	VDD_IO	1.8~2.8V I/O Power	55	PD_REG_DIG	Regulator Power-Down @ HIGH
10	VSS_IO	I/O Ground	56	VDD18_REG	1.8V Regulator Input Powere (VDIG)
11	D5	Parallel Output Data 5	57	DVDD	1.5V Digital Power --> 0.4uF Capacitor
12	D6	Parallel Output Data 6	58	DGND	Digital Ground
13	D7	Parallel Output Data 7	59	VECID	Efuse Write Power
14	D8	Parallel Output Data 8	60	VSS18_TX	Digital Ground
15	D9	Parallel Output Data 9	61	VDD18_TX	1.8V I/O Power
16	D10	Parallel Output Data 10	62	DATA1P	Serial Data Output 1 - positive
17	D11	Parallel Output Data 11	63	DATA1N	Serial Data Output 1 - negative
18	SCE	External Clock Enable @ High	64	CLKP	Serial Clock Output - positive
19	AVDD	2.8V Analog Power	65	CLKN	Serial Clock Output - negative
20	AVDD	2.8V Analog Power	66	DATA0P	Serial Data Output 0 - positive
21	AGND	Analog Ground	67	DATA0N	Serial Data Output 0 - negative
22	AGND	Analog Ground	68	CEXT	External Capacitor --> 0.1uF
23	DGND	Digital Ground	69	VSSA28	Digital Ground
24	DGND	Digital Ground	70	VDDA28	2.8V Analog Power
25	DVDD	1.5V Digital Power - connected to #57	71	PLL_FLT	Analog Test
26	DVDD	1.5V Digital Power - connected to #57	72	EXTCLK	External Input Clock
27	DVDD	1.5V Digital Power - connected to #57	73	DVDD	1.5V Digital Power - connected to #57
28	DVDD	1.5V Digital Power - connected to #57	74	DGND	Digital Ground
29	DGND	Digital Ground	75	SDA	CCI Data Signal
30	DGND	Digital Ground	76	SCL	CCI Clock Signal
31	VREF	Analog Test	77	GRST	Global Reset(Active HIGH)
32	AGND	Analog Ground	78	XSHUTDOWN	Hardware Reset(Active LOW)
33	AVDD	2.8V Analog Power	79	DVDD	1.5V Digital Power - connected to #57
34	VPAD	Analog Test	80	DGND	Digital Ground
35	REFIN	Analog Test	81	VDDIO	1.8~2.8V I/O Power
36	SIGIN	Analog Test	82	VSSIO	I/O Ground
37	GPI0	GPI 0 for module revsion info.	83	DGND	Digital Ground
38	GPI1	GPI 1 for module revsion info.	84	DVDD	1.5V Digital Power - connected to #57
39	GPI2	GPI 2 for module revsion info.	85	STROBEOUT1	Strobe Out 1
40	GPI3	GPI 3 for module revsion info.	86	STROBEOUT2	Strobe Out 2
41	SI_SEL0	Slave_ID Selection 0	87	DVDD	1.5V Digital Power - connected to #57
42	SI_SEL1	Slave_ID Selection 1	88	DGND	Digital Ground
43	TST0	Test Mode Selection 0	89	DVDD	Dummy 1.5V Digital Power
44	TST1	Test Mode Selection 1	90	DVDD	Dummy 1.5V Digital Power
45	TST2	Test Mode Selection 2	91	DGND	Dummy Digital Ground
46	TST3	Test Mode Selection 3	92	DGND	Dummy Digital Ground



6 PIXEL ARRAY INFORMATION

(TOP VIEW ON CHIP. DISPLAYED IMAGE WILL BE FLIPPED.)

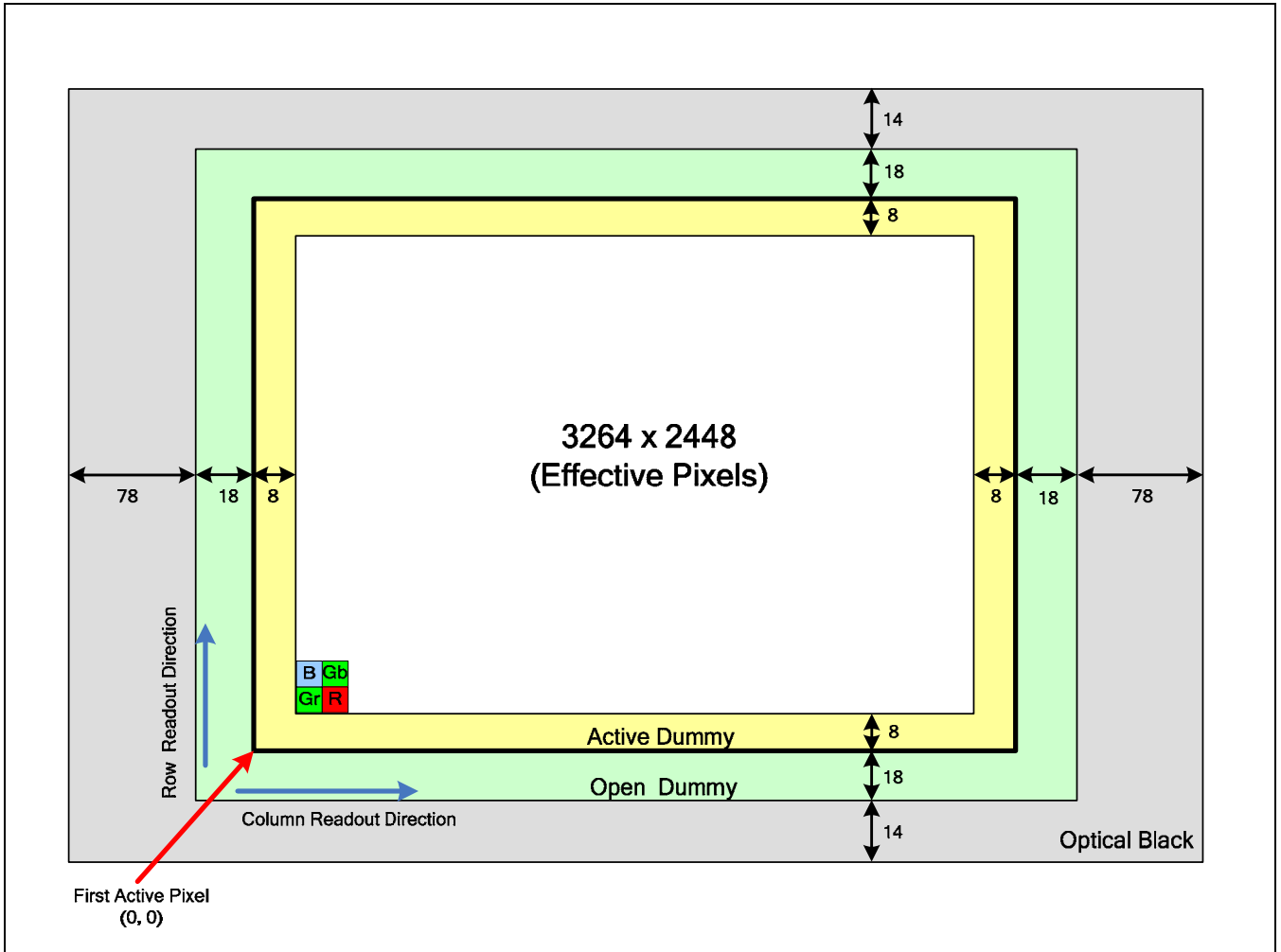


Figure 4. Pixel Array Information

7 VIDEO TIMING

7.1 OVERVIEW

The output image size is a function of the size of the addressed region of the pixel array and the sub-sampling factor programmed. Figure 5 shows the video timing overview.

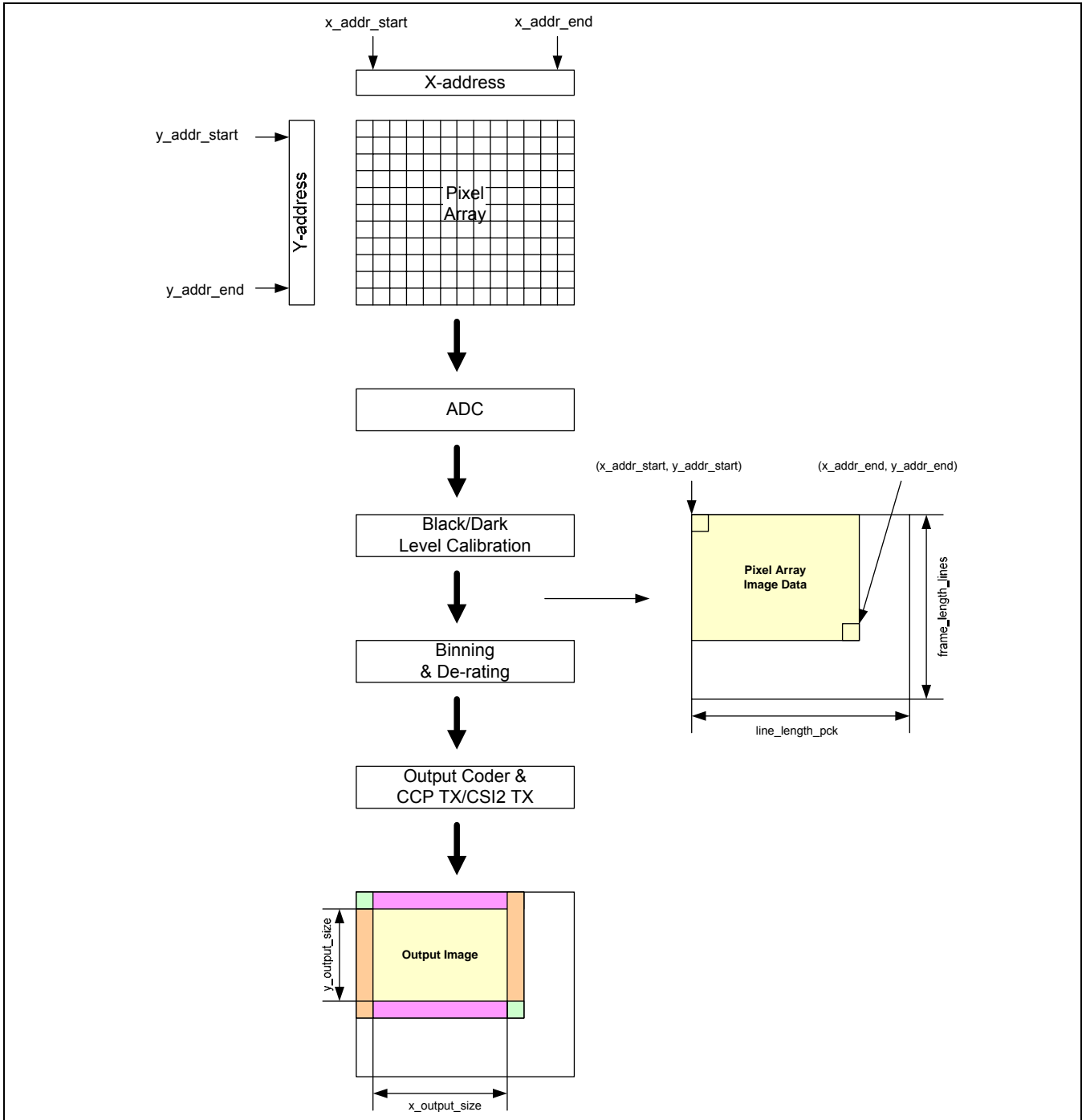


Figure 5. Video Timing Overview

7.2 IMAGE READOUT

7.2.1 Pixel Array Addresses

Addressable pixel array is defined as the pixel address range to be read. The Addressable pixel array can be assigned anywhere on the pixel array. The addressed region of the pixel array is controlled by `x_addr_start`, `y_addr_start`, `x_addr_end` and `y_addr_end` register. Figure 6 refers to a pictorial representation of the Addressable pixel array on the Physical pixel array. The limits for the above parameters are given by the `x_addr_min`, `y_addr_min`, `x_addr_max`, `y_addr_max` register.

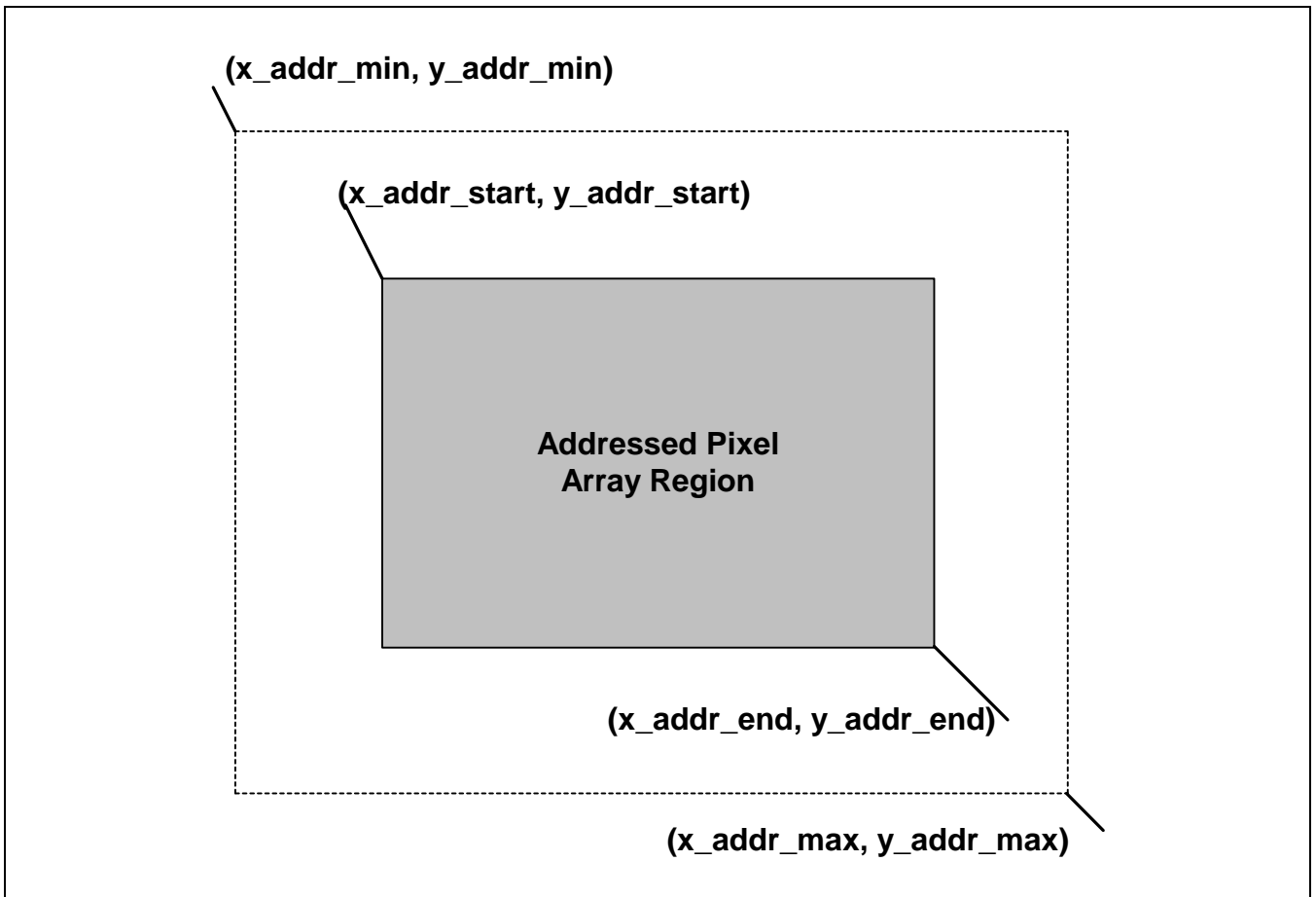


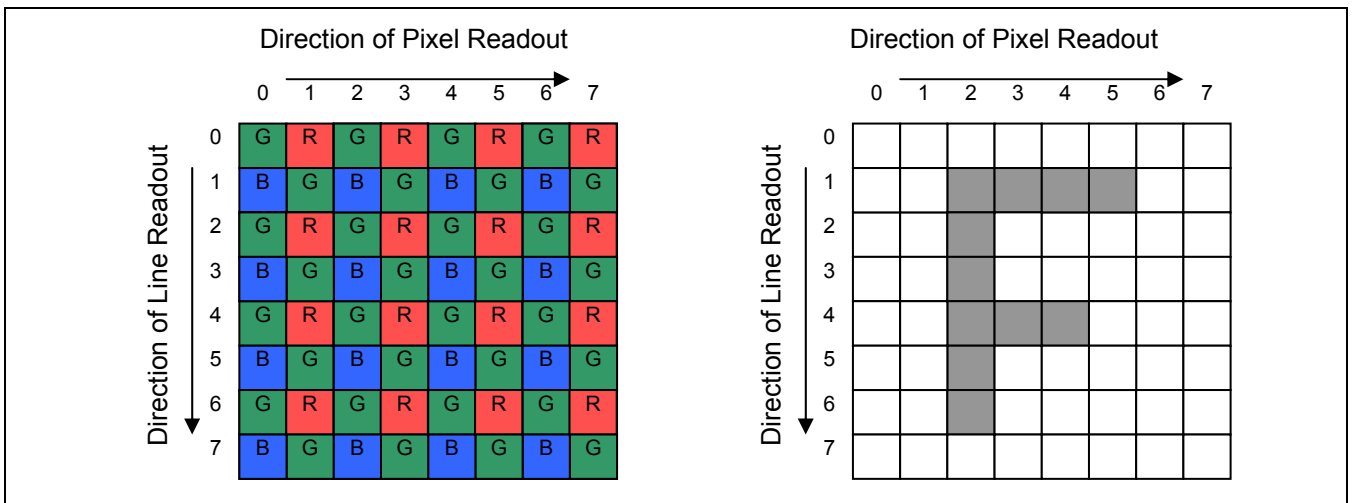
Figure 6. Addressable Pixel Array

7.2.2 Mirror/Flip

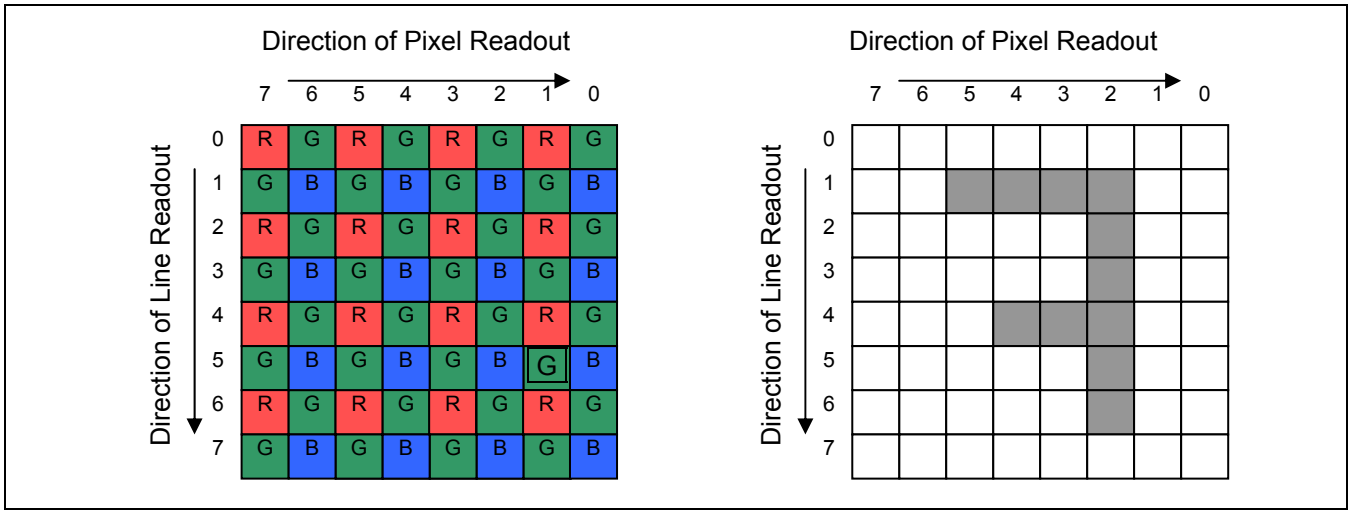
The pixel data are read out from left to right in horizontal direction and from top to bottom in vertical direction normally. By changing the mirror/flip mode, the read-out sequence can be reversed and the resulting image can be flipped like a mirror image. Pixel data are read out from right to left in horizontal mirror mode and from bottom to top in vertical flip mode. The horizontal mirror and the vertical flip mode can be programmed by image orientation register.

The sensor module support 4 possible pixel readout order

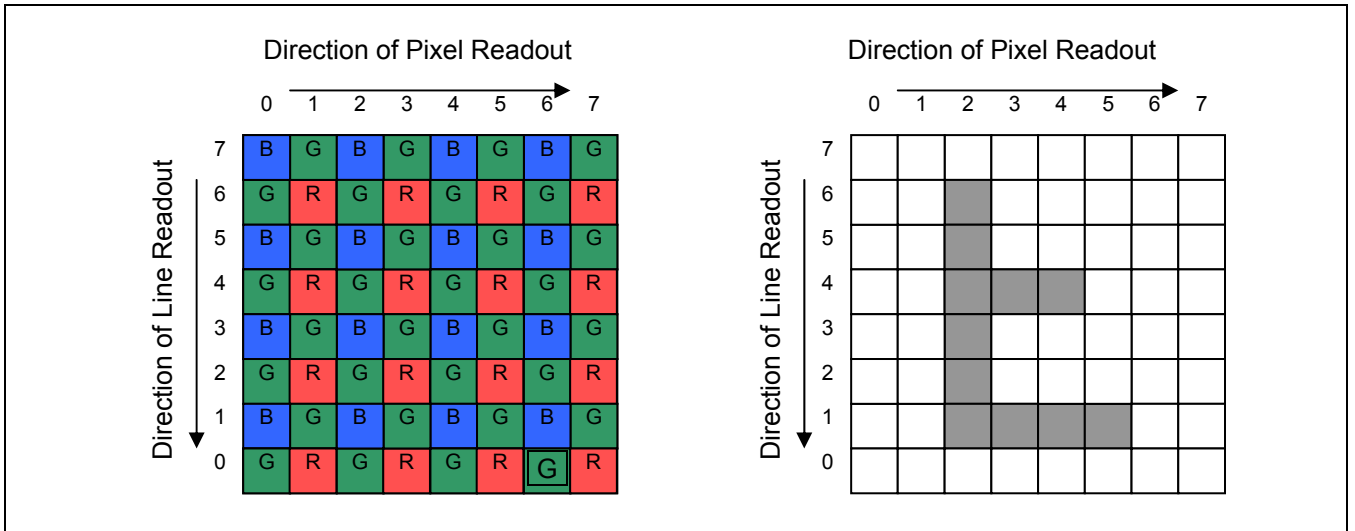
- 1) Standard readout
- 2) Horizontally mirrored readout
- 3) Vertical Flipped readout
- 4) Horizontally Mirrored and Vertically Flipped readout



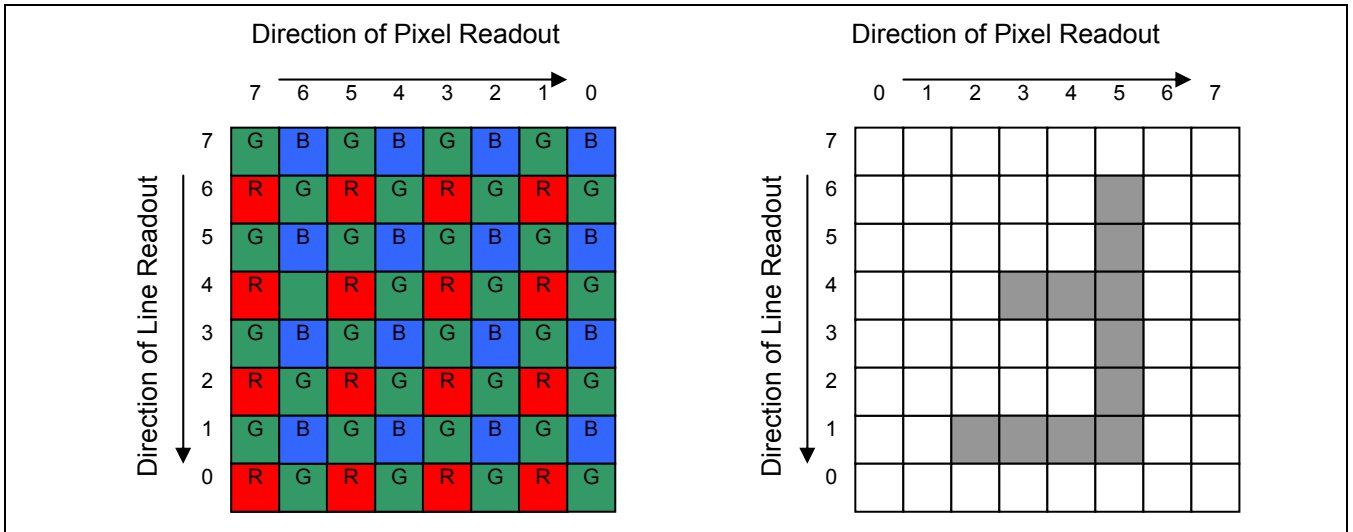
1) Standard Readout



2) Horizontally Mirrored Readout



3) Vertically Flipped Readout



3) Horizontally Mirrored and Vertically Flipped Readout

Figure 7. Mirror and Flip

7.2.3 Sub-Sampled Readout

By programming the x and y odd and even increment register (**x_even_inc**, **x_odd_inc**, **y_even_inc**, **y_odd_inc**). The sensor can be configured to readout sub-sampled pixel data.

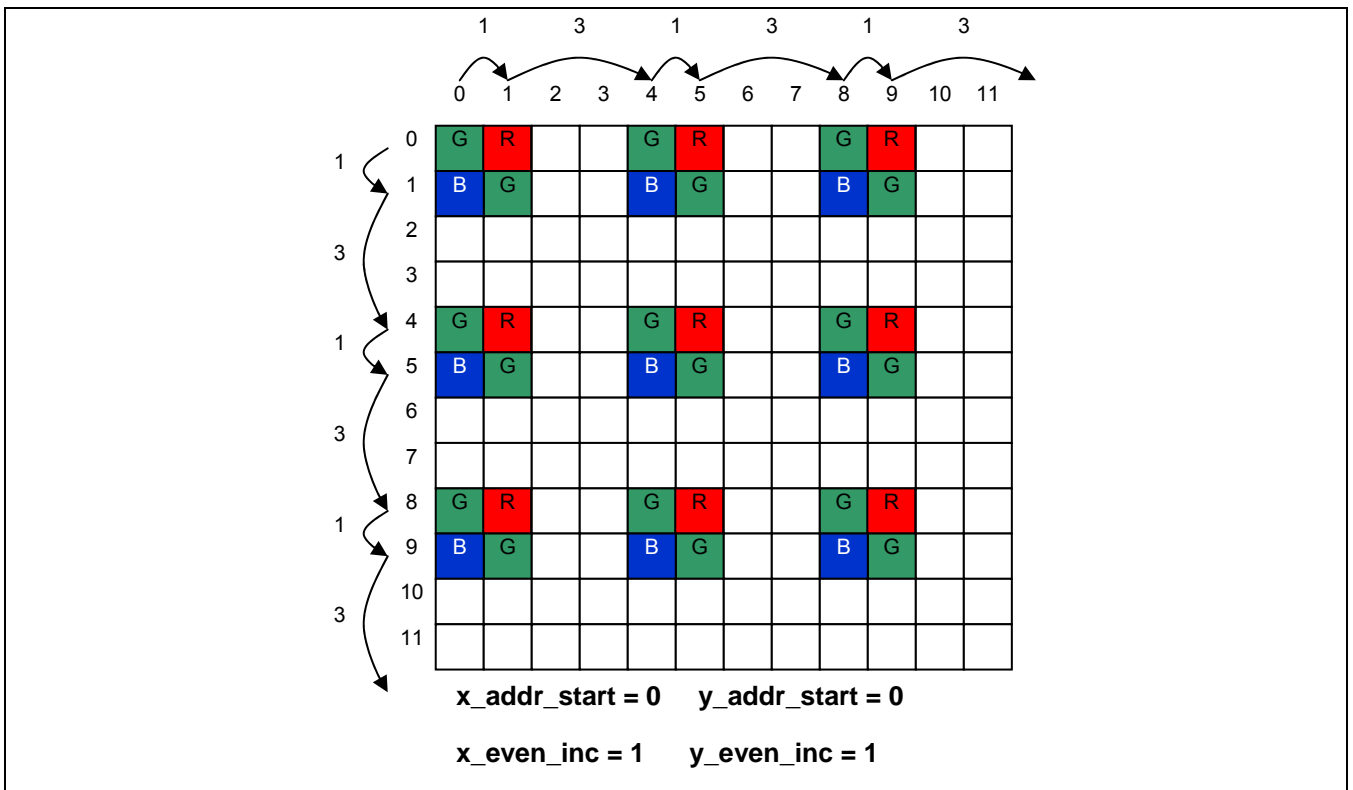


Figure 8. Sub-sampled Readout

7.2.4 Binning Readout

The binning function averages the adjacent two pixel data to one in both X and Y directions per channel. Figure 9 illustrates how the binning readout operates using below table values. At S5K3H1GX only 1/2 binning is available and it is not support sub-sampling readout during binning readout mode.

Index	Setting Value	Bits	Register Name	Description
0x0381	0x01	[7:0]	x_even_inc	Increment for even pixels in X direction
0x0383	0x01	[7:0]	x_odd_inc	Increment for odd pixels in X direction
0x0385	0x01	[7:0]	y_even_inc	Increment for even pixels in Y direction
0x0387	0x03	[7:0]	y_odd_inc	Increment for odd pixels in Y direction
0x300E	1b1	[2]	h_avg_en	Horizontal binning enable - 0 : disable, 1 : enable
	1'b1	[0]	avg_mode	0 : reserved , 1 : averaged binning
0x301D	1'b1	[7]	v_avg_en	Vertical binning enable -0 :disable, 1: enable
0x3085	1'b0	[0]	H-wb_bypass	Binning block enable - 0 : On, 1 : Bypass(default)

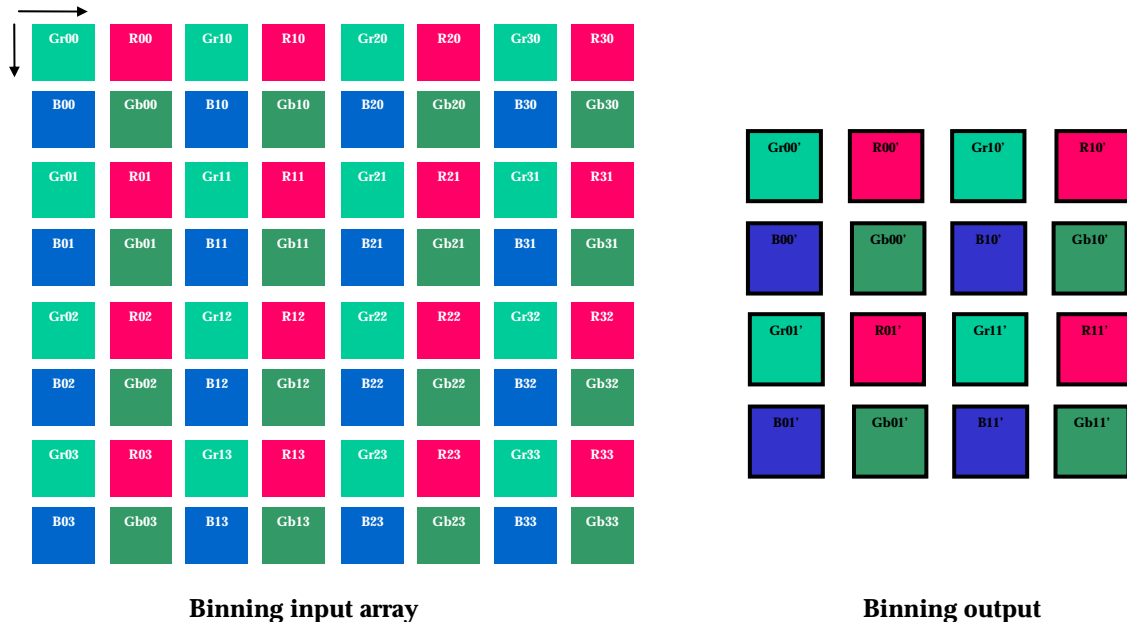


Figure 9. 1/2 Binning Readout

$$\begin{aligned}
 Gr00' &= (Gr00 + Gr10 + Gr01 + Gr11) / 4 & Gr10' &= (Gr20 + Gr30 + Gr21 + Gr31) / 4 \\
 Gr01' &= (Gr02 + Gr12 + Gr03 + Gr13) / 4 & Gr11' &= (Gr22 + Gr32 + Gr23 + Gr33) / 4
 \end{aligned}$$

* R, B, Gb pixels are generated same as Gr pixel

By using the binning function, sensor can be set to the max data rate as shown below.

Data Format	CSI-2 (2-lane)	
	8 M Full	1/2 binning
RAW10	15 fps 1300Mbps	30 fps 1300Mbps
RAW8	18 fps 1300Mbps	37.5 fps 1300Mbps

7.3 FRAME RATE CONTROL (VIRTUAL FRAME)

The line rate and the frame rate can be changed by varying the size of virtual frame. The virtual frame's width and depth are controlled by **line_length_pck** and **frame_length_lines** register. The frame rate can be calculated by the following equation:

$$\text{Frame rate} = 1 / (\text{line_length_pck} * \text{frame_length_lines}) * \text{vt_pix_clk_freq_mhz}$$

For S5K3H1GX, the minimum **line_length_pck** is 3470(decimal) and other parameters can be set appropriately according to the above equation.

7.3.1 Integration Time Control (Electronic Shutter Control)

The pixel integration time is controlled by shutter operation. In shutter operation, the amount of time, integration time, is determined by the column Step Integration Time Control Register (**fine_integration_time**) and line Step Integration Time Control Register (**coarse_integration_time**). The total integration time of sensor module can be calculated using the following formula.

$$\text{Total_integration_time} = \{(\text{coarse_integration_time} * \text{pixel_period_per_line}) + \text{fine_integration_time}\} * \text{pck_clk_period}$$

7.3.2 PLL and Clock Generator

S5K3H1GX contains a Phase-Locked Loop (PLL) and a clock generator, which generates all the necessary video timing and output pixel clocks from the external clock input. By setting the divide-ratio for Pre PLL Clock Divider (**pre_pll_clk_div**) and PLL Multiplier (**pll_multiplier**) appropriately, users can get necessary PLL output Clock (**pll_op_clk_freq_mhz**). The minimum and maximum limits for the output clock frequencies and divide-ratios of the various clock dividers are fully described and limited by the Parameter Limit Registers (Read Only) from 0x1100 to 0x1177 address. The PLL can handle any **ext_clk_freq_mhz** in the range of **6 MHz** to **64 MHz**, and synthesize **pll_op_clk_freq_mhz** between **490 MHz** and **1000 MHz**. For the proper PLL operation, **pll_ip_clk_freq_mhz** should be in the range of **3 MHz** to **6 MHz**. All PLL programming should be performed during software stand-by mode for the stable system operation.

The overall clock tree structure is shown in Figure 10, and there are user-controllable divide-ratios in the red box. All necessary frequencies are synthesized by the following equations.

$$\begin{aligned} \text{pll_ip_clk_freq_mhz} &= \text{ext_clk_freq_mhz} / \text{pre_pll_clk_div} \quad (\text{pll_ip_clk_freq_mhz: } 3 \text{ MHz} \sim 6 \text{ MHz}) \\ \text{pll_op_clk_freq_mhz} &= \text{pll_ip_clk_freq_mhz} * \text{pll_multiplier} \quad (\text{pll_op_clk_freq_mhz: } 490 \text{ MHz} \sim 1000 \text{ MHz}) \\ \text{vt_sys_clk_freq_mhz} &= \text{pll_op_clk_freq_mhz} / \text{vt_sys_clk_div} \\ \text{vt_pix_clk_freq_mhz} &= \text{pll_op_clk_freq_mhz} / (\text{vt_sys_clk_div} * \text{vt_pix_clk_div}) \quad (\text{max. freq.: } 194\text{MHz}) \\ \text{op_sys_clk_freq_mhz} &= \text{pll_op_clk_freq_mhz} / \text{op_sys_clk_div} \\ \text{op_pix_clk_freq_mhz} &= \text{pll_op_clk_freq_mhz} / (\text{op_sys_clk_div} * \text{op_pix_clk_div}) \quad (\text{max. freq. : } 194\text{MHz}) \end{aligned}$$

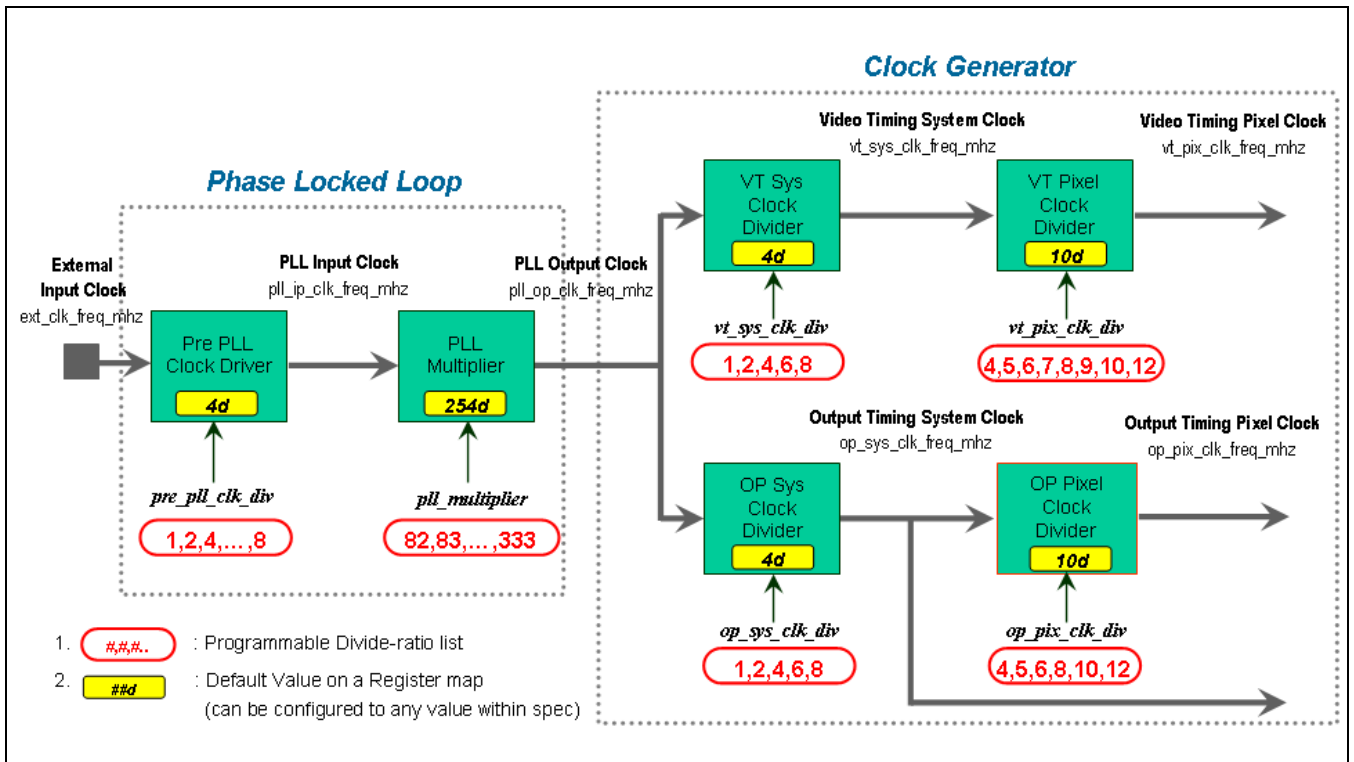


Figure 10. Clock Tree Structure

8 CONTROL INTERFACE

8.1 CAMERA CONTROL INTERFACE (CCI)

S5K3H1GX supports the Camera Control Interface (CCI), which is an I2C Fast-mode compatible interface for controlling the transmitter. S5K3H1GX always a slave in the CCI bus. CCI is capable of handling several slaves in the bus, but multi-master mode is not supported. Typically no other devices than receiver and transmitter are connected to the CCI bus. This makes a pure SW implementation possible.

Typically the CCI is separate from the system I2C bus, but I2C compatibility ensures that it is also possible to connect the transmitter to system I2C bus. CCI is a subset of I2C protocol including the minimum combination of obligatory features for I2C slave device specified in the I2C specification. Therefore transmitters complying with the CCI specification can also be connected to system I2C bus. However, it has to be taken care that the I2C masters do not try to utilize those I2C features, which are not supported in transmitters complying with the CCI specification. Each transmitter conformed to the CCI specification may have additional features implemented to support I2C.

8.1.1 Data transfer protocol

The data protocol is according to I2C standard specified in I2C specification.

8.1.2 Message Format

The S5K3H1GX CCI supports 16-bit index with 8-bit data with basic I2C standard protocol; START condition, slave address with read/write bit, acknowledge from slave, and STOP condition. In read operation, data byte comes from slave till negative ack is asserted from master. The device address for the sensor is 0010000 b.

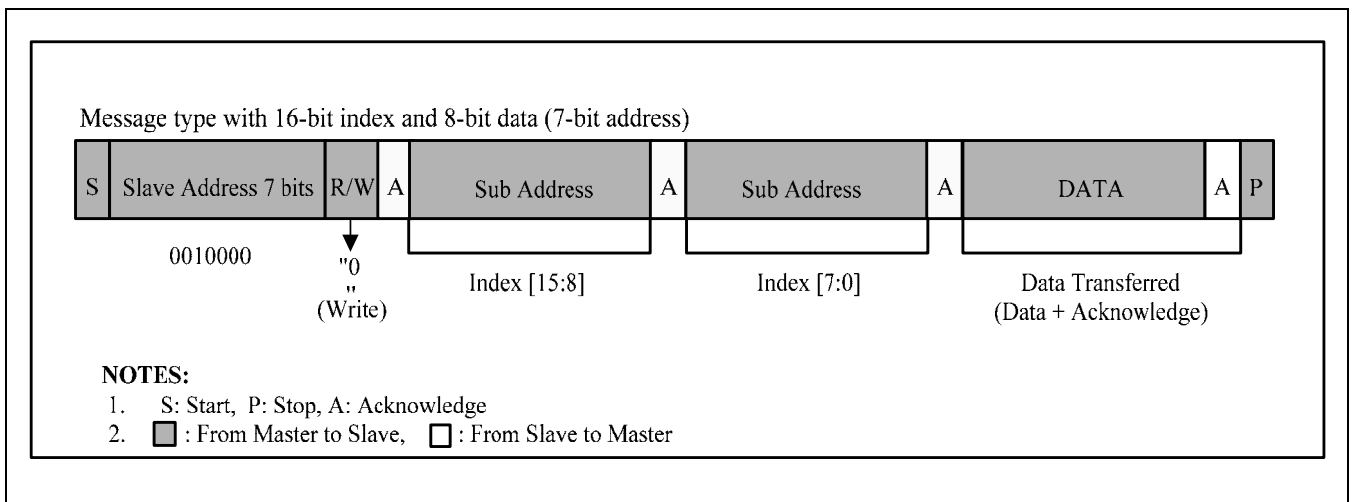


Figure 11. CCI Message Type

8.1.3 Read / Write Operation

The S5K3H1GX CCI interface must be able to support four different read operations and two different write operations; single read from random location, sequential read from random location, single read from current location, sequential read from current location, single write to random location and sequential write starting from random location. The read/write operations are presented in the followings. The 16bit index in the slave device has to be auto incremented after each read/write operation.

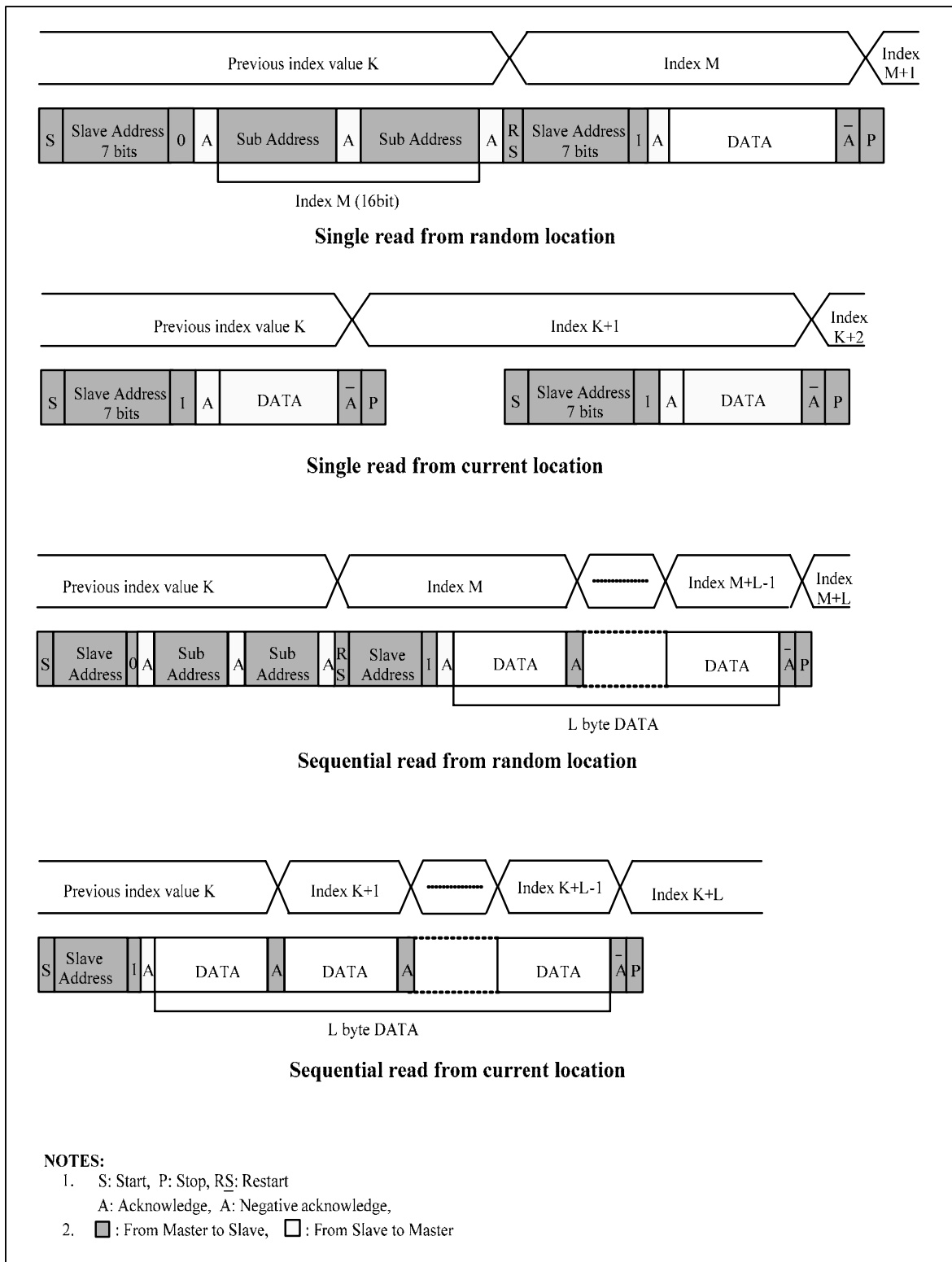


Figure 12. CCI Read Operation

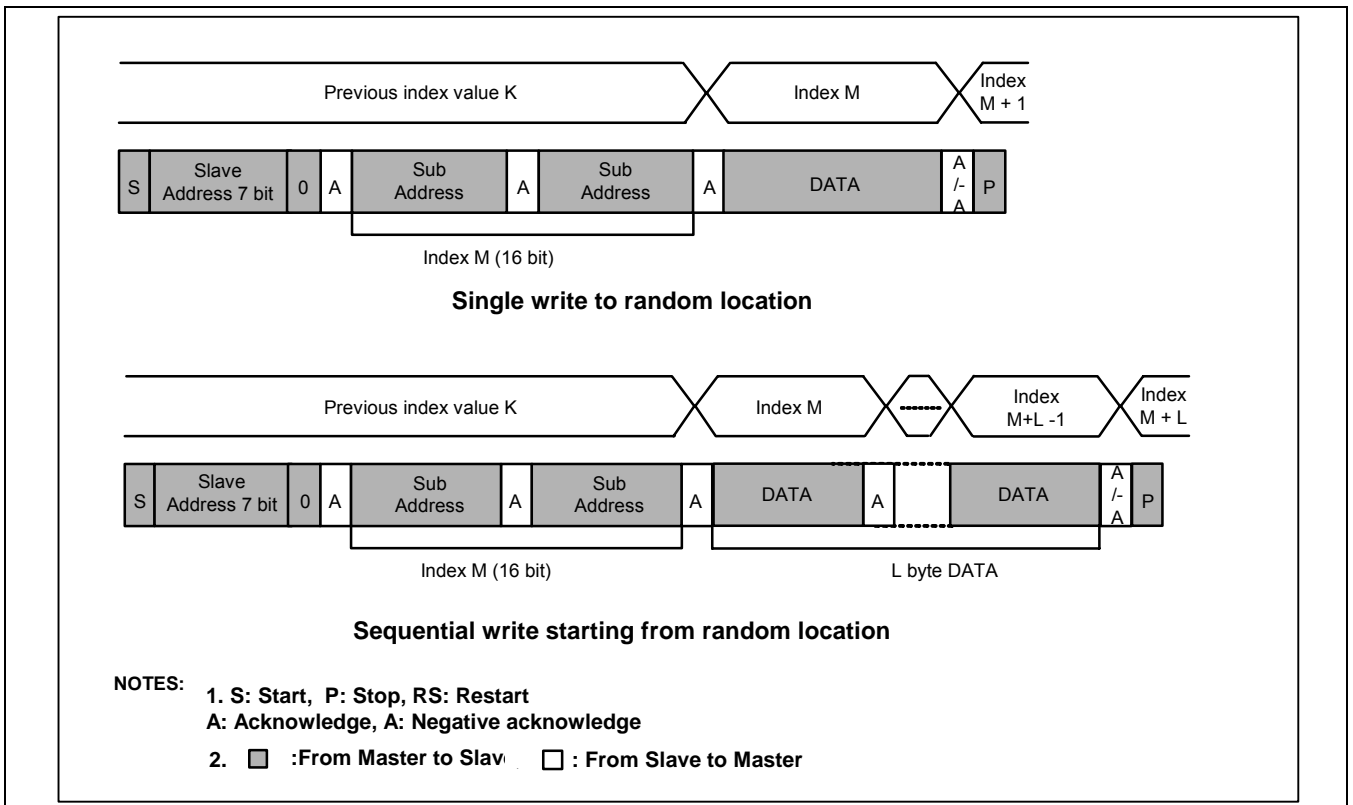


Figure 13. CCI Write Operation

8.2 CCI TIMING

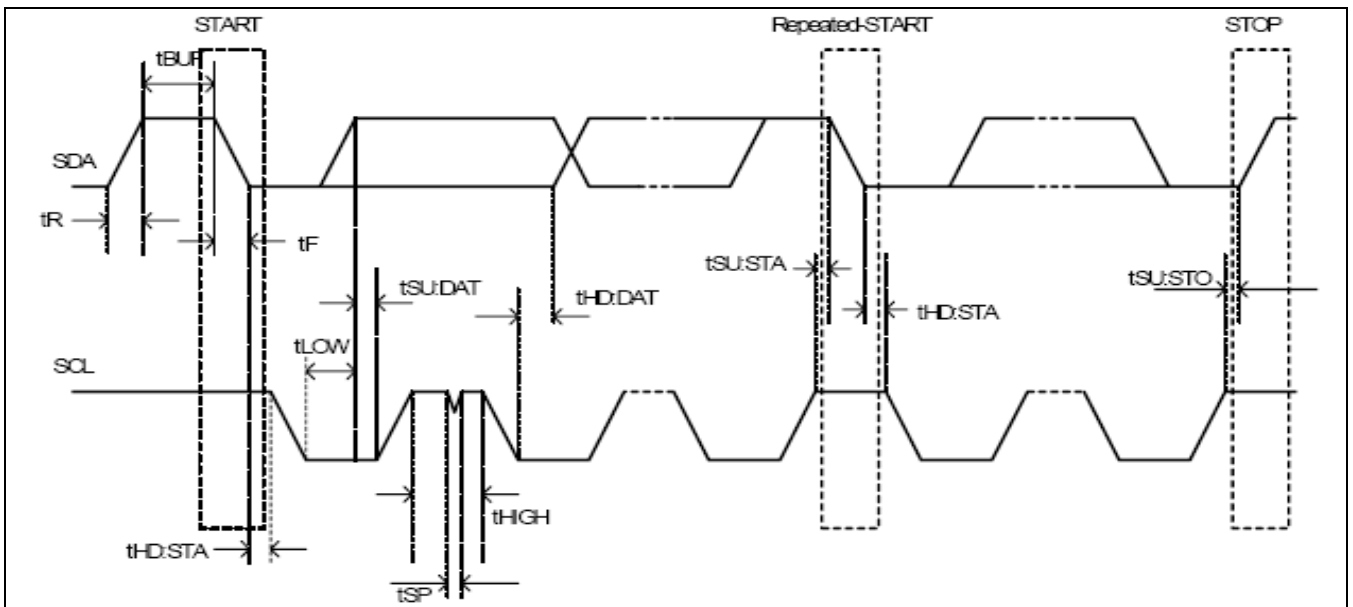


Figure 14. CCI Timing

Table 3 : CCI Timing Specifications

($V_{IHmin} = 0.9 V_{DD}$, $V_{ILmax} = 0.1 V_{DD}$, External pull-up resistor = 4.7kOhm at SCL/SDA for Fast-mode)

Parameter	Symbol	Standard-mode		Fast-mode		Units
		Min	Max	Min	Max	
Output fall time from V_{IHmin} to V_{ILmax}	tof	-	250	$20 + 0.1 CB *$	250	ns
Pulse width of spikes which must be suppressed by the input filter.	tSP	N/A	N/A	0	50	ns
SCL clock frequency	fSCL	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	tHD:STA	0.4	-	0.6	-	us
LOW period of the SCL clock	tLOW	4.7	-	1.3	-	us
HIGH period of the SCL clock	tHIGH	4.0	-	0.6 (5)	-	us
Setup time for a repeated START condition	tSU:STA	4.7	-	0.6	-	us
Data hold time	tHD:DAT	0 (3)	3.45 (4)	0 (3)	0.9 (4)	us
Data setup time	tSU:DAT	250 (2)	-	100 (2)	-	ns
Rise time of both SDA and SCL signals	tr	-	1000	$20 + 0.1 CB *$	300	ns
Fall time of both SDA and SCL signals	tf	-	300	$20 + 0.1 CB *$	300	ns
Setup time for STOP condition	tSU:STO	4.0	-	0.6	-	us
Bus free time between a STOP and START condition	tBUF	4.7	-	1.3	-	us

NOTE

*CB : from 10pF to 400pF

(1) CB = Total capacitance of one bus line in pF

(2) A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250ns$ must be then met. This will be automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the low period of SCL signal, it must output the next data bit to the SDA line $t_{rMAX} + t_{SU;DAT} = 1000 + 250 = 1250 ns$ (according to the Standard-mode I2 bus specification) before the SCL line is released.

(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

(4) The maximum $t_{HD;DAT}$ has only to be met if the device does not meet the LOW period (t_{LOW}) of the SCL signal.

(5) 0.6 us is available with the external clock 14MHz over range.



9 POWER UP/DOWN SEQUENCE

9.1 POWER UP SEQUENCE

The digital and analogue supply voltages can be powered up in any order e.g. VDIG then VANA or VANA then VDIG.

On power Up :

- If XSHUTDOWN is low when the power supplies are brought up then the sensor module will go into hardware standby mode.
- If XSHUTDOWN is high when the power supplies are brought up then the sensor module will go into software standby mode

In both cases the presence of an on-chip power-on reset cell ensures that the CCI register values are initialized correctly to their default values. The EXTCLK clock can either be initially low and then enabled during software standby mode or EXTCLK can be a free running clock.

Table 4 : Power-Up Sequence Timing Constraints (Serial Output Case)

Constant	Label	Min	Max	Units
VANA rising – VDIG rising	t0	VANA and VDIG may rise in any order. The rising separation can vary from 0ns to indefinite		ns
VDIG rising – VANA rising	t1			ns
VANA rising – XSHUTDOWN rising	t2	0.0	-	ns
XSHUTDOWN rising – First I2C transaction	t3	2400	-	EXTCLK cycles
Minimum No. of EXTCLK cycles prior to the first I2C transaction	t4	2400	-	EXTCLK cycles
PLL start up/lock time	t5	-	1	ms
Entering streaming mode – first frame start sequence (fixed part)	t6	-	10	ms
Entering streaming mode – first frame start sequence (variable part)	t7	The delay is the coarse integration time value		lines
DPHY Recovery Time (T_{WAKEUP})	t8	1	-	ms
DPHY Initialization Period (T_{INIT})	t9	0.1	-	ms

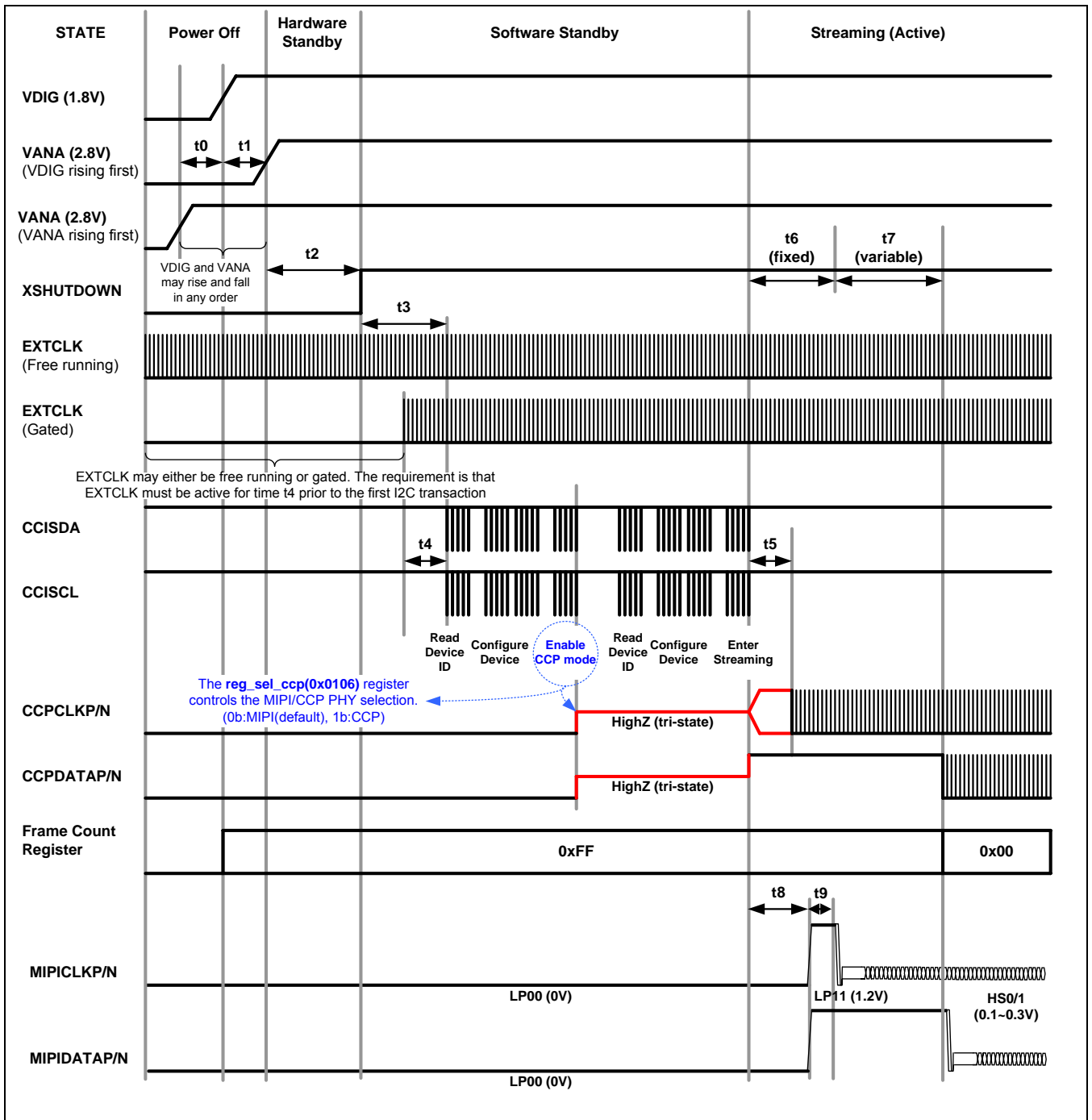
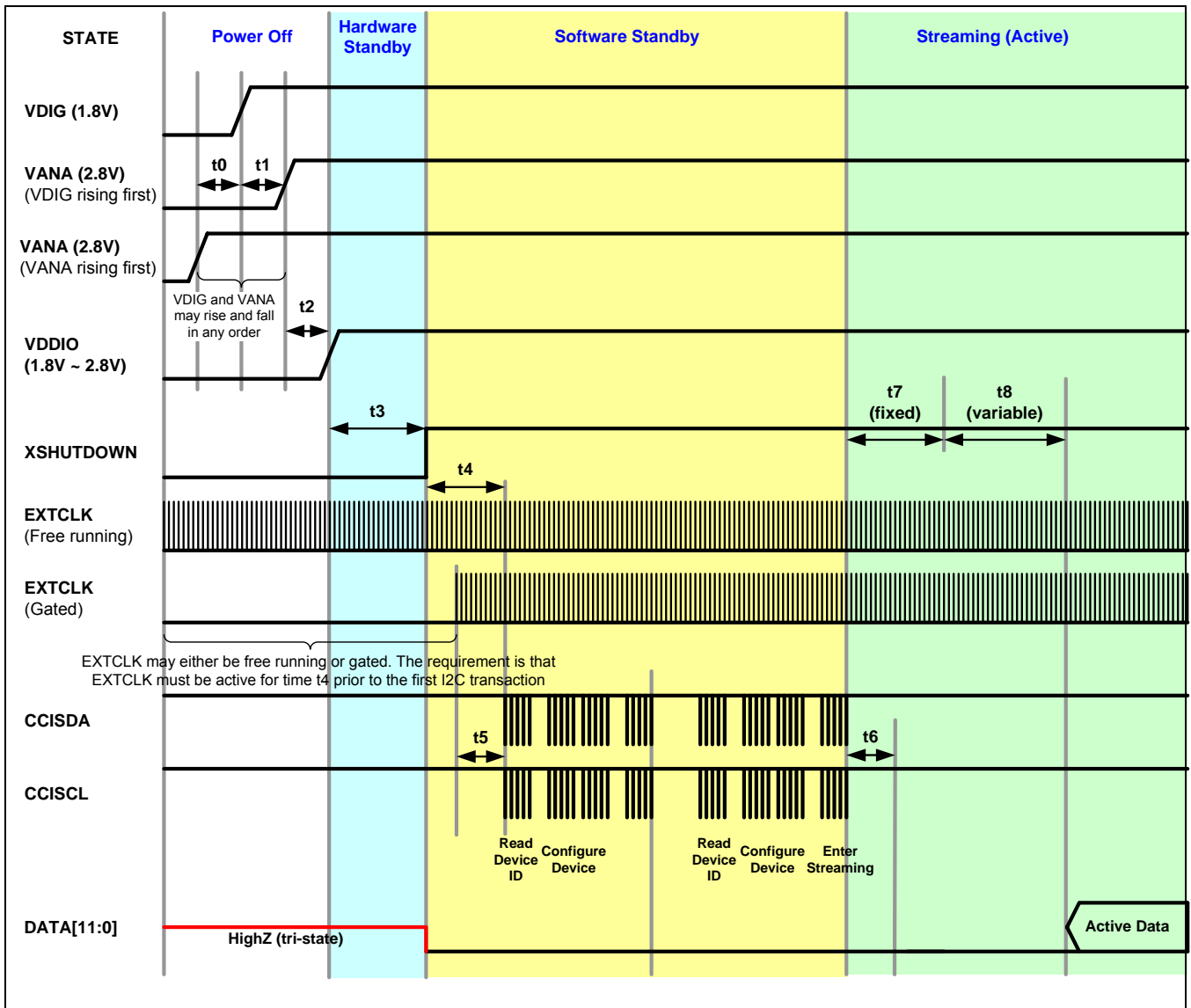


Figure 15. Power-Up Sequence (Serial Output Case)

Table 5 : Power-Up Sequence Timing Constraints (Parallel Output Case)

Constant	Label	Min	Max	Units
VANA rising – VDIG rising	t0	VANA and VDIG may rise in any order. The rising separation can vary from 0ns to indefinite		ns
VANA rising – VDIG rising	t1			ns
VDDIO rising – XSHUTDOWN rising	t2	0.0	-	ns
VANA rising – VDDIO rising	t3	0.0	-	ns
XSHUTDOWN rising – First I2C transaction	t4	2400	-	EXTCLK cycles
Minimum No. of EXTCLK cycles prior to the first I2C transaction	t5	2400	-	EXTCLK cycles
PLL start up/lock time	t6	-	1	ms
Entering streaming mode – first frame start sequence (fixed part)	t7	-	10	ms
Entering streaming mode – first frame start sequence (variable part)	t8	The delay is the coarse integration time value		lines



[Note]

1. User must set TST[3:0] PADs as (4'b0001) (bonding codition).

Figure 16. Power-Up Sequence (Parallel Output Case)

9.2 POWER DOWN SEQUENCE

The digital and analogue supply voltages can be powered down in any order e.g. VDIG then VANA or VANA then VDIG.

Similarly to the power-up sequence the EXTCLK: input clock may be either gated or continuous.

If the CCI command to exit streaming is received while a frame of valid active data is being output then the sensor module must wait to the frame end code before entering software standby mode.

If the CCI command to exit streaming mode is received during the inter frame time then the sensor module must enter software standby mode immediately.

Table 6 : Power-Down Sequence Timing Constraints (Serial Output Case)

Constant	Label	Min	Max	Units
Enter Software Standby CCI command – Device in Software Standby mode	t0	If outputting a frame of MIPI data waits to MIPI frame end code before entering software standby, otherwise enter software standby mode immediately.		
Minimum no of EXTCLK cycles after the last I2C transaction or MIPI frame end code.	t1	512	-	EXTCLK cycles
Last I2C Transaction or MIPI frame end code– XSHUTDOWN falling	t2	512	-	EXTCLK cycles
XSHUTDOWN falling – VANA falling	t3	0.0	-	ns
VANA falling – VDIG falling	t4	VANA and VDIG may fall in any order. The falling separation can vary from 0ns to Indefinite.		Ns
VDIG falling – VANA falling	t5			ns

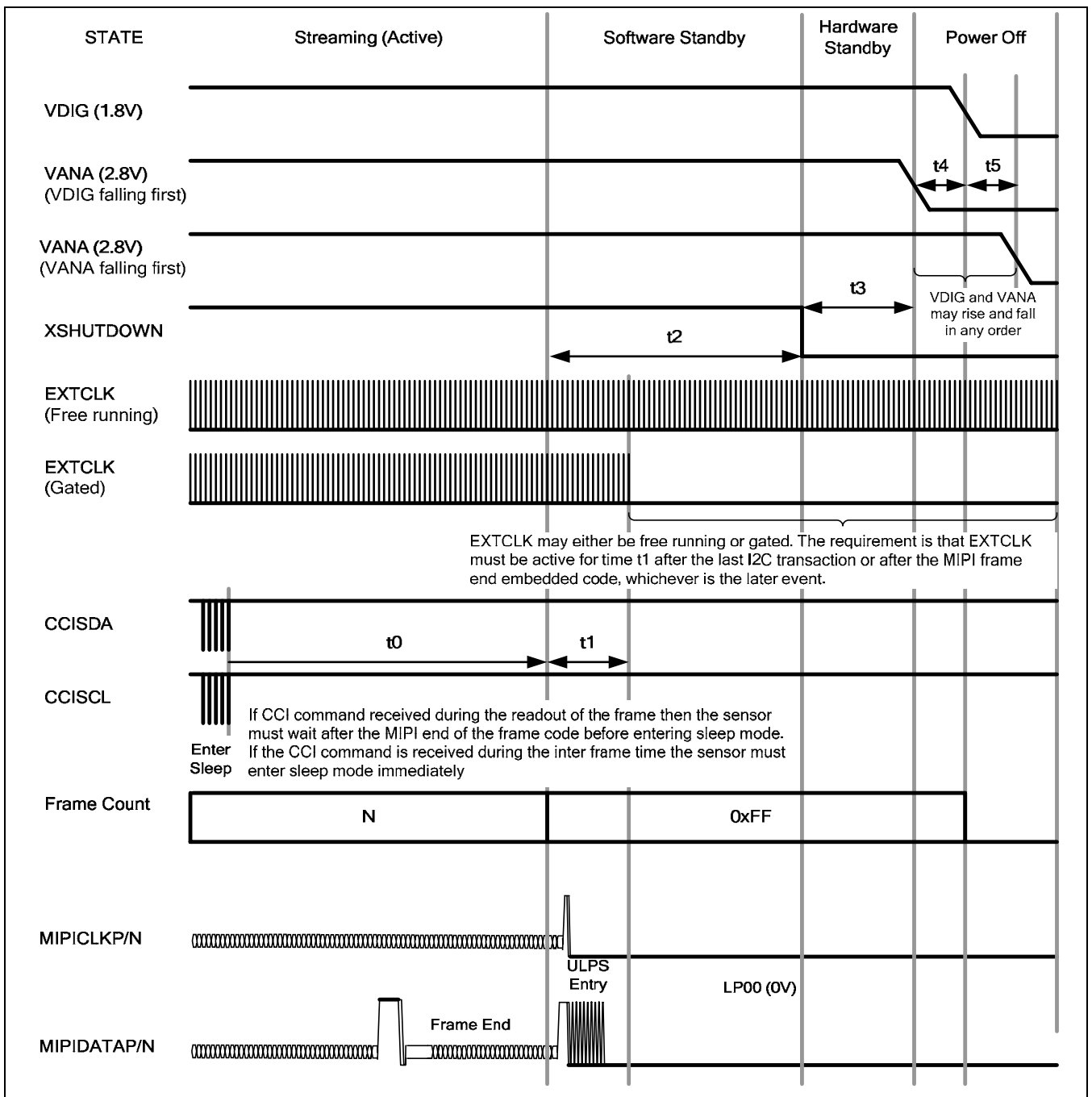


Figure 17. Power-Down Sequence (Serial Output Case)

Table 7 Power-Down Sequence Timing Constraints (Parallel Output Case)

Constant	Label	Min	Max	Units
Enter Software Standby CCI command – Device in Software Standby mode	t0	If outputting a frame of data waits to frame end before entering software standby, otherwise enter software standby mode immediately.		
Minimum no of EXTCLK cycles after the last I ² C transaction or frame end	t1	512	-	EXTCLK cycles
Last I ² C Transaction or frame end – XSHUTDOWN falling	t2	512	-	EXTCLK cycles
XSHUTDOWN falling – VANA falling	t3	0.0	-	ns
VANA falling – VDIG falling	t4	VANA and VDIG may fall in any order. The falling separation can vary from 0ns to Indefinite.		ns
VDIG falling – VANA falling	t5			ns
VANA falling – VDDIO falling	t6	0.0	-	ns

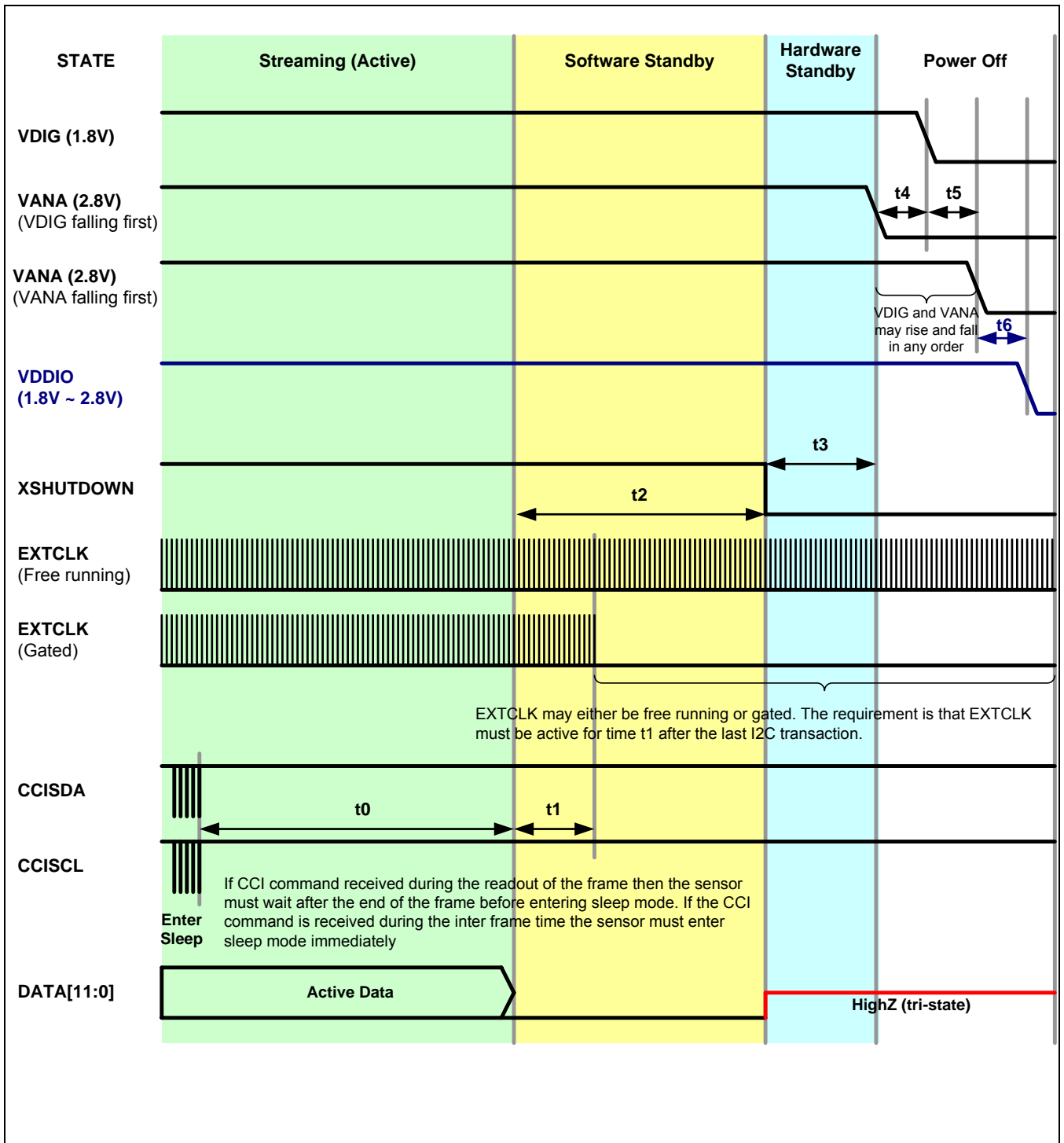


Figure 18. Power-Down Sequence (Parallel Output Case)

10 FUNCTIONAL FEATURE

10.1 DARK LEVEL COMPENSATION

The image sensor has an on-chip ADC. Column parallel ADC scheme is used for low power analog processing.

10.1.1 CORRELATED DOUBLE SAMPLING (CDS)

The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action and some fixed pattern noise caused by the in-pixel amplifier offset deviation. To eliminate those noise components, a Correlated Double Sampling (CDS) circuit is used before converting to digital. The output signal sampled twice, once for the reset level and once for the actual signal level sampling.

10.1.2 ANALOG GAIN CONTROL

The user can control the gain of pixel signal by Analog Gain Control Register (analogue_gain_code_global). According to SMIA 1.0 specification, the analog gain can be given by the following equation:

$$\text{Analog Gain} = (m0 \times x + c0) / (m1 \times x + c1)$$

S5K3H1GX specifies analog gain by coefficients of $m0 = 1$, $c0 = 0$, $m1 = 0$, $c1 = 32$. As a result, users can control analog gain as following equation:

$$\text{Analog Gain} = \text{analogue_gain_code_global} [15:0] / 32$$

10.2 DATA PEDESTAL

The data pedestal is the pixel value the sensor module produces when there is no light incident on the sensor module. The sensor module must have an internal calibration function, which ensures that data pedestal value remains constant with integration time, gain, and temperature and between different sensors. The host system should always use the data_pedestal register value to determine the sensor output black level.

Register Name	Type	RW	Comment
data_pedestal	16-bit unsigned integer	RO Static	

System	Typical Data Pedestal
8-bit	16
10-bit	64
12-bit	256

10.3 GLOBAL RESET

The S5K3H1GX provides global reset mode. Global reset allows all rows to have the same integration start and end. Global reset mode is used in conjunction with the external mechanical shutter controlled by host. The host must program following the sequence and restrictions.



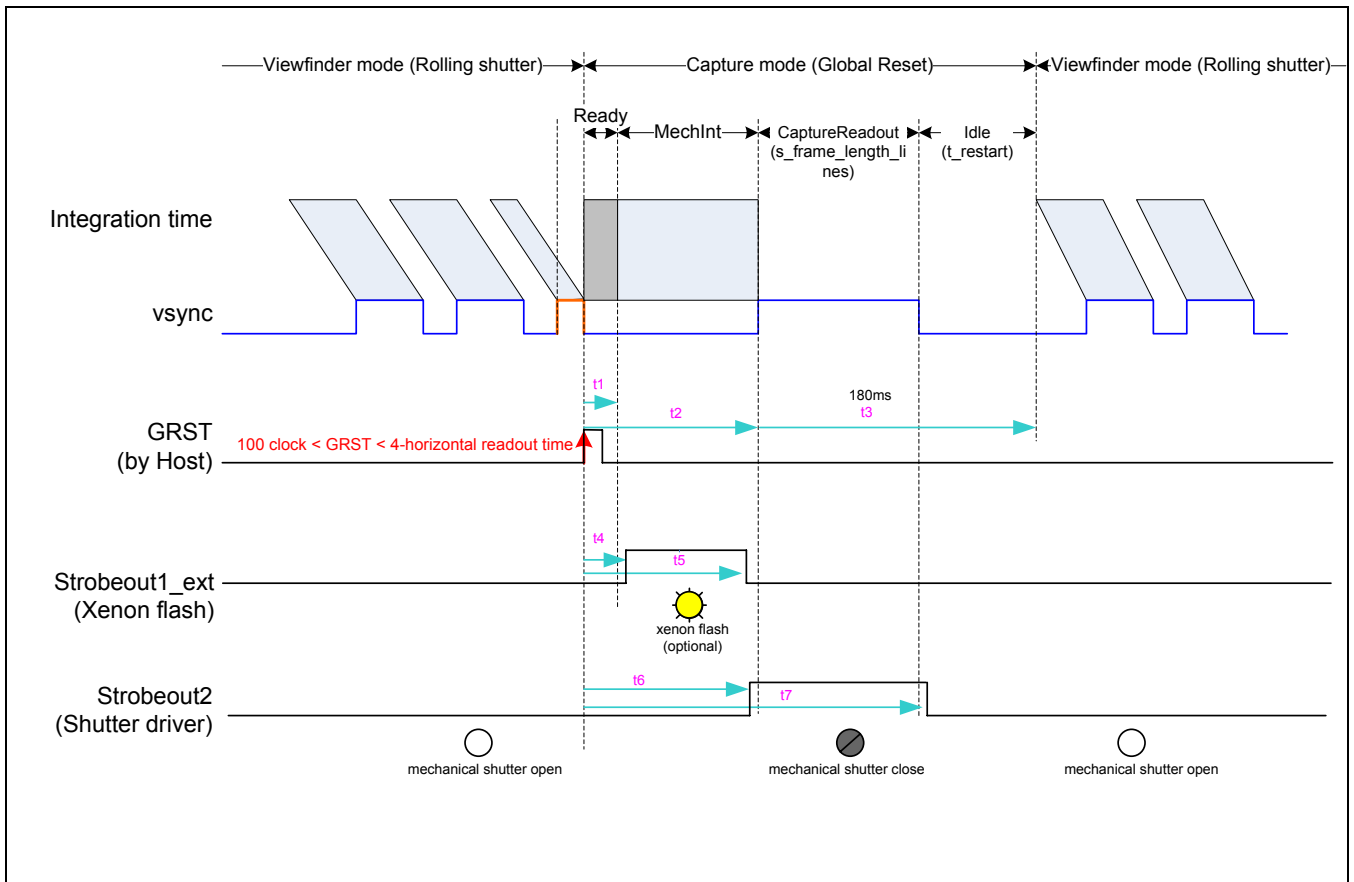


Figure 19. Global Reset Timing

10.3.1 Starting the Global Reset Sequence

The host starts global reset operation by rising edge of GRST signal. This operation stops current rolling shutter frame. In case of using Parallel mode, if GRST signal is asserted while a frame is being transferred the frame is truncated, immediately. In case of using MIPI bus, if GRST signal is asserted while a frame is being transferred the frame is truncated after the line end sync code out during t_ready time..

S5K3H1GX has “shadow” registers for global reset frame settings, which may be different from the viewfinder settings. (Exposure time, analog gain, etc) Before asserting the GRST signal, the host programs the timings.

10.3.2 Indicating the Start of the Exposure to Host

The delay from the rising edge of GRST to start of the exposure (t_ready) of all rows is the same regardless of the time instant GRST is asserted. The t_ready is a programmable parameter.

10.3.3 Starting the Frame Readout

The host can control readout start time which is same with integration time or longer. The t_readout is synchronized to rising edge of GRST.

10.3.4 Starting the Rolling Shutter Mode After Global Reset

S5K3H1GX starts the viewfinder mode automatically after frame readout. The host does not need to program the viewfinder settings because S5K3H1GX has separate set of registers for viewfinder and global reset frames.

10.3.5 Programmable Output Strobe Signals

S5K3H1GX may provide one or two programmable output strobe signals. The signals are synchronized to the rising edge of GRST, as every other signal in the sequence. The assertion of the strobes is controlled by **t_flash_strt**, **t_flash_end**, **t_shut_strt**, **t_shut_end**, as shown in the above Figure 19.

10.3.6 Programmable Registers Descriptions

t_ready (t1) : Time to prepare GRST including pixel reset time.

t_readout (t2) : Captured frame readout time after integration. **Actual integration time is (t2-t1).**

t_restart + s_frame_length_lines (t3) : Closed Mechanical shutter re-open time to return to ERS mode after captured frame readout. **Capture frame size + shutter closing time**

t_flash_strt (t4): Rising Point for Strobeout1

$$t1 < t_flash_start < t2 - 25lines \text{ (Fixed by design margin)}$$

t_flash_end (t5): Falling Point for Strobeout1

$$t4 < t_flash_end < t2 - 25lines \text{ (Fixed by design margin)}$$

t_shut_strt (t6): Rising Point for Strobeout2

$$t1 < t_shut_strt < t2 - 25lines \text{ (Fixed by design margin)}$$

t_shut_end (t7): Falling Point for Strobeout2

$$t2 + s_frame_length_lines < t_shut_end < t2 + t3$$

Index	Reset Value	Bits	Register Name	RW	Comment
0x302F	0x00	[31:0]	t_ready	RW	Designer Guide Value
0x3030	0x00			RW	
0x3031	0x14			RW	
0x3032	0x46			RW	
0x3033	0x00	[31:0]	t_readout	RW	Captured frame readout time after integration
0x3034	0x20			RW	
0x3035	0xBB			RW	
0x3036	0xB0			RW	
0x3037	0x00	[31:0]	t_flash_strt	RW	Rising Point for Strobeout1
0x3038	0x00			RW	
0x3039	0x00			RW	
0x303A	0x00			RW	
0x303B	0x00	[31:0]	t_flash_end	RW	Falling Point for Strobeout1
0x303C	0x00			RW	

0x303D	0x00			RW	
0x303E	0x00			RW	
0x303F	0x00			RW	
0x3040	0x00	[31:0]	t_shut_strt	RW	Rising Point for Strobeout2
0x3041	0x00			RW	
0x3042	0x00			RW	
0x3043	0x00			RW	
0x3044	0x00			RW	
0x3045	0x00	[31:0]	t_shut_end	RW	Falling Point for Strobeout2
0x3046	0x00			RW	
0x3047	0x04			RW	
0x3048	0xE2			RW	
0x3049	0x00	[15:0]	t_atx_width	RW	Designer Guide Value
0x304A	0x00			RW	
0x3049	0x00	[15:0]	t_restart	RW	Closed Mechanical shutter re-open time to return to ERS mode after captured frame readout
0x304A	0x00			RW	

10.3.7 Shadow registers (Capture Frame Setting Registers)

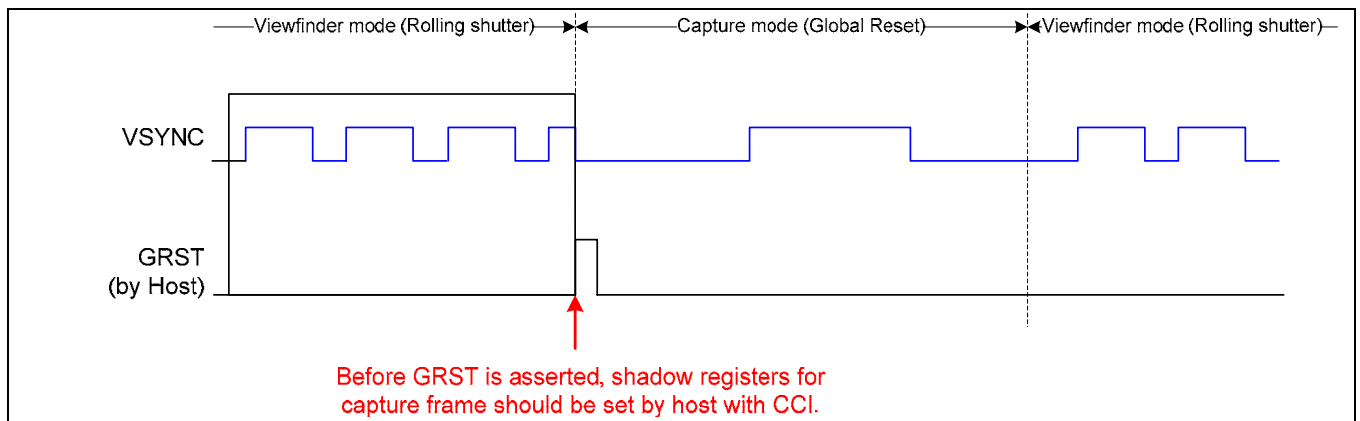


Figure 20. Shadow register setting time

Index	Reset Value	Bits	Register Name	RW	Comment
0x30D4	0x08	[7:4]	reserved	RO	
		[3:0]	s_outif_offset_video	RW	Shadow Number of valid bytes in last 12byte word for video
0x30D5	0x10	[15:0]	s_video_data_length	RW	Shadow length (in bytes) of video data for transmission
0x30D6	0x04			RW	
0x30D7	0x0C	[15:0]	s_x_output_size	RW	
0x30D8	0xD0			RW	
0x30D9	0x09	[15:0]	s_y_output_size	RW	
0x30DA	0xA0			RW	
0x30DB	0x00	[7:0]	s_Scaling_mode	RW	0 – No scaling 1 – Horizontal Scaling 2 – Full Scaling (both horizontal and vertical)

0x30DC	0x00	[7:0]	s_Spatial_sampling	RW	0 – Bayer Sampling 1 – Co-sited 2 – <i>Reserved</i>
0x30DD	0x10	[7:0]	s_scale_m	RW	Down scale factor: M component Range: 1 to 16 upwards Format: 16-bit unsigned integer
0x30DE	0x05	[15:0]	s_fifo_water_mark_pixels	RW	FIFO usage level triggering Line output Format : 16bit unsigned integer
0x30DF	0x30			RW	
0x30E9	0x09	[15:0]	s_frame_length_lines	RW	
0x30EA	0xAC			RW	
0x30EB	0x0D	[15:0]	s_line_length_pck	RW	
0x30EC	0x8E			RW	
0x30F1	0x00	[15:0]	s_x_addr_start	RW	
0x30F2	0x00			RW	
0x30F3	0x0C	[15:0]	s_x_addr_end	RW	
0x30F4	0xCF			RW	
0x30F5	0x00	[15:0]	s_y_addr_start	RW	
0x30F6	0x00			RW	
0x30F7	0x09	[15:0]	s_y_addr_end	RW	
0x30F8	0x9F			RW	
0x30F9	0x01	[7:0]	s_x_even_inc	RW	
0x30FA	0x01	[7:0]	s_x_odd_inc	RW	
0x30FB	0x01	[7:0]	s_y_even_inc	RW	
0x30FC	0x01	[7:0]	s_y_odd_inc	RW	
0x30FD	0x00	[15:13]	<i>reserved</i>	RO	
0x30FE	0x20	[12:0]	s_analogue_gain_code_Global	RW	
0x30FF	0x20	[7]	s_hd_mode	RW	
		[6]	s_h_average_en	RW	
		[5]	s_h_wb_bypass	RW	bypass or w_binning selection signal
		[4]	s_avg_mode	RW	
		[3]	s_h_avg_subsmpl_en	RW	
		[2]	s_v_avg_subsmpl_en	RW	0b : normal / 1b : v_avg_en
		[1]	s_h_mirror	RW	
		[0]	s_v_flip	RW	
0x3100	0x00	[15:0]	s_analogue_gain_code_greenR	RW	
0x3101	0x20			RW	
0x3102	0x00	[15:0]	s_analogue_gain_code_red	RW	
0x3103	0x20			RW	
0x3104	0x00	[15:0]	s_analogue_gain_code_blue	RW	
0x3105	0x20			RW	
0x3106	0x00	[15:0]	s_analogue_gain_code_greenB	RW	
0x3107	0x20			RW	
0x3180	0x67	[7:0]	s_sh4ch_blk_width	RW	Grid Block Horizontal direction Size, ceil(2624/16)
0x3181	0x9A	[7:0]	s_sh4ch_blk_height	RW	Grid Block Vertical direction Size, ceil(1968/16)
0x3182	0x02	[15:0]	s_sh4ch_step_x	RW	Horizontal Direction Step Size, floor(2^16/sh_4ch_blk_width_r)
0x3183	0x7C			RW	
0x3184	0x01	[15:0]	s_sh4ch_step_y	RW	Vertical Direction Step Size, floor(2^16/sh_4ch_blk_height_r)
0x3185	0xAA			RW	
0x3186	0x00	[7:0]	s_sh4ch_start_blk_cnt_x	RW	
0x3187	0x00	[7:5]	<i>reserved</i>	RO	

		[4:0]	s_sh4ch_start_int_cnt_x	RW	
0x3188	0x00	[15:0]	s_sh4ch_start_frac_cnt_x	RW	
0x3189	0x00			RW	
0x318A	0x00	[7:0]	s_sh4ch_start_blk_cnt_y	RW	
0x318B	0x00	[7:5]	reserved	RO	
		[4:0]	s_sh4ch_start_int_cnt_y	RW	
0x318C	0x00	[15:0]	s_sh4ch_start_frac_cnt_y	RW	
0x318D	0x00			RW	

10.4 DE-RATING

To provide a wider range of data rate reduction function is able to reduce the data rates in both the horizontal and vertical directions. This is achieved by the use of a FIFO between video timing and output clock domains (Figure 21).

Index	Reset Value	Bits	Register Name	RW	Description
0x0400	0x0000	[15:0]	Derating_en	RW	0 – De-rating disable
0x0401					1 – De-rating enable

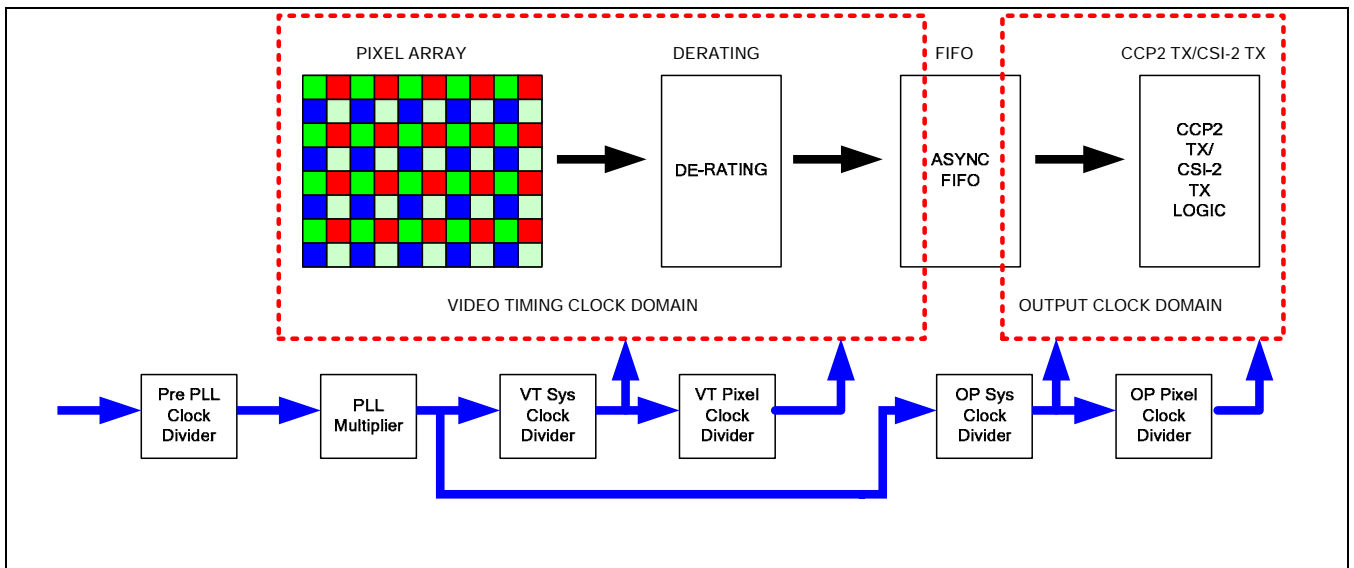


Figure 21. De-RatingBlock Diagram

To use De-Rating on MIPI mode, horizontal blank should be enough for MIPI SoT/EoT operation. Its minimum value depends on the number of MIPI data lane, output data format, and the Bit Clock.

$$line_length_pck \geq (\text{Minimum H-Blank}^{(1)} + x_addr_end - x_addr_start + 1)$$

Number of MIPI Data Lane	Output Data Format	Bit Clock	Minimum H-Blank ⁽¹⁾
1Lane	Bayer 8bit	Over 500MHz	$106 \times (\text{op_sys_clk_div} \times \text{op_pix_clk_div}) / (\text{vt_sys_clk_div} \times \text{vt_sys_clk_div})$
		Under 500MHz	$92 \times (\text{op_sys_clk_div} \times \text{op_pix_clk_div}) / (\text{vt_sys_clk_div} \times \text{vt_sys_clk_div})$
	Bayer 10bit	Over 500MHz	$96 \times (\text{op_sys_clk_div} \times \text{op_pix_clk_div}) / (\text{vt_sys_clk_div} \times \text{vt_sys_clk_div})$
		Under 500MHz	$84 \times (\text{op_sys_clk_div} \times \text{op_pix_clk_div}) / (\text{vt_sys_clk_div} \times \text{vt_sys_clk_div})$
2Lane	Bayer 8bit	Over 500MHz	$158 \times (\text{op_sys_clk_div} \times \text{op_pix_clk_div}) / (\text{vt_sys_clk_div} \times \text{vt_sys_clk_div})$
		Under 500MHz	$134 \times (\text{op_sys_clk_div} \times \text{op_pix_clk_div}) / (\text{vt_sys_clk_div} \times \text{vt_sys_clk_div})$
	Bayer 10bit	Over 500MHz	$136 \times (\text{op_sys_clk_div} \times \text{op_pix_clk_div}) / (\text{vt_sys_clk_div} \times \text{vt_sys_clk_div})$
		Under 500MHz	$112 \times (\text{op_sys_clk_div} \times \text{op_pix_clk_div}) / (\text{vt_sys_clk_div} \times \text{vt_sys_clk_div})$

10.5 TEST PATTERN

Two types of full frame deterministic test patterns are defined. Most are Bayer test patterns more suitable for some tests than real image data and are injected early in the sensor data path. The only exception to this is a test pattern that is intended to test sensor-host link integrity, the data in this pattern is not Bayer data and it is injected just prior to serializer.

Use of these full frame test patterns is controlled by the test_pattern_mode parameter. The following table shows all the defined parameter settings.

Parameter Name	Type	R/W	Coding	Function
test_pattern_mode	16-bit unsigned integer	RW	0 – no pattern (default) 1 – solid color 2 – 100 % color bars 3 – fade to grey color bars 4 – PN9 (no embedded lines) 5 – 255 reserved 256-65535 – manufacturer specific	Controls the output of the test pattern mode

10.6 PN9 CODE GENERATION

The PN9 test pattern is included to ease testing of sensor-link integrity (measurement of bit error rate etc). PN9 linear feedback shift register has the polynomial $X^9 + X^5 + 1$ in Fibonacci type notation (Figure 22). The reset value of

PN9 is 0x1FF.

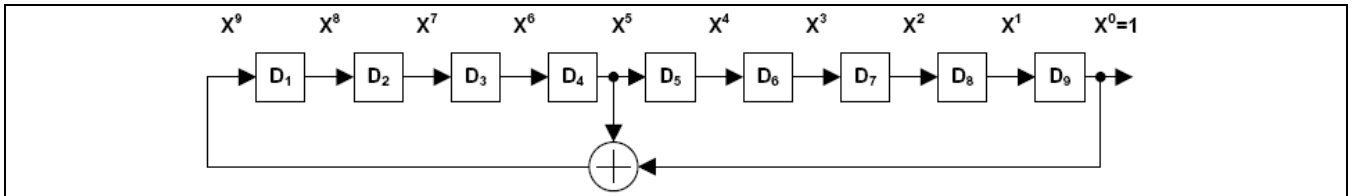


Figure 22. PN9 Linear Feedback Shift Registers

10.7 COLOR SHADING CORRECTION

S5K3H1GX’s color shading compensation method is a Grid-Type and four channels processing, R, Gr, Gb and B. We divide each channel’s profile into M by N grids and calculate compensation factor at points of intersection. Finally, M+1 by N+1 coefficient are extracted. We compress coefficients (M+1 by N+1) into a K by L SEED matrix using RNP data processing algorithm (Recursive – Near Polynomial, invented by SEC). This method describes computation effective representation of 2D function, which reconstruction does not require multipliers. We can design various orders’ function like as polynomial using only adder and bit shifter. Resulting surface is equivalent in complexity and number of parameters to the polynomial surface. Those SEED values, signed fixed point values, will be written to OTP by module maker. Its total size is 2,880bits. Anti-Color shading block has a RNP decoder. This decoder de-compress K by L SEED matrix to M+1 by N+1 compensation factors. Total consuming time is about 16,000 operating clocks (Data transferring time from OTP to Anti-Shade Block + Decoding time). After that, we get each input’s compensation factor by bi-linear interpolation using nearest 4 node points’ of current input pixel location. We can control the result shape of compensation profile and ratio before calculating SEED value by application program. Ratio means the intensity degree from image center to corner. SEC can release this tool to customer.

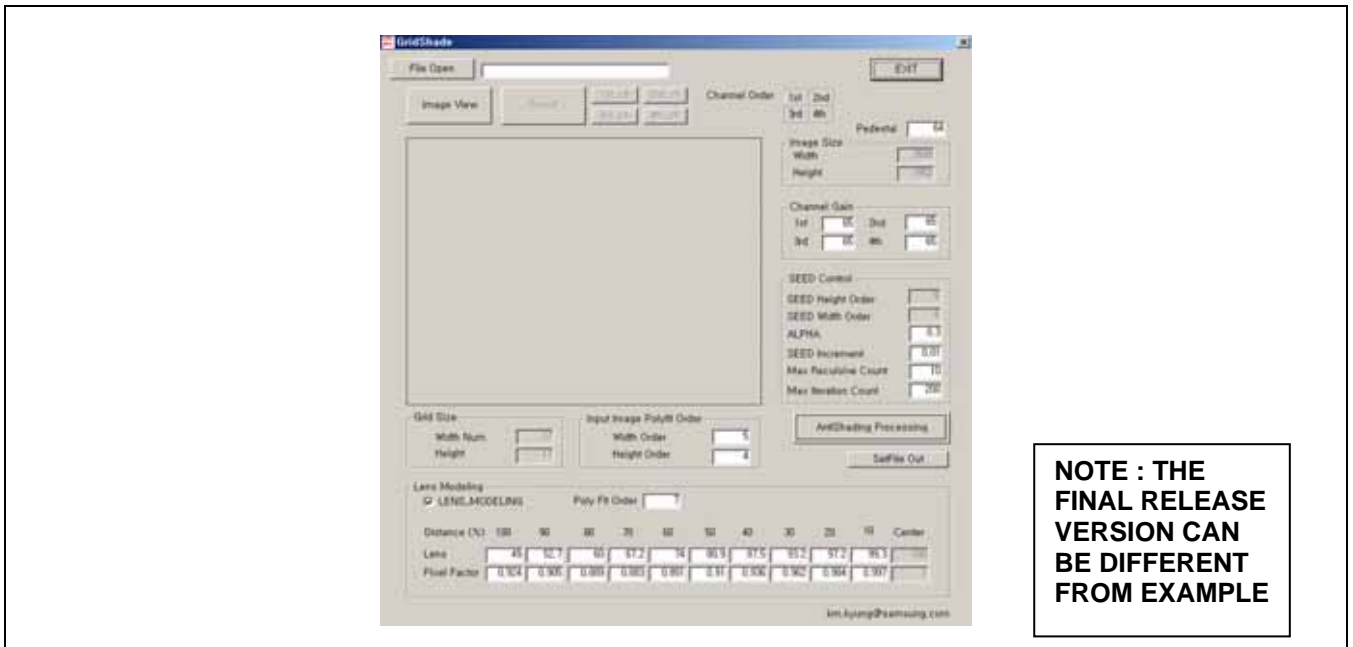


Figure 23. Example of Control Application Program

10.8 SHADING DECOMPRESSION SEQUENCE

Shading has two parts which are decompression and compensation block. The compensation block must be op-

erated after decompression block works because the compensation block needs grid-gains which are decompressed. Decompression Sequence is below and the compensation block can be controlled by bypass register(the lowest bit of 0x3200 address, shade_bypass). The important this is that compensation block is worked when hsync and vsync are active although bypass is turn-off.

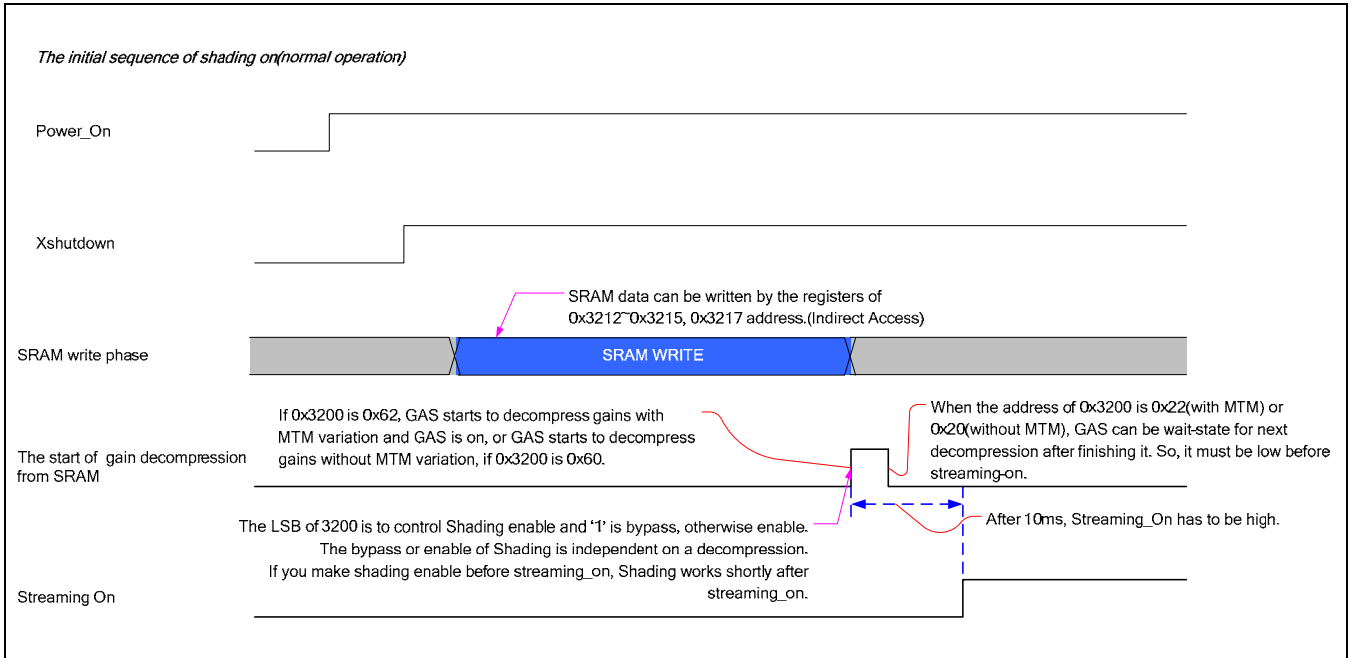


Figure 24. Shading Decompression Sequence

10.9 MSR REGISTER EQUATION

If the input size of shading is changed(sub-sampling or cropping), several registers should be set to different values according to the equations. The registers which are used for the equations are from TG. See below table.

* TG registers which is used for auto-MSR calculation:

Index	Reset Value	Bits	Register Name	RW	Description
0x0344	0x0000	[15:0]	x_addr_start	RW	X-address of the top left corner of the visible pixel data Format: 16-bit unsigned integer (Pixels)
0x0345					
0x0346	0x0000	[15:0]	y_addr_start	RW	Y-address of the top left corner of the visible pixel data Format: 16-bit unsigned integer (Lines)
0x0347					
0x0380	0x0001	[15:0]	x_even_inc	RW	Increment for even pixels – 0, 2, 4 etc Format: 16-bit unsigned integer
0x0381					
0x0382	0x0001	[15:0]	x_odd_inc	RW	Increment for odd pixels – 1, 3, 5 etc Format: 16-bit unsigned integer
0x0383					
0x0384	0x0001	[15:0]	y_even_inc	RW	Increment for even pixels – 0, 2, 4 etc Format: 16-bit unsigned integer
0x0385					
0x0386	0x0001	[15:0]	y_odd_inc	RW	Increment for odd pixels – 1, 3, 5 etc Format: 16-bit unsigned integer
0x0387					

The description of equation is as follows:

1. sh4ch_blk_width_r(0x3201, 8bits)

Grid Anti-Shade in S5K3H1GX separates 17x17 grid from a frame.

This register stands for the width of a grid.(unit : the number of pixels)

In H/W, the datapath is double, so that there are even data and odd data in one clock.(Full_Width is h active size from sensor, Full_Width is 3280 in case of S5K3H1GX)

2. sh4ch_blk_height_r(0x3202, 8bits)

this register stands for the height of a grid.(unit : the number of pixels)

(Full_Height is v active size from sensor, Full_Height is 2464 in case of S5K3H1GX)

Caution : embedded lines must be excluded in Full_Height.

3. sh4ch_step_x_r(0x3203: MSB part 8bits, 0x3204: LSB part 8bits)

Grid Anti-Shade operates bi-linear interpolation method for the pixels of a grid.

In this case, we must give the information of the distance between pixel and pixel in a grid which is rate when the distance of grid is 1. Of course, this register is fully fractional parts and 16bits.(this register < 1)

This register is for horizontal direction.

In H/W, the datapath is double, so that there are even data and odd data in one clock.

4. sh4ch_step_y_r(0x3205: MSB part 8bits, 0x3206: LSB part 8bits)

This register is responsible for the step of vertical direction as like sh4ch_step_x_r.

Of course, this register is fully fractional parts and 16bits.(this register < 1)

This register is for vertical direction.

5. sh4ch_start_blk_cnt_x_r(0x3207, 8bits)

This register stands for the point of start pixel position in a grid when input image is cropped.

So that, this is initial value for the position of first pixel in a grid per a line

In H/W, the datapath is double, so that there are even data and odd data in one clock.

6. sh4ch_start_blk_int_x_r(0x3208, 5bits)

This register stands for the first number of horizontal grids in a frame . In case of full image, this is 0.

In H/W, the datapath is double, so that there are even data and odd data in one clock.

7. sh4ch_start_frac_x_r(0x3209: MSB part 8bits, 0x320A: LSB part 8bits)

This register stands for the start value of horizontal step in a line. In case of full image, this is 0.

In H/W, the datapath is double, so that there are even data and odd data in one clock.

8. sh4ch_start_blk_cnt_y_r(0x320B, 8bits)

This register stands for the point of start line position in a grid when input image is cropped.

So that, this is initial value for the position of first line in a grid per a frame

9. sh4ch_start_blk_int_y_r(0x320C, 5bits)

This register stands for the first number of vertical grids in a frame. In case of full image, this is 0.

10. sh4ch_start_frac_y_r(0x320D: MSB part 8bits, 0x320E: LSB part 8bits)

This register stands for the start value of vertical step in a frame.

In case of full image, this is 0.

10.10 SHADING PROFILE OTP ROM

S5K3H1GX provides shading profile OTP ROM in order that color shading correction is performed outside of

camera module by ISP. This ROM's size is 720 bit and the all data are OTP registers. The data in the OTP should store shading profile data for each module

OTP	
Shading Coefficient ROM Size	36x20 = 720bit
Accessed by	CCI
Address Map	Indirect Address
Data information for Shading ROM	shading profile data for each module

Table 8 : OTP Control Registers

Index	Reset Value	Bits	Register Name	RW	Description
0x3125	0x95	[7:0]	otp_fen_cnt	RW	fen signal width control at otp write
0x3126	0x02	[7:0]	otp_read_cnt	RW	width control register related to using signal of otp read sequence
0x3127	0xB0	[7]	ecc_en	RW	ECC logic enable 0 : not used, 1 : used (default)
		[6]	otp_sec_dis	RW	efuse mode selection
		[5:4]	otp_sector_sel	RW	efuse mode selection
		[3]	rewrite_start	RW	start write stage enable
		[2]	write_start	RW	start initial stage enable
		[1]	fuse_start	RW	start pre write stage enable
		[0]	read_start	RW	start read stage enable
0x3128	0x00	[7:0]	otp_wdata0	RW	write data0
0x3129	0x00	[7:0]	otp_wdata1	RW	write data1
0x312A	0x00	[7:0]	otp_wdata2	RW	write data2
0x312B	0x00	[7:6]	reserved		reserved
		[5:0]	otp_raddr	RW	otp read address
0x312C	0x00	[7:0]	otp_Gsahde2	RO	Gshade data2 from otp[19:16]
0x312D	0x00	[7:0]	otp_Gsahde1	RO	Gshade data1 from otp[15:8]
0x312E	0x00	[7:0]	otp_Gsahde0	RO	Gshade data0 from otp[7:0]
0x312F	0x00	[7:0]	reserved		reserved
0x3130	0x00	[7:0]	reserved		reserved
0x3131	0x00	[7:0]	reserved		reserved
0x3132	0x00	[7:0]	reserved		reserved
0x3133	0x00	[7:0]	reserved		reserved
0x3134	0x00	[7:0]	reserved		reserved
0x3135	0x00	[7:0]	reserved		reserved
0x3136	0x00	[7:0]	reserved		reserved
0x3137	0x00	[7:0]	reserved		reserved
0x3138	0x00	[7:0]	reserved		reserved
0x3139	0x00	[7:0]	reserved		reserved
0x313A	0x00	[7:0]	reserved		reserved
0x313B	0x00	[7:0]	reserved		reserved

Index	Reset Value	Bits	Register Name	RW	Description
0x313C	0x00	[7:0]	reserved		reserved
0x313D	0x00	[7:0]	reserved		reserved
0x313E	0x00	[7:0]	reserved		reserved
0x313F	0x00	[7:0]	reserved		reserved
0x3140	0x00	[7:0]	reserved		reserved
0x3141	0x00	[7:0]	reserved		reserved
0x3142	0x00	[7:1]	reserved	-	reserved
		[0]	ecc_error	RO	when wrong efuse data is written, it is high

10.11 OTP READ WRITE PROCEDURE

The internal OTP size for the shading correction is 36x20 = 720 bits. Figure 25 shows the data structure in OTP array. The data for the shading correction consists of 36 rows. Each row has 20 bits. These 20 bits need 3 bytes to be written into the OTP. Each bit is assigned as below :

- 0x3128 : shading correction data[7:0] – D0, D3, ...
- 0x3129 : shading correction data[15:8] – D1, D4, ...
- 0x312A : {4'd0, shading correction data[19:16]} – D2, D5, ...

By using 3 addresses (0x3128, 0x3129, 0x312A) repeatedly, whole data for the shading correction is written into the OTP. The procedure about write/read of OTP is shown in Figure 26.

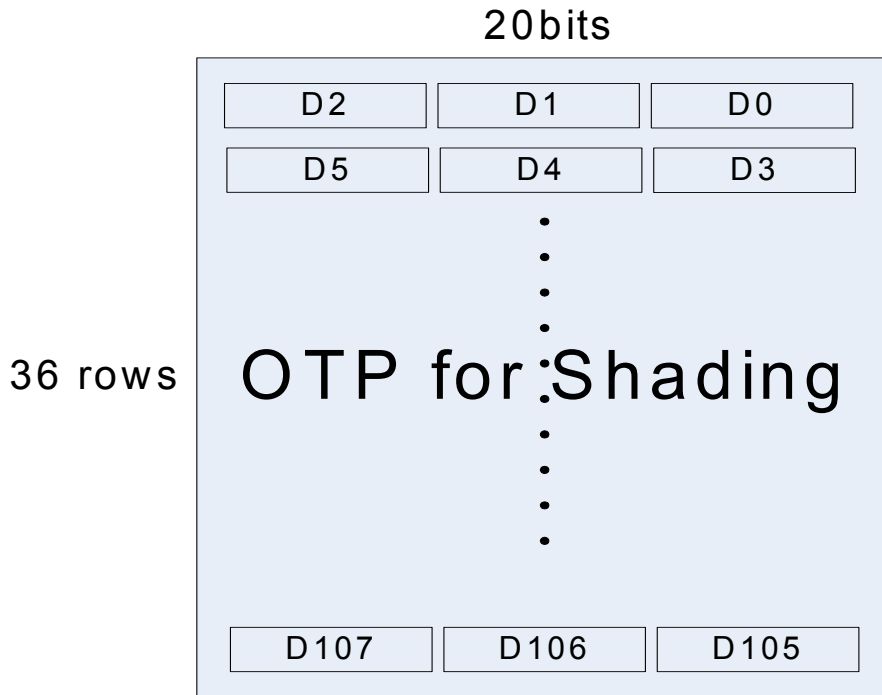


Figure 25. OTP(One-Time Programmable Memory)

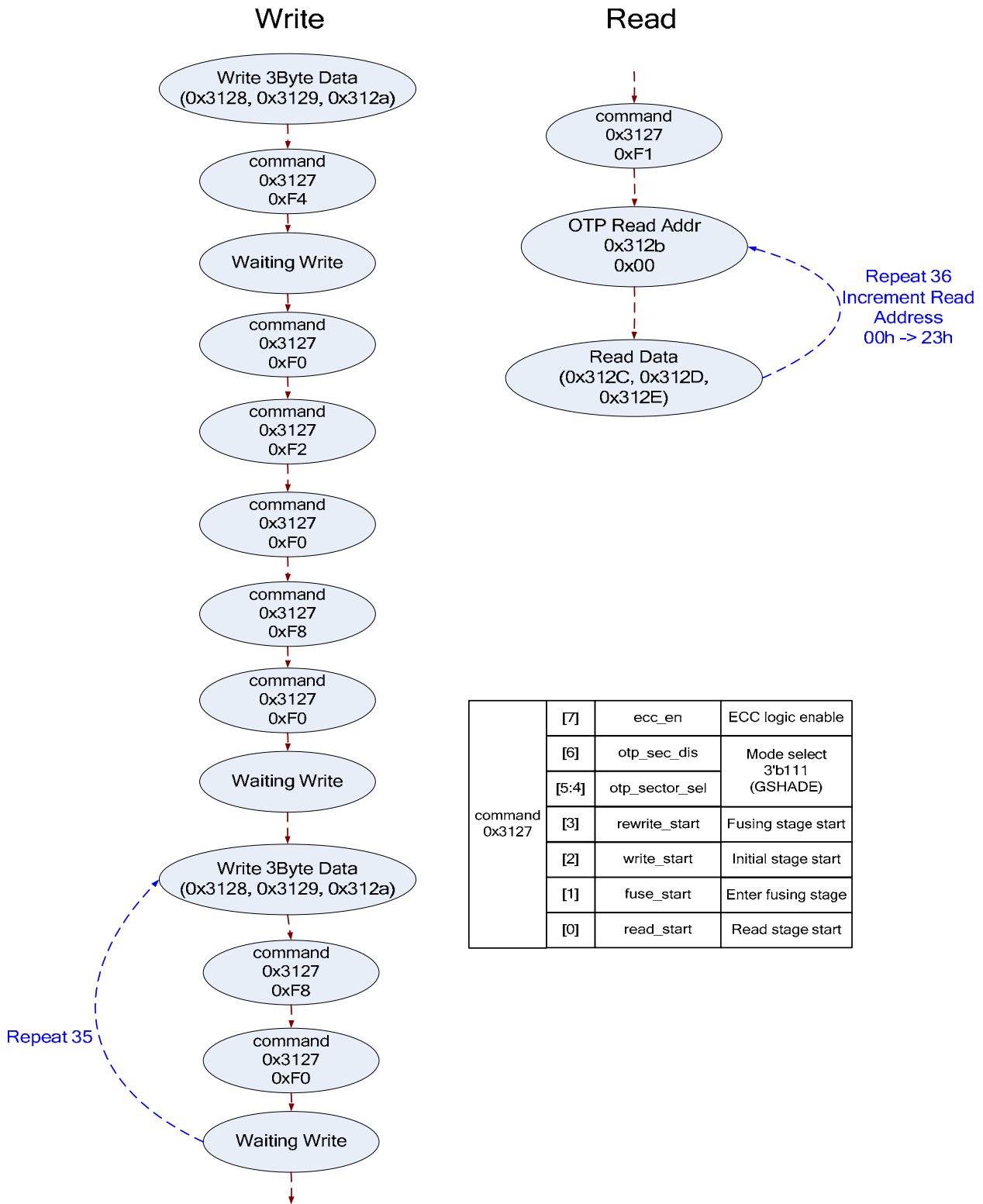


Figure 26. Shading OTP write/read procedure

11 OUTPUT DATA INTERFACE

The S5K3H1GX has the three different way to output the pixel data. The control method is described in "Device Operating modes" on page 3.

11.1 PARALLEL OUTPUT DATA INTERFACE

The S5K3H1Gx can be configured to output the parallel pixel data (Refer to "Device Operating Modes" on page 3). Figure 27, 28 shows the default parallel output timings in terms of pixel clock (PCLK).

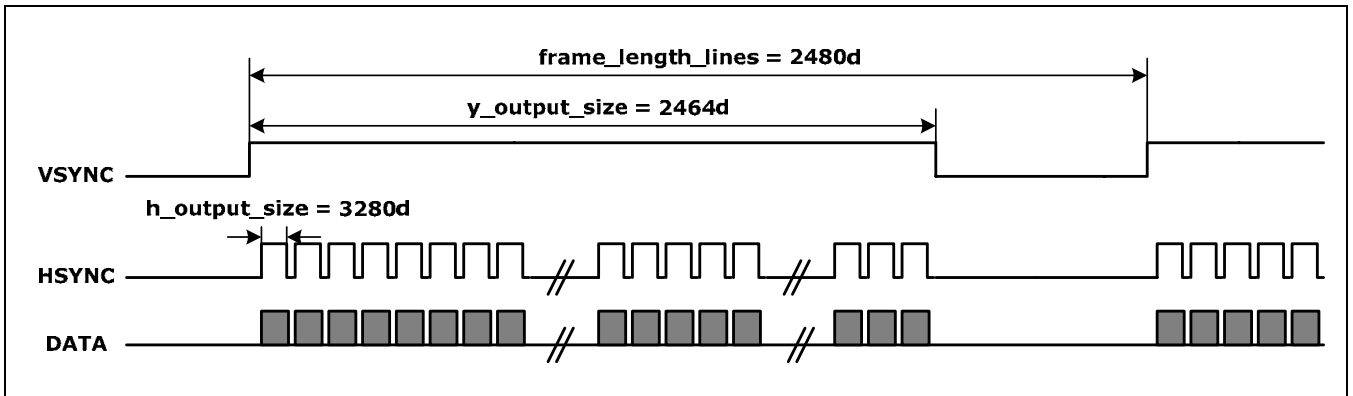


Figure 27. Vertical Timing (Default Case)

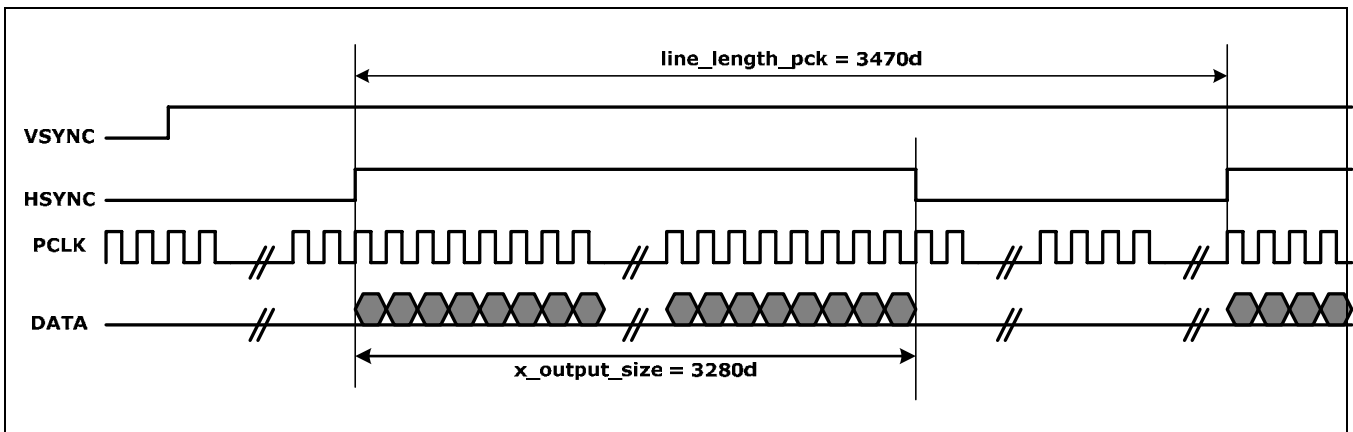


Figure 28. Horizontal Timing (Default Case)

11.2 CSI-2 OUTPUT DATA INTERFACE

The **CSI2_TX** is a transmitter of **CSI-2** (Camera Serial Interface) of **MIPI** (Mobile Industry Processor Interface). **CSI-2** is a unidirectional differential serial interface with data and clock signals between application layer and **PPI** (PHY-Protocol Interface), and it uses **D-PHY** of the **MIPI** Alliance Standard for the physical layer.

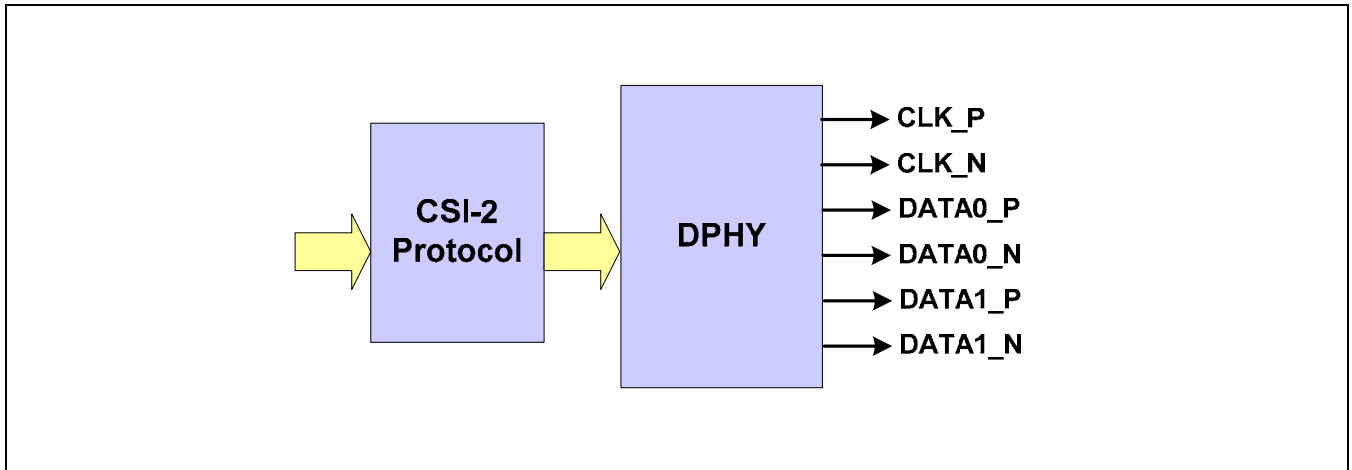


Figure 29. MIPI with 2 Lane DPHY

In order to operate S5K3H1GX data serial interface, registers related CSI2_TX should be programmed properly.

Table 9 : MIPI Control Register

Index	Default	Bits	Mnemonic	R/W	Description
Related MIPI Selector Registers					
0x30C4	0x00	[7:1]	Reserved		
		[0]	SEL_MIPI	RW	MIPI PHY selection (0b: MIPI, 1b: none)
Related Clock Divider Registers					
0x0308	0x00	[15:0]	op_pix_clk_div	RW	Output Pixel Clock Divider
0x0309	0x0A				4 : RAW 8bit, 10-to-8bit Compressed Data @ MIPI 2lane
					5 : RAW 10bit @ MIPI 2lane 6 : RAW 12bit @ MIPI 2lane 8 : RAW 8bit, 10-to-8bit Compressed Data 10 : RAW 10bit 12 : RAW 12bit
0x030A	0x00	[15:0]	op_sys_clk_div	RW	Output System Clock Divider,
0x030B	0x04				MIPI Bit Clock = pll_op_clk / op_sys_clk_div
Related MIPI Registers					
0x3098	0x2B	[7]	outif_enable	RW	output interface for MIPI enable (0b:OFF, 1b:ON)
		[6:1]	Reserved for test		Do Not Change Default Value
0x309A	0x00	[7:1]	Reserved for test		Do Not Change Default Value
		[0]	pack_video_enable	RW	Packer for MIPI Enable (0b:OFF, 1b:ON)

Index	Default	Bits	Mnemonic	R/W	Description
0x30A0	0x03	[7:4]	<i>Reserved for test</i>		Do Not Change Default Value
		[3]	ileaver_types_en_line_end ileaver_types_en_line_start	RW	Line End Short Packet enable (default Off, it need more line_length_pclk for line end packet)
		[2]		RW	Line Start Short Packet enable (default Off, it need more line_length_pclk for line end packet)
		[1:0]	<i>Reserved for test</i>		Do Not Change Default Value
0x30AA	0x00	[7:6]	virtual_channel_line_end	RW	Virtual Channel ID for line end short packet
		[5:4]	virtual_channel_line_start	RW	Virtual Channel ID for line start short packet
		[3:2]	virtual_channel_frame_end	RW	Virtual Channel ID for frame end short packet
		[1:0]	virtual_channel_frame_start	RW	Virtual Channel ID for frame start short packet
0x30AB	0x00	[7:6]	<i>Reserved</i>		
		[5:4]	virtual_channel_video	RW	Virtual Channel ID for video data long packet
		[3:0]	<i>Reserved for test</i>		Do Not Change Default Value
0x30BB	0x02	[7:2]	<i>Reserved for test</i>		Do Not Change Default Value
		[1:0]	number_of_lanes	RW	Numbers of Data Lanes 2'b01 – one lane 2'b10 – two lanes
0x30C1	0x0F	[7:4]	<i>Reserved</i>		
		[3]	DPHY_continuous_clk	RW	0: Non-Continuous Clock 1: Continuous Clock (default)
		[2]	DPHY_enableLane2	RW	DPHY 2 nd data lane power enable, 0: off / 1: on(default)
		[1]	DPHY_enableLane1	RW	DPHY 1 st data lane power enable, 0: off / 1: on(default)
		[0]	DPHY_enableClkLane	RW	DPHY clock lane power enable, 0: off / 1: on(default)
0x30C6	0x30	[7:6]	<i>Reserved</i>		
		[5:0]	adr_compressed_bayer	RW	define data type for 10bit-to-8bit compressed Bayer data
0x30C7	0x08	[7:6]	<i>Reserved</i>		
		[5:4]	esc_ref_div	RW	Escape Clock divider $MCLK / (2^{esc_ref_div}) = \text{Escape Clock} \leq 20\text{MHz}$
		[3:2]	<i>Reserved for test</i>		Do Not Change Default Value
		[1]	DPHY_Enable	RW	DPHY Enable (0b:OFF, 1b:ON)
		[0]	<i>Reserved for test</i>		Do Not Change Default Value
Related DPHY Timing Registers					
0x30BC	0x19	[15:0]	outif_mld_ulpm_rxinit_limit	RW	DPHY T _{WAKEUP} @ DPHY ULPS exit se- quence > 1msec / (MCLK period x 2)
0x30BD	0x64				
0x30CC	0xF0	[7:4]	DPHY_band_ctl	RW	Timing Control for Global operation
		[3:0]	<i>Reserved for test</i>		Do Not Change Default Value
0x3110	0x32	[15:0]	outif_enable_time	R/W	DPHY T _{WAKEUP} @ DPHY Power Up se- quence > 1msec / MCLK period
0x3111	0xC9				

Index	Default	Bits	Mnemonic	R/W	Description
0x3112	0x38	[15:0]	streaming_enable_time	R/W	Streaming delay time ($T_{WAKEUP} + T_{INIT}$) > outif_mld_ulpm_rxinit_limit x 2 + 100usec / MCLK period, > outif_enable_time + 100usec / MCLK period
0x3113	0x00				

11.3 DATA TYPE CONFIGURATION

S5K3H1GX data serial interface supports RAW8, RAW10 and 10bits to 8bits compressed data. The configuration register for data type is **data_format** 16bit register. This should be programmed in order to support RAW8, RAW10 and 10bits to 8bits compressed data Data Type.

Name	Address	Bits	Description
data_format[15:8]	0x0112	[7:0]	MIPI Output Data Format 0x0808 : RAW8
data_format[7:0]	0x0113	[7:0]	0x0A08 : 10bits to 8bits compressed data or RAW8 0x0A0A : RAW10 (default)
adr_compressed_bayer	0x30C6	[5:0]	Define User Defined 8-bit Data Type ID for 10bits-to-8bits Compressed Data (default : 0x30)

11.4 MIPI MULTI-LANE CONTROL

S5K3H1GX MIPI DPHY Transmitter can support 1-data-lane mode and 2-data-lane mode. (Horizontal output size must be a multiple of 8pixels at RAW10 MIPI 2 Lane)

Name	Address	Bits	Description
outif_number_of_lanes	0x30BB	[1:0]	2'b10 : Using 2 Data Lanes (default) 2'b01 : Using 1 Data Lane

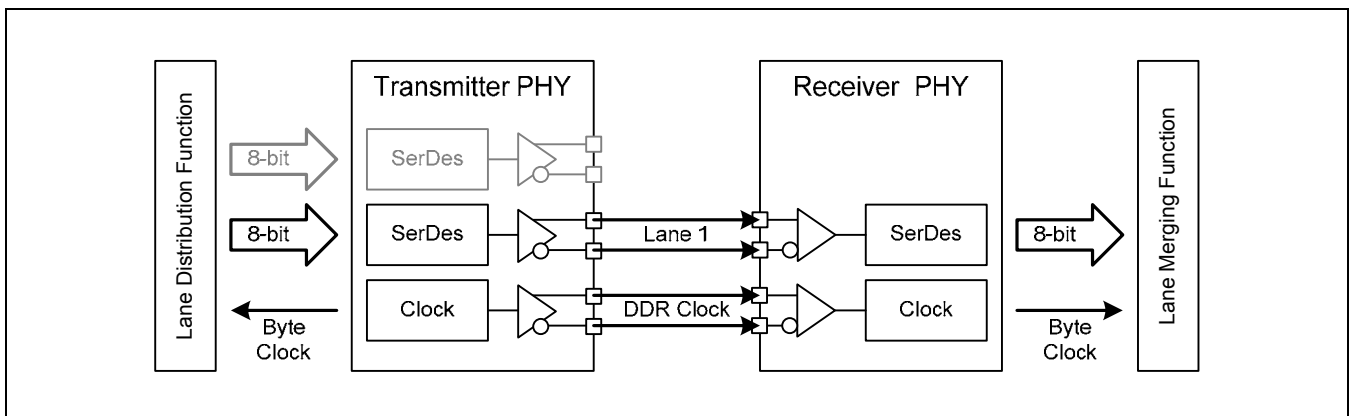


Figure 30. Using 1 Data Lane (outif_number_of_lanes = 01b)

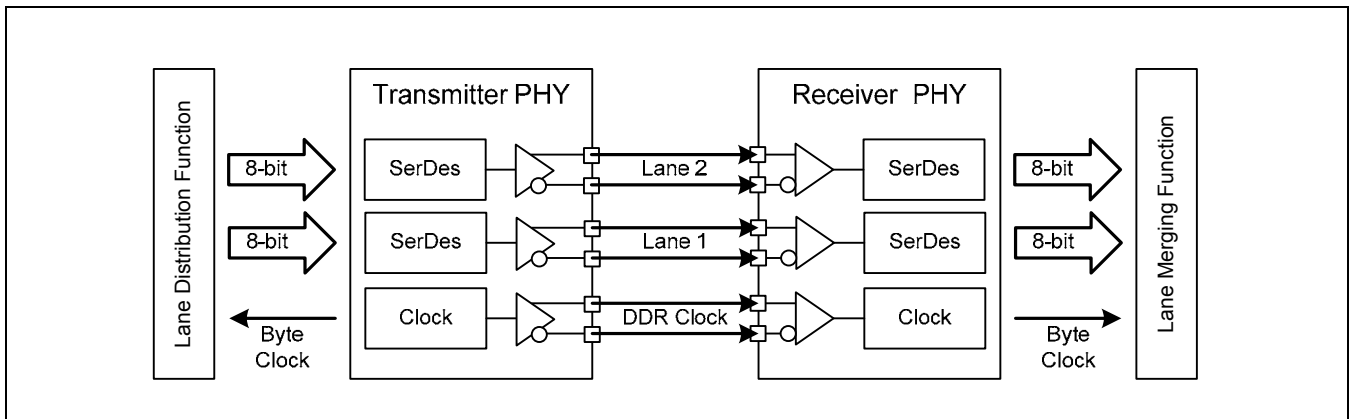


Figure 31. Using 2 Data Lanes (outif_number_of_lanes = 10b)

11.5 MIPI ENABLE, CLOCK DIVIDER CONTROL

Name	Addr	Bits	Description
SEL_MIPI	0x0106	[0]	Select PHY mode, 0: MIPI(default) / 1: none
outif_enable	0x3098	[7]	OUTPUT I/F for CSI2 enable, 0: off(default) / 1: on
pack_video_enable	0x309A	[0]	Enable Video Packer for MIPI, 0: off(default) / 1: on
DPHY_enableLane2	0x30C1	[2]	DPHY 2 nd data lane power enable, 0: off / 1: on(default)
DPHY_enableLane1		[1]	DPHY 1 st data lane power enable, 0: off / 1: on(default)
DPHY_enableCikLane		[0]	DPHY clock lane power enable, 0: off / 1: on(default)
ESC_REF_DIV	0x30C7	[5:4]	Divider for DPHY Escape Clock MCLK / (2 ^{ESC_REF_DIV}) 20MHz
DPHY_Enable		[1]	DPHY power enable, 0: off(default) / 1: on

11.6 ULPS/CONTINUOUS CLOCK CONFIGURATION

S5K3H1GX MIPI Lanes will enter ULPS mode automatically at every software standby mode. DPHY can reduce power consumption by entering ULPS mode.

S5K3H1GX MIPI can support Continuous clock mode and Non-Continuous clock mode. Default mode is Continuous Clock mode, the MIPI Clock Lane remains in high-speed mode between the transmissions of data packets.

At Non-Continuous Clock mode, horizontal line blank time should be increase more to enter LP11 state between the transmissions of data packets.

Name	Addr	Bits	Description
DPHY_continuous_clk	0x30C1	[3]	0: Non-Continuous Clock 1: Continuous Clock (default)

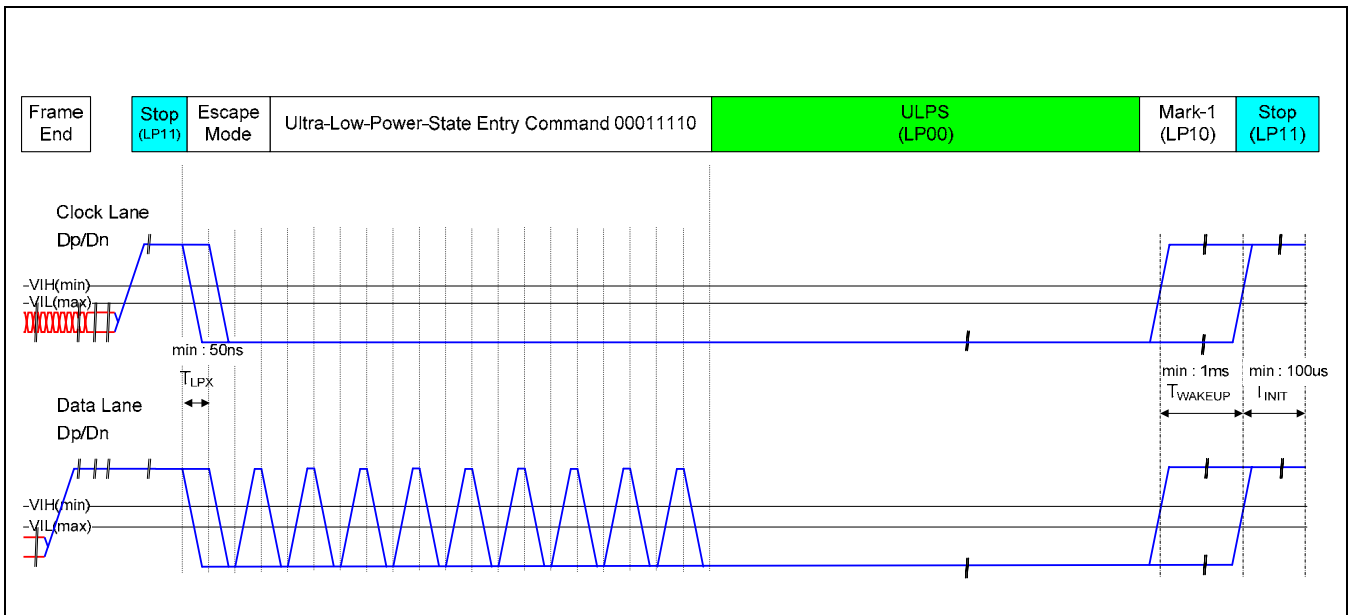


Figure 32. DPHY Ultra-Low-Power State Sequence

11.7 DPHY GLOBAL OPERATION TIMING CONFIGURATION

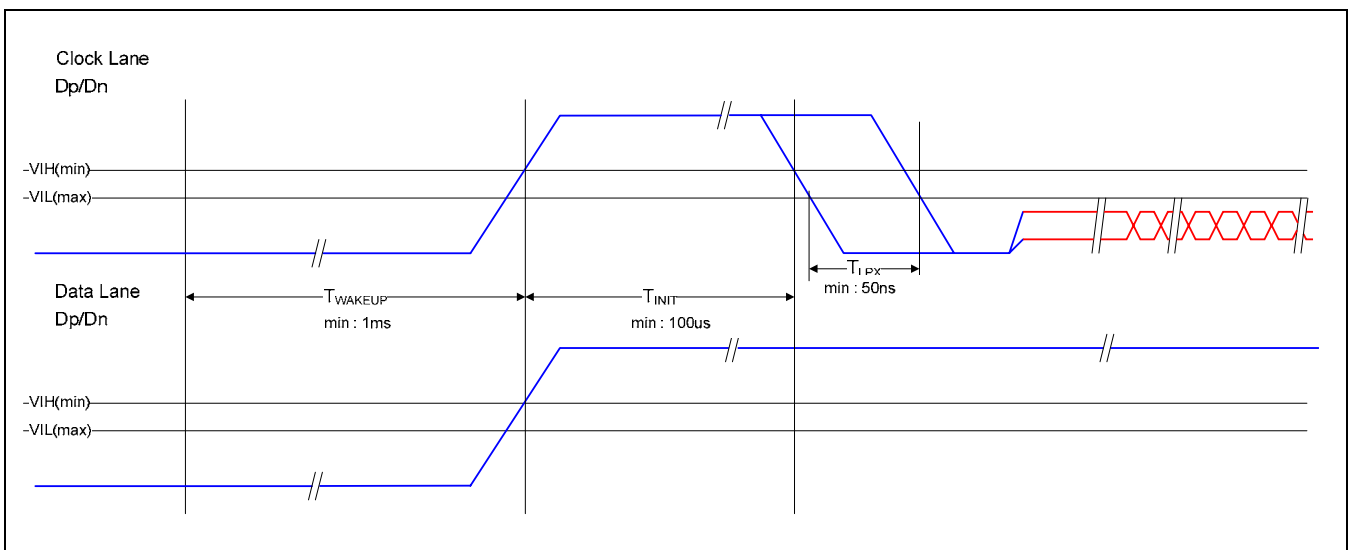


Figure 33. DPHY Global Timing for Initialization

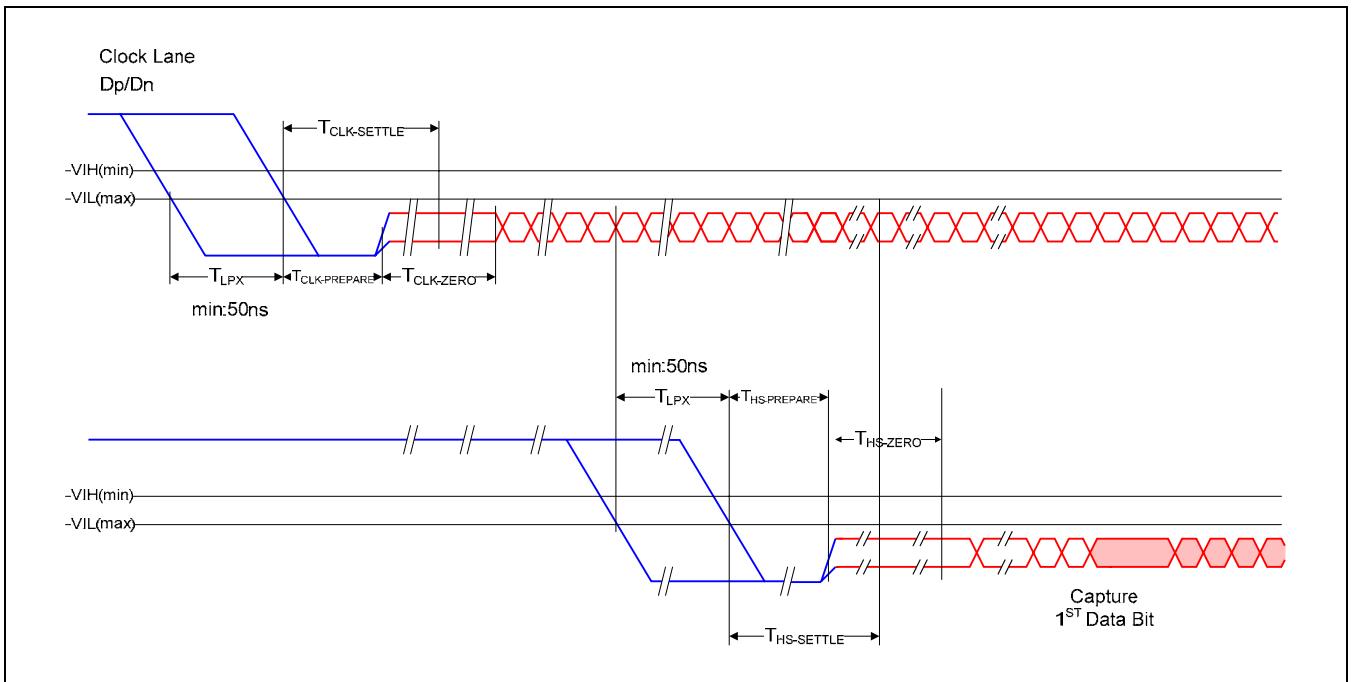


Figure 34. DPHY Global Timing Parameter for HS-TX

S5K3H1GX DPHY can control global operation timing parameter by below registers.

Name	Address	Bits	Description
outif_mld_ulpm_rxinit_limit [15:8]	0x30BC	[7:0]	DPHY T_{WAKEUP} @ DPHY ULPS exit sequence > 1msec / (MCLK period x 2)
outif_mld_ulpm_rxinit_limit [7:0]	0x30BD	[7:0]	
outif_enable_time [15:8]	0x3110	[7:0]	DPHY T_{WAKEUP} @ DPHY Power Up sequence > 1msec / MCLK period
outif_enable_time [7:0]	0x3111	[7:0]	
streaming_enable_time [15:8]	0x3112	[7:0]	Streaming delay time ($T_{WAKEUP} + T_{INIT}$) > outif_mld_ulpm_rxinit_limit x 2 + 100usec / MCLK period, > outif_enable_time + 100usec / MCLK period
streaming_enable_time [7:0]	0x3113	[7:0]	
DPHY_band_ctrl [3:0]	0x30CC	[7:4]	Timing control register for DPHY Global Operation Timing. DPHY_band_ctrl value should be decided by Serial Clock (per lane) Frequency. 0x0 : 80 MHz ~ 100 MHz 0x1 : 100 MHz ~ 120 MHz 0x2 : 120 MHz ~ 170 MHz 0x3 : 170 MHz ~ 220 MHz 0x4 : 220 MHz ~ 270 MHz 0x5 : 270 MHz ~ 320 MHz 0x6 : 320 MHz ~ 390 MHz 0x7 : 390 MHz ~ 450 MHz 0x8 : 450 MHz ~ 510 MHz

Name	Address	Bits	Description
			0x9 : 510 MHz ~ 560 MHz 0xA : 560 MHz ~ 640 MHz 0xB : 640 MHz ~ 690 MHz 0xC : 690 MHz ~ 770 MHz 0xD : 770 MHz ~ 870 MHz 0xE : 870 MHz ~ 950 MHz 0xF : 950 MHz ~ 1 GHz

11.8 EMBEDDED DATA INSERTION

S5K3H1GX MIPI can insert 2 Embedded Data Lines. Its payload data format is same with SMIA Embedded Data.

Name	Address	Bits	Description
serial_emb_on	0x310D	[5]	1'b0 : No Embedded Data Insertion 1'b1 : Embedded Data Insertion (default)
sync_mode	0x3065	[4]	1'b0 : Generate 2 dummy lines for embedded data and image lines (default) 1'b1 : Generate image lines only

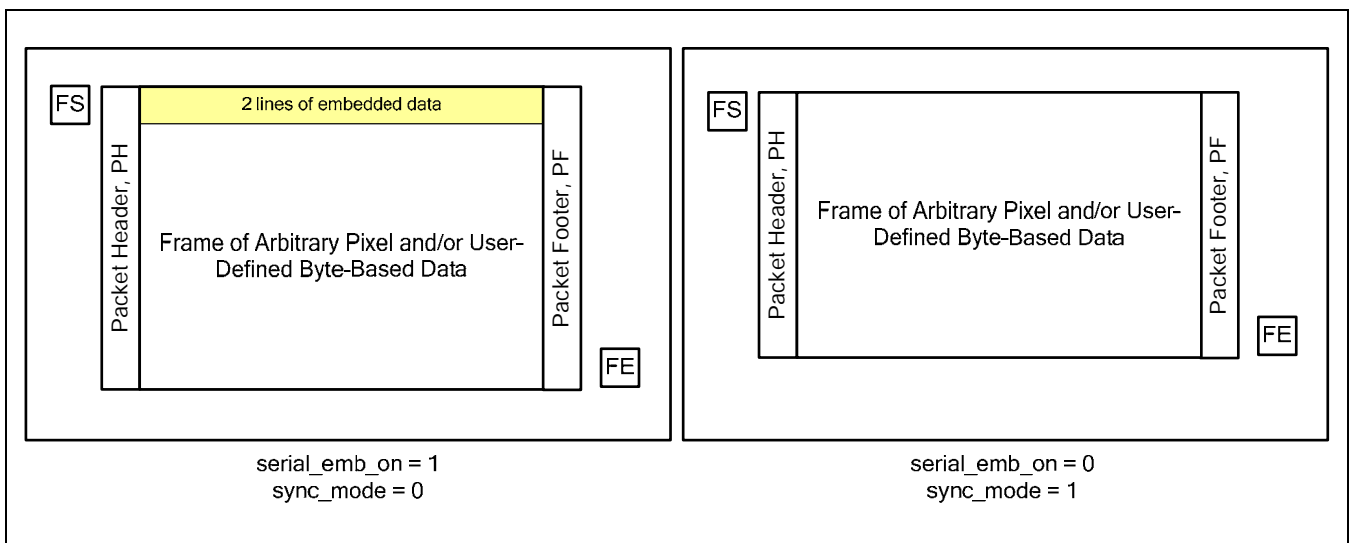


Figure 35. MIPI Embedded Data Line Insertion

12 ELECTRICAL CHARACTERISTICS

Table 10 : Absolute Maximum Rating

Symbol	Description	Min	Typical	Max	Units
VDIG(MAX)	Digital Absolute Max (1)	-0.3	-	2.2	V
VANA(MAX)	Analogue Absolute Max (2)	-0.3	-	4	V
VIO(MAX)	Parallel IO Absolute Max(3)	-0.3	-	3.6	V
VIP(DIG)	Digital Input Voltages (4)	-0.3	-	VANA+0.3	V
VCAP	VCAP Analogue Voltage	-0.3	-	4.2	V
VOTP	OTP Voltage (5)	-0.3	-	5.5	V
TSTR	Storage Temperature	-40	-	85	°C

NOTE

- (1) Digital Supply 1.9V + 0.3V
- (2) Analogue Supply 2.9V + 1.1V
- (3) Parallel IO Supply 2.9V + 0.7V
- (4) Digital Inputs: EXTCLK, XSHUTDOWN, SCL, SDA
- (5) Target(expected) value

Table 11 : Operating Conditions

Symbol	Description	Min	Typical	Max	Units
VDIG	Digital Power Supply(1)	1.7	1.8	1.9	V
VANA	Analogue Power Supply(2)	2.6	2.8	2.9	V
VIO	Parallel IO Supply	1.7	2.8	3.0	V
VIP(DIG)	Digital Input Voltages (3)	0	-	VANA	V
VCAP	VCAP Analogue Voltage	0	-	4.2	V
VOTP	OTP Write Voltage (8)	4.9	5.0	5.1	V
	OTP Read/Normal Voltage		Floating	-	V
TTEST	Test Temperature (4)	21	23	25	°C
TOPT	Optimum Operating Temperature (5)	5	-	40	°C
TOPR	Normal Operating Temperature (6)	-25	-	55	°C
TFUNC	Functional Operating Temperature (7)	-30	-	70	°C

NOTE

- (1) Digital Supply tolerances: 1.8V +/- 100mV
- (2) Analogue Supply Tolerances: Lower limit 2.7V-100mV, Upper Limit: 2.8V+100mV
- (3) Digital Inputs: EXTCLK, XSHUTDOWN, SCL, SDA
- (4) Test Temperature – image quality test conditions
- (5) Optimum Operating Temperature – no visible degradation in image quality
- (6) Normal Operating Temperature – camera produces acceptable images
- (7) Functional Operating Temperature – camera fully functional
- (8) Target(expected) value

Table 12 : DC Characteristics

(V_{ANA} = 2.6V ~ 2.9V, V_{DIG} = 1.8V ± 0.1V, Ta = -30 to +70 °C)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit	
Input voltage(1)	VIH	-	0.7*VDIG	-	-	V	
	VIL	-	-	-	0.3*VDIG		
Input leakage current(1)	IIL	VIN = VANA to VSS	-10	-	10	uA	
High level output voltage (2)	VOH	IOH = -100uA	VDIG-0.2	-	-	V	
		IOH = -2, -4, -6, -8mA	0.7* VDIG	-	-		
Low level output voltage (2)	VOL	IOL = 100uA	-	-	0.2	V	
		IOL = 2, 4, 6, 8mA	-	-	0.3*VDIG		
High-Z output leakage current (3)	IOZ	VOUT = VSS or VDIG	-10	-	10	uA	
Input capacitance(1)	CIN	-	-	-	4	pF	
Differential voltage swing (4)	VOD	Termination resistor=100Ω	100	150	200	mV	
Fixed common mode voltage (4)	VCMF	-	0.8	0.9	1.0	V	
Drive current range (4)	IDRV	Termination resistor=100Ω	0.833	1.5	2	mA	
Drive current variation (4)	DIO	-	-	-	15	%	
Output impedance (4)	RO	-	40	-	140	Ω	
Output impedance mismatch (4)	DRO	-	-	-	10	%	
Supply current (5)	IHWSBA	Hardware standby mode Analog (6)	-	-	5	uA	
	IHWSBD	Hardware standby mode Digital (6)	-	-	200	uA	
	ISWSB1A	Software standby mode Analog(7)	-	-	50	uA	
	ISWSB1D	Software standby mode Digital(7)	-	-	500	uA	
	ISWSB2A	Software standby mode Analog (8)	-	-	50	uA	
	ISWSB2D	Software standby mode Digital (8)	-	-	1	mA	
	ISTRMA	Streaming mode Analog (9) @ 27 fps		-	73.4	90.0	mA
		Streaming mode Analog (10) @ 15fps		-	61.5	82.0	mA
		Streaming mode Analog (11) @ 15fps		-	66.5	85.0	
	ISTRMD2	Streaming mode Digital (9) @ 27 fps		-	62.0	70.0	mA
		Streaming mode Digital (10) @ 15 fps		-	70.0	80.0	mA
Streaming mode Digital (11) @ 15 fps		-	81.3	98.0			

NOTE

- (1) Applied to EXTCLK, XSHUTDOWN, SCL, SDA pins
- (2) Applied to SCL, SDA pins
- (3) Applied to SCL, SDA pins when in High-Z output state
- (4) Applied to DATA+/DATA-, CLK+/CLK- pins
- (5) Summation of currents from V_{DIG} and V_{ANA}
- (6) At 25deg., External clock active or not switching
- (7) External clock not switching
- (8) External clock active (6MHz)
- (9) Readout of the Binning raw Bayer image at the maximum frame rate of MIPI 2lane(27fps)
- (10) Readout of the full raw Bayer image at the 15fps(MIPI 2lane, PCLK=130MHz)
- (11) Readout of the full raw Bayer image at the 15fps(MIPI 2lane, PCLK=194MHz)

Table 13 : AC Characteristics

($V_{ANA} = 2.6V \sim 2.9V$, $V_{DIG} = 1.8V \pm 0.1V$, $T_a = -30$ to $+70$ °C)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
External clock frequency (1)	fXCLK	-	6.0	-	64.0	MHz
External clock duty cycle (1)	fXDUTY	-	45	-	55	%
PLL locking time	tLOCK	-	-	200	1000	us
Random jitter (2)	tRJIT	0101 pattern at 650Mbps	-	150	-	ps(p-p)
Total jitter (3)	tTJIT	PN9 pattern at 650Mbps	-	300	-	ps(p-p)
VOD rise time 20%-80% (4)	tRISE	20%~80% at VOD	300	-	400	ps
VOD fall time 80%-20% (4)	tFALL	80%~20% at VOD	300	-	400	ps
Power-up/down time (5)	tPD	-	-	-	20	us
Power supply rejection ratio 0-100MHz (6)	PSRRL	0~100MHz	30	-	-	dB
Power supply rejection ratio 100-1000MHz (6)	PSRRH	100~1000MHz	10	-	-	dB

NOTE

- (1) Applied to EXTCLK pin
- (2) Jitter generated by PLL only
- (3) Total Jitter generated by PLL, serializer, and SubLVDS driver
- (4) Applied to DATA+/DATA-, CLK+/CLK- pins
- (5) Power-up and down time which SubLVDS driver fully operates and goes into Hi-Z state respectively
- (6) Nominal value for the interference at V_{CM} voltage through digital supply relative to the interference at digital supply over the 0-1GHz operating range. $PSRR = 20 \cdot \log_{10}(V_{DDinterference(peak-to-peak)} / V_{CMinterference(peak-to-peak)})$

Table 14 : Electrostatic Characteristics

Index	Electrostatic Standard			Unit	Remark
	PIN No.	Design Target	Reference Product		
Human Body Model	ALL	2000	2000	V	JESD22-A114-B
Machine Model	ALL	200	250	V	JESD22-A115-A
CDM	ALL	500	1000	V	JESD22-C101C
Latch-up	I-test	$I_{norm} \pm 100mA$	-	mA	JESD78



	V supply over-voltage test	$V_{op,max} \times 1.5$	-	V	
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12.1 TX DRIVER CHARACTERISTICS

Table 15 : TX HS Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
VCMTX	HS transmit static common-mode voltage	150	200	250	mV	1
$ \Delta VCMTX(1,0) $	V_{CMTX} mismatch when output is Differential-1 or Differential-0			5	mV	2
VOD	HS transmit differential voltage	140	200	270	mV	1
$ \Delta VOD $	V_{OD} mismatch when output is Differential-1 or Differential-0			10	mV	2
VOHHS	HS output high voltage			360	mV	1
Zos	Single ended output impedance	40	50	62.5	Ω	
ΔZos	Single ended output impedance mismatch			10	%	

Notes:

1. Value When driving into load impedance anywhere in the Z_{ID} range.
2. It is recommended the implementer minimize ΔVOD and $\Delta VCMTX(1,0)$ in order to minimize radiation and optimize signal integrity.

Table 16 : TX HS Transmitter AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
VCMTX(HF)	Common-level variation above 450MHz			15	mV _{RMS}	
VCMTX(LF)	Common-level variation between 50-450MHz			25	mV _{PEAK}	
t_R and t_F	20% - 80% rise time and fall time			0.3	UI	1
		150			ps	

Notes:

1. UI is equal to $1/(2 \cdot f_h)$. 'f_h' is the highest fundamental frequency for data transmission.

Table 17 : TX LP Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
VOH	Thevenin output high level	1.1	1.2	1.3	V	
VOL	Thevenin output low level	-50		50	mV	
ZOLP	Output impedance of LP transmitter	110			Ω	



Table 18 : TX LP Transmitter AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
TRLP/ TFLP	15%-85% rise time and fall time			25	ns	
TREOT	30%-85% rise time and fall time			35	ns	
TLP-PULSE-TX	Pulse width of the LP exclusive-OR clock	40			ns	
	First LP exclusive –OR clock pulse after Stop state or last pulse before Stop state All other pulse	20			ns	
TLP-PER-TX	Period of the LP exclusive-OR clock	90			ns	
	Slew rate@ C _{LOAD} = 20pF	30		150	mV/ns	
	Slew rate@ C _{LOAD} = 70pF	30		100		
C _{LOAD}	Load capacitance	0		70	pF	

12.2 RECEIVER CHARACTERISTICS

Table 19 : RX HS Receiver DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
VCMRX(DC)	Common-mode voltage HS receive mode	70		330	mV	1
VIDTH	Differential input high threshold			70	mV	
VIDTL	Differential input low threshold	-70			mV	
VIHHS	Single-ended input high voltage			460	mV	1
VILHS	Single-ended input low voltage	-40			mV	1
VTEM-EN	Single-ended threshold for HS termination enable			450	mV	
Z _{ID}	Differential input impedance	80	100	125	Ω	

Notes:

1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz.

Table 20 : RX HS Receiver AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450MHz			100	mV	2
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz - 450MHz	-50		50	mV	1,4
C_{CM}	Common-mode termination			60	pF	3

Notes:

1. Excluding 'static' ground shift of 50mV
2. $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.
3. For Higher bit rate a 14pF capacitor will be needed to meet the common –mode return loss specification.
4. Voltage difference compared to the DC average common-mode potential.

Table 21 : RX LP Receiver DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{IH}	Logic 1 input voltage	880			mV	
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP state			300	mV	
V_{HYST}	Input hysteresis	25			mV	

Table 22 : RX LP Receiver AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
e_{SPIKE}	Input pulse rejection			300	V.ps	1,2,3
T_{MIN-RX}	Minimum plse width response	20			ns	4
V_{INT}	Peak interference amplitude			200	mV	
f_{int}	Interference frequency	450			MHz	

Notes:

1. Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being LP-1 state.
2. An Amplitude less than will not change the receiver state
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
4. An input pulse greater than shall toggle the output.



13 REGISTER DESCRIPTION

The address space is occupied 4-major region as a pre-allocated grouped.

Index	Description
0x0000~0x0FFF	Configuration Registers
0x1000~0x1FFF	Parameter Limit Registers (All registers are Read Only and Static)
0x2000~0x2FFF	Image Statistics Registers (Reserved)
0x3000~0x3FFF	Manufacture Specific Registers

The S5K3H1GX provides Multi-Byte registers index. MS and LS bytes of 8-bit, 16-bit, 24-bit and 32-bit register is defined the valid location. If the width of an register is narrower than the CCI 8-bit, 16-bit, 24-bit or 32-bit register which reports it's value, then the register value is Right aligned within the CCI register and the unused MS bits are padded with zeroes.

Table 15 lists the valid register format

Table 23 : Register Format

Name	Description
8-bit unsigned integer	0 to 255
8-bit signed integer	-128 to 127 Two's complement
16-bit unsigned integer	0 to 65535
16-bit signed integer	-32768 to 32767 Two's complement
16-bit unsigned iReal	0 to 255.99609375
16-bit signed iReal	-128 to 127.9960375
32-bit unsigned iReal	0 to 65535.99998474
32-bit signed iReal	-32768 to 32767.99998474
32-bit IEEE floating-point number	As per IEEE754

Some registers of Configuration Register and Manufacture Specific Registers, 're-timed' parameters, can be changed on a frame blank not to cause a discontinuity within any image and a corrupted image. 're-timed' parameters are also grouped for changing at the same field boundary. A grouped of 're-timed' parameter changes is controlled by a Boolean control parameter, grouped_parameter_hold. While the grouped_parameter_hold signal is in the 'hold' state, 're-timed' parameters can not be changed.

Mnemonic	RW	Reset value	Description
grouped_parameter_hold	RW	0(no-hold)	The grouped parameter hold register disables the consumption of integration, gain and video timing parameters 0 – consume as normal 1 - hold

In some circumstances, re-timing changes to a frame boundary may not be sufficient to prevent corruption to subsequent frames when changing parameters while streaming. The control parameter mask_corrupted_frames allows the host to choose whether to receive these frames. If the parameter is set to 0, the sensor module shall output the corrupt frames. If the parameter is set to 1, the sensor module shall blank all corrupt frames.

Mnemonic	RW	Reset value	Description
mask_corrupted_frames	RW	0	0 - allow corrupted frames 1 - mask corrupted frames

13.1 CONFIGURATION REGISTERS 1

Index	Reset Value	Bits	Mnemonic	RW	Description
0x0000	0x3810	[15:0]	model_id	RO	16-bit Sensor model number
0x0001					
0x0002	0x00	[7:0]	revision_number	RO	Silicon Revision Number
0x0003	0x09	[7:0]	manufacturer_id	RO	Manufacturer ID (dec:9)
0x0004	0x0A	[7:0]	smia_version	RO	9 - SMIA V0.9 10 - SMIA V1.0 11 - SMIA V1.1
0x0005	0xFF	[7:0]	frame_count	RO	8-bit (0-255) Frame counter value (dec:255)
0x0006	0x00	[7:0]	pixel_order	RO	Colour Pixel Order = {6'h00, image_orientation[1:0]} (This register should apply the change of <i>image_orientation</i> .)
0x0007			Reserved		
0x0008	0x0040	[7:0]	data_pedestal	RO	Data pedestal – typically code 64 for 10-bit systems (dec:64)
0x0009					
0x000A					
0x000B					
0x000C	0x0A	[7:0]	pixel_depth	RO	8-bit or 10-bit pixel (dec:10)
0x0040	0x01	[7:0]	frame_format_model_type	RO	
0x0041	0x12	[7:0]	frame_format_model_subtype	RO	
0x0042	0x5CD0	[15:0]	frame_format_descriptor_0	RO	(dec: 3264+16 columns)
0x0043					
0x0044	0x1002	[15:0]	frame_format_descriptor_1	RO	(dec: 2 embedded lines)
0x0045					
0x0046	0x59A0	[15:0]	frame_format_descriptor_2	RO	(dec: 2448+16)
0x0047					
0x0048	0x0000	[15:0]	frame_format_descriptor_3	RO	
0x0049					
0x004A	0x0000	[15:0]	frame_format_descriptor_4	RO	
0x004B					
0x004C	0x0000	[15:0]	frame_format_descriptor_5	RO	
0x004D					
0x004E	0x0000	[15:0]	frame_format_descriptor_6	RO	
0x004F					
0x0050	0x0000	[15:0]	frame_format_descriptor_7	RO	
0x0051					
0x0052	0x0000	[15:0]	frame_format_descriptor_8	RO	
0x0053					
0x0054	0x0000	[15:0]	frame_format_descriptor_9	RO	
0x0055					

Index	Reset Value	Bits	Mnemonic	RW	Description
0x0056	0x0000	[15:0]	frame_format_descriptor_10	RO	
0x0057					
0x0058	0x0000	[15:0]	frame_format_descriptor_11	RO	
0x0059					
0x005A	0x0000	[15:0]	frame_format_descriptor_12	RO	
0x005B					
0x005C	0x0000	[15:0]	frame_format_descriptor_13	RO	
0x005D					
0x005E	0x0000	[15:0]	frame_format_descriptor_14	RO	
0x005F					
0x0080	0x0000	[15:0]	analogue_gain_capability	RO	Analogue Gain Capability 0 - single global analogue gain only 1 - separate channel analogue gains only (Not supported)
0x0081					
0x0082			Reserved	RO	
0x0083					
0x0084	0x0020	[15:0]	analogue_gain_code_min	RO	Minimum recommended analogue gain code (dec: 32) Format : 16-bit unsigned integer
0x0085					
0x0086	0x0200	[15:0]	analogue_gain_code_max	RO	Maximum recommended analogue gain code (dec: 512) Format : 16-bit unsigned integer
0x0087					
0x0088	0x0001	[15:0]	analogue_gain_code_step	RO	Analogue gain code step size (dec:1) Format : 16-bit unsigned integer
0x0089					
0x008A	0x0000	[15:0]	analogue_gain_type	RO	Analogue gain type (dec:0) Format : 16-bit unsigned integer
0x008B					
0x008C	0x0001	[15:0]	analogue_gain_m0	RO	Analogue gain m0 constant (dec:m0=1) Format : 16-bit signed integer
0x008D					
0x008E	0x0000	[15:0]	analogue_gain_c0	RO	Analogue gain c0 constant (dec:c0=0) Format ; 16-bit signed integer
0x008F					
0x0090	0x0000	[15:0]	analogue_gain_m1	RO	Analogue gain m1 constant (dec:m1=0) Format : 16-bit signed integer
0x0091					
0x0092	0x0020	[15:0]	analogue_gain_c1	RO	Analogue gain c1 constant (dec:c1=32) Format : 16-bit signed integer
0x0093					
0x00C0	0x01	[7:0]	data_format_model_type	RO	0x01: 2-Byte Data Format
0x00C1	0x04	[7:0]	data_format_model_subtype	RO	Contains the number of data format descriptors used
0x00C2	0x0A0A	[15:0]	data_format_descriptor_0	RO	ex) 0x0A0A: top 10-bit transmitted as RAW10
0x00C3					
0x00C4	0x0A08	[15:0]	data_format_descriptor_1	RO	ex) 0x0A08: top 10-bit compressed to 8-bit, and transmitted as RAW8
0x00C5					
0x00C6	0x0808	[15:0]	data_format_descriptor_2	RO	ex) 0x0808: top 8-bit transmitted as RAW8
0x00C7					

Index	Reset Value	Bits	Mnemonic	RW	Description
0x00C8	0x0C0C	[15:0]	data_format_descriptor_3	RO	
0x00C9					
0x00CA	0x0000	[15:0]	data_format_descriptor_4	RO	
0x00CB					
0x00CC	0x0000	[15:0]	data_format_descriptor_5	RO	
0x00CD					
0x00CE	0x0000	[15:0]	data_format_descriptor_6	RO	
0x00CF					

Configuration Registers 2

Index	Reset Value	Bits	Register Name	RW	Description
0x0100	0x00	[7:0]	mode_select	RW	Mode Select 0 – Software Standby 1 - Streaming
0x0101	0x00	[7:0]	image_orientation	RW	Image orientation i.e. horizontal mirror and vertical flip
0x0102			Reserved		
0x0103	0x00	[7:0]	software_reset	RW	Software reset
0x0104	0x00	[7:0]	grouped_parameter_hold	RW	The grouped parameter hold register disables the consumption of integration, gain and video timing parameters 0 – consume as normal 1 - hold
0x0105	0x00	[7:0]	mask_corrupted_frames	RW	
0x0110	0x00	[7:0]	Reserved		
0x0111	0x00	[7:0]	Reserved		
0x0112	0x0A0A	[15:0]	Data_format	RW	MIPI Data Format 0x0808: Top 8-b of pixel data, RAW8 0x0A08: 10-b to 8-b compression, RAW8 0x0A0A: Top 10-b of pixel data, RAW10
0x0113					
0x0120	0x00	[7:0]	gain_mode	RW	0 – Global Analogue Gain (Default) 1 – Per Channel Analogue Gain (Not supported)
0x0200	0x06C2	[15:0]	fine_integration_time	RW	Fine integration time (pixels) (dec:1730) Format: 16-bit unsigned integer
0x0201					
0x0202	0x04D8	[15:0]	coarse_integration_time	RW	Coarse integration time (lines) (dec:1240) Format: 16-bit unsigned integer
0x0203					
0x0204	0x0020	[15:0]	analogue_gain_code_global	RW	Global Analogue Gain Code (dec:1x) Format: 16-bit unsigned integer
0x0205					
0x0206	0x0020	[15:0]	Reserved		
0x0207					

Index	Reset Value	Bits	Register Name	RW	Description
0x0208	0x0020	[15:0]	Reserved		
0x0209					
0x020A	0x0020	[15:0]	Reserved		
0x020B					
0x020C	0x0020	[15:0]	Reserved		
0x020D					
0x020E	0x0100	[15:0]	digital_gain_greenR	RW	Green (Red Row) channel digital gain value (1x) Format: 16-bit unsigned iReal
0x020F					
0x0210	0x0100	[15:0]	digital_gain_red	RW	Red channel digital gain value (1x) Format: 16-bit unsigned iReal
0x0211					
0x0212	0x0100	[15:0]	digital_gain_blue	RW	Blue channel digital gain value (1x) Format: 16-bit unsigned iReal
0x0213					
0x0214	0x0100	[15:0]	digital_gain_greenB	RW	Green (Blue Row) channel digital gain value (1x) Format: 16-bit unsigned iReal
0x0215					
0x0300	0x000A	[15:0]	vt_pix_clk_div	RW	Video Timing Pixel Clock Divider (dec:10) Format: 16-bit unsigned integer
0x0301					
0x0302	0x0001	[15:0]	vt_sys_clk_div	RW	Video Timing System Clock Divider Value (dec:1) Format: 16-bit unsigned integer
0x0303					
0x0304	0x0004	[15:0]	pre_pll_clk_div	RW	Pre PLL clock Divider Value (dec:4) Format: 16-bit unsigned integer
0x0305					
0x0306	0x00C8	[15:0]	pll_multiplier	RW	PLL multiplier Value (dec:200) Format: 16-bit unsigned integer
0x0307					
0x0308	0x000A	[15:0]	op_pix_clk_div	RO	Output Pixel Clock Divider (dec:10) Format: 16-bit unsigned integer
0x0309					
0x030A	0x0001	[15:0]	op_sys_clk_div	RW	Output System Clock Divider Value (dec:1) Format: 16-bit unsigned integer
0x030B					
0x0340	0x09B0	[15:0]	frame_length_lines	RW	Frame Length (dec:2480) Format: 16-bit unsigned integer (Lines)
0x0341					
0x0342	0x0D8E	[15:0]	line_length_pck	RW	Line Length (dec:3470) Format: 16-bit unsigned integer (Pixel Clocks)
0x0343					
0x0344	0x0000	[15:0]	x_addr_start	RW	X-address of the top left corner of the visible pixel data (dec:0) Format: 16-bit unsigned integer (Pixels)
0x0345					
0x0346	0x0000	[15:0]	y_addr_start	RW	Y-address of the top left corner of the visible pixel data (dec:0) Format: 16-bit unsigned integer (Lines)
0x0347					
0x0348	0x0CCF	[15:0]	x_addr_end	RW	X-address of the bottom right corner of the visible pixel data (dec:3279) Format: 16-bit unsigned integer (Pixels)
0x0348					

Index	Reset Value	Bits	Register Name	RW	Description
0x034A	0x099F	[15:0]	y_addr_end	RW	Y-address of the bottom right corner of the visible pixel data (dec:2463) Format: 16-bit unsigned integer (Lines)
0x034B					
0x034C	0x0CD0	[15:0]	x_output_size	RW	Width of image data output from the sensor module (dec:3280) Format: 16-bit unsigned integer (Pixels)
0x034D					
0x034E	0x09A0	[15:0]	y_output_size	RW	Height of image data output from the sensor module (dec:2464) Format: 16-bit unsigned integer (Lines)
0x034F					
0x0380	0x0001	[15:0]	x_even_inc	RW	Increment for even pixels – 0, 2, 4 etc (dec:1) Format: 16-bit unsigned integer
0x0381					
0x0382	0x0001	[15:0]	x_odd_inc	RW	Increment for odd pixels – 1, 3, 5 etc (dec:1) Format: 16-bit unsigned integer
0x0383					
0x0384	0x0001	[15:0]	y_even_inc	RW	Increment for even pixels – 0, 2, 4 etc (dec:1) Format: 16-bit unsigned integer
0x0385					
0x0386	0x0001	[15:0]	y_odd_inc	RW	Increment for odd pixels – 1, 3, 5 etc (dec:1) Format: 16-bit unsigned integer
0x0387					

Configuration Registers 3

Index	Reset Value	Bits	Register Name	RW	Description
0x0400	0x0000	[15:0]	Derating_en	RW	0 – De-rating disable 1 – De-rating enable
0x0401					
0x0402	0x0000	[15:0]	Reserved	RW	
0x0403					
0x0404	0x0010	[15:0]	Reserved	RW	
0x0405					
0x0406	0x0010	[15:0]	Reserved	RO	
0x0407					
0x0500	0x0000	[15:0]	compression_mode	RW	1 – DPCM/PCM Compression - Simple Predictor 0 – no compression
0x0501					
0x0600	0x0000	[15:0]	test_pattern_mode	RW	
0x0601					
0x0602	0x0800	[15:0]	test_data_red	RW	(dec:512)
0x0603					
0x0604	0x0800	[15:0]	test_data_greenR	RW	(dec:512)
0x0605					
0x0606	0x0800	[15:0]	test_data_blue	RW	(dec:512)
0x0607					
0x0608	0x0800	[15:0]	test_data_greenB	RW	(dec:512)
0x0609					
0x060A	0x0000	[15:0]	horizontal_cursor_width	RW	(dec:0 – no h-cursor)
0x060B					
0x060C	0x0100	[15:0]	horizontal_cursor_position	RW	(dec:256)
0x060D					
0x060E	0x0000	[15:0]	vertical_cursor_width	RW	(dec:0 – no v-cursor)
0x060F					
0x0610	0x0100	[15:0]	vertical_cursor_position	RW	(dec:256)
0x0611					
0x0700	0x0530	[15:0]	fifo_water_mark_pixels	RW	(dec:1328)
0x0701					

Parameter Limit Registers – [0x1000-0x1FFF] (Read Only and Static)

Index	Reset Value	Bits	Register Name	RW	Description
0x1000	0x0001	[15:0]	integration_time_capability	RO	0 – coarse integration but NO fine integration
0x1001					1 – course and smooth (1 pixel) fine integration
0x1002	0x0000	[15:0]	Reserved	RO	
0x1003					
0x1004	0x0001	[15:0]	coarse_integration_time_min	RO	Lines (dec:1)
0x1005					Format: 16-bits unsigned integer
0x1006	0x0004	[15:0]	coarse_integration_time_max_margin	RO	(Current frame length – current max coarse exp) (dec:4)
0x1007					Format: 16-bits unsigned integer
0x1008	0x0308	[15:0]	fine_integration_time_min	RO	Pixels (dec:776)
0x1009					Format: 16-bits unsigned integer
0x100A	0x0000	[15:0]	fine_integration_time_max_margin	RO	(Current line length – current max fine exp) (dec:0)
0x100B					Format: 16-bits unsigned integer
0x1080	0x0001	[15:0]	digital_gain_capability	RO	0 – none 1 – per channel digital gain
0x1081					
0x1082	0x0000	[15:0]	Reserved	RO	
0x1083					
0x1084	0x0100	[15:0]	digital_gain_min	RO	Minimum recommended digital gain value (dec:1x)
0x1085					Format: 16-bit unsigned 8.8 fixed point number
0x1086	0x0800	[15:0]	digital_gain_max	RO	Maximum recommended digital gain value (dec:8x)
0x1087					Format: 16-bit unsigned 8.8 fixed point number
0x1088	0x0001	[15:0]	digital_gain_step_size	RO	Digital gain step size (dec:1/256)
0x1089					Format: 16-bit unsigned 8.8 fixed point number
0x1100	0x40C0_0000	[31:0]	min_ext_clk_freq_mhz	RO	Minimum external clock frequency
0x1101					Format: IEEE 32-bit float Units: MHz (dec:6MHz)
0x1102					
0x1103					
0x1104	0x41D8_0000	[31:0]	max_ext_clk_freq_mhz	RO	Maximum external clock frequency (dec:27MHz)
0x1105					Format: IEEE 32-bit float Units: MHz
0x1106					
0x1107					
0x1108	0x0001	[15:0]	min_pre_pll_clk_div	RO	Minimum Pre PLL divider value (dec:1)
0x1109					Format: 16-bit unsigned integer
0x110A	0x0008	[15:0]	max_pre_pll_clk_div	RO	Maximum Pre PLL divider value (dec:8)
0x110B					Format: 16-bit unsigned integer

Index	Reset Value	Bits	Register Name	RW	Description
0x110C	0x4040_0000	[31:0]	min_pll_ip_freq_mhz	RO	Minimum PLL input clock frequency (dec:3MHz) Format: IEEE 32-bit float Units: MHz
0x110D					
0x110E					
0x110F					
0x1110	0x40C0_0000	[31:0]	max_pll_ip_freq_mhz	RO	Maximum PLL input clock frequency (dec:6MHz) Format: IEEE 32-bit float Units: MHz
0x1111					
0x1112					
0x1113					
0x1114	0x0052	[15:0]	min_pll_multiplier	RO	Minimum PLL multiplier (dec:82) Format: 16-bit unsigned integer
0x1115					
0x1116	0x014D	[15:0]	max_pll_multiplier	RO	Maximum PLL multiplier (dec:333) Format: 16-bit unsigned integer
0x1117					
0x1118	0x43F5_0000	[31:0]	min_pll_op_freq_mhz	RO	Minimum PLL output clock frequency (dec:490MHz) Format: IEEE 32-bit float Units: MHz
0x1119					
0x111A					
0x111B					
0x111C	0x447A_0000	[31:0]	max_pll_op_freq_mhz	RO	Maximum PLL output clock frequency (dec:1000MHz) Format: IEEE 32-bit float Units: MHz
0x111D					
0x111E					
0x111F					
0x1120	0x0001	[15:0]	min_vt_sys_clk_div	RO	Minimum video timing system clock divider value (dec:1) Format: 16-bit unsigned integer
0x1121					
0x1122	0x0008	[15:0]	max_vt_sys_clk_div	RO	Maximum video timing system clock divider value (dec:8) Format: 16-bit unsigned integer
0x1123					
0x1124	0x4275_0000	[31:0]	min_vt_sys_clk_freq_mhz	RO	Minimum video timing system clock frequency (dec:61.25MHz) Format: IEEE 32-bit float Units: MHz
0x1125					
0x1126					
0x1127					
0x1128	0x447A_0000	[31:0]	max_vt_sys_clk_freq_mhz	RO	Maximum video timing system clock frequency (dec:1000MHz) Format: IEEE 32-bit float Units: MHz
0x1129					
0x112A					
0x112B					
0x112C	0x4124_F5C3	[31:0]	min_vt_pix_clk_freq_mhz	RO	Minimum video timing pixel clock frequency (dec:10.31MHz) Format: IEEE 32-bit float Units: MHz
0x112D					
0x112E					
0x112F					
0x1130	0x42A6_0000	[31:0]	max_vt_pix_clk_freq_mhz	RO	Maximum video timing pixel clock frequency (dec:83MHz) Format: IEEE 32-bit float Units: MHz
0x1131					
0x1132					
0x1133					

Index	Reset Value	Bits	Register Name	RW	Description
0x1134	0x0004	[15:0]	min_vt_pix_clk_div	RO	Minimum video timing pixel clock divider value (dec:4) Format: 16-bit unsigned integer
0x1135					
0x1136	0x000C	[15:0]	max_vt_pix_clk_div	RO	Maximum video timing pixel clock divider value (dec:12) Format: 16-bit unsigned integer
0x1137					
0x1140	0x01FE	[15:0]	min_frame_length_lines	RO	Minimum Frame Length allowed. Value both sensor dependent Units: Lines (dec:510) Format: 16-bit unsigned integer
0x1141					
0x1142	0xFFFF	[15:0]	max_frame_length_lines	RO	Maximum possible number of lines per Frame. (dec:65535) Value sensor dependent Format: 16-bit unsigned integer Units: Lines
0x1143					
0x1144	0x0D8E	[15:0]	min_line_length_pck	RO	Minimum Line Length allowed. Value sensor dependent (dec:3470) Format: 16-bit unsigned integer Units: Pixel Clocks
0x1145					
0x1146	0xAAAA	[15:0]	max_line_length_pck	RO	Maximum possible number of pixel clocks per line. (dec:43690) Value sensor dependent Format: 16-bit unsigned integer Units: Pixel Clocks
0x1147					
0x1148	0x00BE	[15:0]	min_line_blanking_pck	RO	Minimum line blanking time in pixel clocks (dec:190) Format: 16-bit unsigned integer Units: Pixel Clocks
0x1149					
0x114A	0x0010	[15:0]	min_frame_blanking_lines	RO	Minimum frame blanking in video timing lines (dec:16) Format: 16-bit unsigned integer Units: Pixel Clocks
0x114B					
0x1160	0x0001	[15:0]	min_op_sys_clk_div	RO	Minimum output system clock divider value (dec:1) Format: 16-bit unsigned integer
0x1161					
0x1162	0x0008	[15:0]	max_op_sys_clk_div	RO	Maximum output system clock divider value (dec:8) Format: 16-bit unsigned integer
0x1163					
0x1164	0x4275_0000	[31:0]	min_op_sys_ck_clk_freq_mhz	RO	Minimum output system clock frequency (dec:61.25 MHz) Format: IEEE 32-bit float Units: MHz
0x1165					
0x1166					
0x1167					
0x1168	0x447A_0000	[31:0]	max_op_sys_clk_freq_mhz	RO	Maximum output system clock frequency (dec:1000MHz) Format: IEEE 32-bit float Units: MHz
0x1169					
0x116A					
0x116B					

Index	Reset Value	Bits	Register Name	RW	Description
0x116C	0x0008	[15:0]	min_op_pix_clk_div	RO	Minimum output pixel clock divider value (dec:8) Format: 16-bit unsigned integer
0x116D					
0x116E	0x000C	[15:0]	max_op_pix_clk_div	RO	Maximum output pixel clock divider value (dec:12) Format: 16-bit unsigned integer
0x116F					
0x1170	0x40A3_3333	[31:0]	min_op_pix_clk_freq_mhz	RO	Minimum output pixel clock frequency (dec:5.1MHz) Format: IEEE 32-bit float Units: MHz
0x1171					
0x1172					
0x1173					
0x1174	0x42A6_0000	[31:0]	max_op_pix_clk_freq_mhz	RO	Maximum output pixel clock frequency (dec:83MHz) Format: IEEE 32-bit float Units: MHz
0x1175					
0x1176					
0x1177					
0x1180	0x0000	[15:0]	x_addr_min	RO	(dec:0)
0x1181					
0x1182	0x0000	[15:0]	y_addr_min	RO	(dec:0)
0x1183					
0x1184	0x0CCF	[15:0]	x_addr_max	RO	(dec:3279)
0x1185					
0x1186	0x099F	[15:0]	y_addr_max	RO	(dec:2463)
0x1187					
0x1188	0x0100	[15:0]	min_x_output_size	RO	(dec:256)
0x1189					
0x118A	0x00C0	[15:0]	min_y_output_size	RO	(dec:192)
0x118B					
0x118C	0x0CD0	[15:0]	max_x_output_size	RO	(dec:3280)
0x118D					
0x118E	0x09A0	[15:0]	max_y_output_size	RO	(dec:2464)
0x118F					
0x11C0	0x0001	[15:0]	min_even_inc	RO	Minimum Increment for even pixels (dec:1) Format: 16-bit unsigned integer (static)
0x11C1					
0x11C2	0x0009	[15:0]	max_even_inc	RO	Maximum increment for even pixels (dec:15) Format: 16-bit unsigned integer (static)
0x11C3					
0x11C4	0x0001	[15:0]	min_odd_inc	RO	Minimum Increment for odd pixels (dec:1) Format: 16-bit unsigned integer (static)
0x11C5					
0x11C6	0x0009	[15:0]	max_odd_inc	RO	Maximum Increment for odd pixels (dec:15) Format: 16-bit unsigned integer (static)
0x11C7					
0x1200	0x0002	[15:0]	scaling_capability	RO	0 – None 1 – Horizontal 2 – Full (Horizontal & Vertical) Format: 16-bit unsigned integer
0x1201					

Index	Reset Value	Bits	Register Name	RW	Description
0x1202	0x0000	[15:0]	reserved	RO	
0x1203					
0x1204	0x0010	[15:0]	reserved	RO	
0x1205					
0x1206	0x00CA	[15:0]	reserved	RO	
0x1207					
0x1208	0x0010	[15:0]	reserved	RO	
0x1209					
0x120A	0x0010	[15:0]	reserved	RO	
0x120B					
0x1300	0x0001	[15:0]	compression_capability	RW	0 – No Compression 1 – DPCM/PCM Compression
0x1301					
0x1400	0x0144	[15:0]	matrix_element_RedInRed	RO	Colour matrix parameter for Red in Red (dec:1.266) Format: 16-bit signed iReal
0x1401					
0x1402	0xFFA5	[15:0]	matrix_element_GreenInRed	RO	Colour matrix parameter for Green in Red (dec:-0.355) Format: 16-bit signed iReal
0x1403					
0x1404	0x0017	[15:0]	matrix_element_BlueInRed	RO	Colour matrix parameter for Blue in Red (dec:0.09) Format: 16-bit signed iReal
0x1405					
0x1406	0xFF81	[15:0]	matrix_element_RedInGreen	RO	Colour matrix parameter for Red in Green (dec:-0.496) Format: 16-bit signed iReal
0x1407					
0x1408	0x022E	[15:0]	matrix_element_GreenInGreen	RO	Colour matrix parameter for Green in Green (dec:2.180) Format: 16-bit signed iReal
0x1409					
0x140A	0xFF51	[15:0]	matrix_element_BlueInGreen	RO	Colour matrix parameter for Blue in Green (dec:-0.684) Format: 16-bit signed iReal
0x140B					
0x140C	0x0002	[15:0]	matrix_element_RedInBlue	RO	Colour matrix parameter for Red in Blue (dec:0.008) Format: 16-bit signed iReal
0x140D					
0x140E	0xFFB2	[15:0]	matrix_element_GreenInBlue	RO	Colour matrix parameter for Green in Blue (dec:-0.305) Format: 16-bit signed iReal
0x140F					
0x1410	0x014C	[15:0]	matrix_element_BlueInBlue	RO	Colour matrix parameter for Blue in Blue (dec:1.297) Format: 16-bit signed iReal
0x1411					
0x1500	0xCE0	[15:0]	fifo_size_pixels	RO	FIFO size in pixels (0 = no FIFO present) (dec:3296) Format : 16-bit unsigned integer
0x1501					

Manufacturer Specific Registers – [0x3000-0x3FFF] (Read/Write)

Index	Reset Value	Bits	Register Name	RW	Description
0x3000	0x07	[7:0]	Reserved	RW	
0x3001	0x05	[7:0]	Reserved	RW	
0x3002	0x19	[7:0]	Reserved	RW	
0x3003	0x1E	[7:0]	Reserved	RW	
0x3004	0x46	[7:0]	Reserved	RW	
0x3005	0x1E	[7:0]	Reserved	RW	
0x3006	0x64	[7:0]	Reserved	RW	
0x3007	0x06	[7:0]	Reserved	RW	
0x3008	0x5A	[7:0]	Reserved	RW	
0x3009	0x5A	[7:0]	Reserved	RW	
0x300A	0x2D	[7:0]	Reserved	RW	
0x300B	0x28	[7:0]	Reserved	RW	
0x300C	0x28	[7:0]	Reserved	RW	
0x300D	0x02	[7:0]	Reserved	RW	
0x300E	0x39	[7:0]	Reserved	RW	
0x300F	0x00	[7:0]	Reserved	RW	
0x3010	0x80	[7:0]	Reserved	RW	
0x3011	0x49	[7:0]	Reserved	RW	
0x3012	0x80	[7:0]	Reserved	RW	
0x3013	0x10	[7:0]	Reserved	RW	
0x3014	0x80	[7:0]	Reserved	RW	
0x3015	0x00	[7:0]	Reserved	RW	
0x3016	0x3C	[7:0]	Reserved	RW	
0x3017	0x74	[7:0]	Reserved	RW	
0x3018	0x00	[7:0]	Reserved	RW	
0x3019	0x08	[7:0]	Reserved	RW	
0x301A	0x77	[7:0]	Reserved	RW	
0x301B	0x06	[7:0]	Reserved	RW	
0x301C	0xD4	[7:0]	Reserved	RW	
0x301D	0x00	[7:0]	Reserved	RW	
0x301E	0x00	[7:0]	Reserved	RW	
0x301F	0x00	[7:0]	Reserved	RW	
0x3020	0x00	[7:0]	Reserved	RW	
0x3021	0x44	[7:0]	Reserved	RW	
0x3022	0x1F	[7:0]	Reserved	RW	
0x3023	0x08	[7:0]	Reserved	RW	
0x3024	0x08	[7:0]	Reserved	RW	
0x3025	0x08	[7:0]	Reserved	RW	
0x3026	0x08	[7:0]	Reserved	RW	
0x3027	0x00	[7:0]	Reserved	RW	
0x3028	0x41	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x3029	0x00	[7:0]	Reserved	RW	
0x302A	0x10	[7:0]	Reserved	RW	
0x302B	0x05	[7:0]	Reserved	RW	
0x302C	0x00	[7:0]	Reserved	RW	
0x302D	0x01	[7:0]	Reserved	RW	
0x302E	0x00	[7:0]	Reserved	RW	
0x302F	0x00	[7:0]	Reserved	RW	
0x3030	0x00	[7:0]	Reserved	RW	
0x3031	0x14	[7:0]	Reserved	RW	
0x3032	0x46	[7:0]	Reserved	RW	
0x3033	0x00	[7:0]	Reserved	RW	
0x3034	0x20	[7:0]	Reserved	RW	
0x3035	0xBB	[7:0]	Reserved	RW	
0x3036	0xB0	[7:0]	Reserved	RW	
0x3037	0x00	[7:0]	Reserved	RW	
0x3038	0x00	[7:0]	Reserved	RW	
0x3039	0x00	[7:0]	Reserved	RW	
0x303A	0x00	[7:0]	Reserved	RW	
0x303B	0x00	[7:0]	Reserved	RW	
0x303C	0x00	[7:0]	Reserved	RW	
0x303D	0x00	[7:0]	Reserved	RW	
0x303E	0x00	[7:0]	Reserved	RW	
0x303F	0x00	[7:0]	Reserved	RW	
0x3040	0x00	[7:0]	Reserved	RW	
0x3041	0x00	[7:0]	Reserved	RW	
0x3042	0x00	[7:0]	Reserved	RW	
0x3043	0x00	[7:0]	Reserved	RW	
0x3044	0x00	[7:0]	Reserved	RW	
0x3045	0x00	[7:0]	Reserved	RW	
0x3046	0x00	[7:0]	Reserved	RW	
0x3047	0x04	[7:0]	Reserved	RW	
0x3048	0xE2	[7:0]	Reserved	RW	
0x3049	0x00	[7:0]	Reserved	RW	
0x304A	0x00	[7:0]	Reserved	RW	
0x304B	0x00	[7:0]	Reserved	RW	
0x304C	0x00	[7:0]	Reserved	RW	
0x304D	0x00	[7:0]	Reserved	RW	
0x304E	0x40	[7:0]	Reserved	RW	
0x304F	0x01	[7:0]	Reserved	RW	
0x3050	0x00	[7:0]	Reserved	RW	
0x3051	0x00	[7:0]	Reserved	RW	
0x3052	0x00	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x3053	0xDF	[7:0]	Reserved	RW	
0x3054	0x11	[7:0]	Reserved	RW	
0x3055	0x20	[7:0]	Reserved	RW	
0x3056	0x20	[7:0]	Reserved	RW	
0x3057	0x00	[7:0]	Reserved	RW	
0x3058	0x00	[7:0]	Reserved	RW	
0x3059	0x00	[7:0]	Reserved	RW	
0x305A	0x00	[7:0]	Reserved	RW	
0x305B	0x00	[7:0]	Reserved	RW	
0x305C	0x00	[7:0]	Reserved	RW	
0x305D	0x00	[7:0]	Reserved	RW	
0x305E	0x00	[7:0]	Reserved	RW	
0x305F	0x00	[7:0]	Reserved	RW	
0x3060	0x00	[7:0]	Reserved	RW	
0x3061	0x20	[7:0]	Reserved	RW	
0x3062	0x10	[7:0]	Reserved	RW	
0x3063	0x20	[7:0]	Reserved	RW	
0x3064	0x10	[7:0]	Reserved	RW	
0x3065	0x05	[7:0]	Reserved	RW	
0x3066	0x00	[7:0]	Reserved	RW	
0x3067	0x00	[7:0]	Reserved	RW	
0x3068	0x00	[7:0]	Reserved	RW	
0x3069	0x01	[7:0]	Reserved	RW	
0x306A	0x00	[7:0]	Reserved	RW	
0x306B	0x08	[7:0]	Reserved	RW	
0x306C	0x00	[7:0]	Reserved	RW	
0x306D	0x00	[7:0]	Reserved	RW	
0x306E	0x00	[7:0]	Reserved	RW	
0x306F	0x20	[7:0]	Reserved	RW	
0x3070	0x00	[7:0]	Reserved	RW	
0x3071	0x88	[7:0]	Reserved	RW	
0x3072	0x26	[7:0]	Reserved	RW	
0x3073	0x2E	[7:0]	Reserved	RW	
0x3074	0x6A	[7:0]	Reserved	RW	
0x3075	0x2E	[7:0]	Reserved	RW	
0x3076	0x98	[7:0]	Reserved	RW	
0x3077	0x09	[7:0]	Reserved	RW	
0x3078	0x88	[7:0]	Reserved	RW	
0x3079	0x88	[7:0]	Reserved	RW	
0x307A	0x44	[7:0]	Reserved	RW	
0x307B	0x41	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x307C	0x41	[7:0]	Reserved	RW	
0x307D	0x05	[7:0]	Reserved	RW	
0x307E	0x03	[7:0]	Reserved	RW	
0x307F	0x30	[7:0]	Reserved	RW	
0x3080	0x03	[7:0]	Reserved	RW	
0x3081	0xB0	[7:0]	Reserved	RW	
0x3082	0x02	[7:0]	Reserved	RW	
0x3083	0xB0	[7:0]	Reserved	RW	
0x3084	0x00	[7:0]	Reserved	RW	
0x3085	0x01	[7:0]	Reserved	RW	
0x3086	0x03	[7:0]	Reserved	RW	
0x3087	0x34	[7:0]	Reserved	RW	
0x3088	0x01	[7:0]	Reserved	RW	
0x3089	0x00	[7:0]	Reserved	RW	
0x308A	0x00	[7:0]	Reserved	RW	
0x308B	0x0C	[7:0]	Reserved	RW	
0x308C	0x00	[7:0]	Reserved	RW	
0x308D	0x00	[7:0]	Reserved	RW	
0x308E	0x00	[7:0]	Reserved	RW	
0x308F	0x00	[7:0]	Reserved	RW	
0x3090	0x18	[7:0]	Reserved	RW	
0x3091	0x00	[7:0]	Reserved	RW	
0x3092	0x08	[7:0]	Reserved	RW	
0x3093	0x08	[7:0]	Reserved	RW	
0x3094	0x00	[7:0]	Reserved	RW	
0x3095	0x00	[7:0]	Reserved	RW	
0x3096	0x00	[7:0]	Reserved	RW	
0x3097	0x2B	[7:0]	Reserved	RW	
0x3098	0x80	[7:0]	Reserved	RW	
0x3099	0x80	[7:0]	Reserved	RW	
0x309A	0x00	[7:0]	Reserved	RW	
0x309B	0x00	[7:0]	Reserved	RW	
0x309C	0xBF	[7:0]	Reserved	RW	
0x309D	0x00	[7:0]	Reserved	RW	
0x309E	0x01	[7:0]	Reserved	RW	
0x309F	0x04	[7:0]	Reserved	RW	
0x30A0	0x03	[7:0]	Reserved	RW	
0x30A1	0x10	[7:0]	Reserved	RW	
0x30A2	0x04	[7:0]	Reserved	RW	
0x30A3	0x00	[7:0]	Reserved	RW	
0x30A4	0x00	[7:0]	Reserved	RW	
0x30A5	0x00	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x30A6	0x00	[7:0]	Reserved	RW	
0x30A7	0x00	[7:0]	Reserved	RW	
0x30A8	0x00	[7:0]	Reserved	RW	
0x30A9	0x00	[7:0]	Reserved	RW	
0x30AA	0x00	[7:0]	Reserved	RW	
0x30AB	0x00	[7:0]	Reserved	RW	
0x30AC	0x0A	[7:0]	Reserved	RW	
0x30AD	0x0B	[7:0]	Reserved	RW	
0x30AE	0x0C	[7:0]	Reserved	RW	
0x30AF	0x0D	[7:0]	Reserved	RW	
0x30B0	0x2E	[7:0]	Reserved	RW	
0x30B1	0x2D	[7:0]	Reserved	RW	
0x30B2	0x00	[7:0]	Reserved	RW	
0x30B3	0x00	[7:0]	Reserved	RW	
0x30B4	0x00	[7:0]	Reserved	RW	
0x30B5	0x00	[7:0]	Reserved	RW	
0x30B6	0x00	[7:0]	Reserved	RW	
0x30B7	0x00	[7:0]	Reserved	RW	
0x30B8	0x00	[7:0]	Reserved	RW	
0x30B9	0x00	[7:0]	Reserved	RW	
0x30BA	0x00	[7:0]	Reserved	RW	
0x30BB	0x02	[7:0]	Reserved	RW	
0x30BC	0x19	[7:0]	Reserved	RW	
0x30BD	0x64	[7:0]	Reserved	RW	
0x30BE	0x0F	[7:0]	Reserved	RW	
0x30C0	0x00	[7:0]	Reserved	RW	
0x30C1	0x0F	[7:0]	Reserved	RW	
0x30C2	0x00	[7:0]	Reserved	RW	
0x30C3	0x00	[7:0]	Reserved	RW	
0x30C4	0x00	[7:0]	Reserved	RW	
0x30C5	0x00	[7:0]	Reserved	RW	
0x30C6	0x30	[7:0]	Reserved	RW	
0x30C7	0x08	[7:0]	Reserved	RW	
0x30C8	0x00	[7:0]	Reserved	RW	
0x30C9	0x00	[7:0]	Reserved	RW	
0x30CA	0x00	[7:0]	Reserved	RW	
0x30CB	0x00	[7:0]	Reserved	RW	
0x30CC	0xF0	[7:0]	Reserved	RW	
0x30CD	0x00	[7:0]	Reserved	RW	
0x30CE	0x00	[7:0]	Reserved	RW	
0x30CF	0x00	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x30D0	0x00	[7:0]	Reserved	RW	
0x30D1	0x00	[7:0]	Reserved	RW	
0x30D2	0x00	[7:0]	Reserved	RW	
0x30D3	0x00	[7:0]	Reserved	RW	
0x30D4	0x08	[7:0]	Reserved	RW	
0x30D5	0x10	[7:0]	Reserved	RW	
0x30D6	0x04	[7:0]	Reserved	RW	
0x30D7	0x0C	[7:0]	Reserved	RW	
0x30D8	0xD0	[7:0]	Reserved	RW	
0x30D9	0x09	[7:0]	Reserved	RW	
0x30DA	0xA0	[7:0]	Reserved	RW	
0x30DB	0x00	[7:0]	Reserved	RW	
0x30DC	0x00	[7:0]	Reserved	RW	
0x30DD	0x10	[7:0]	Reserved	RW	
0x30DE	0x05	[7:0]	Reserved	RW	
0x30DF	0x30	[7:0]	Reserved	RW	
0x30E0	0x0A	[7:0]	Reserved	RW	
0x30E1	0x01	[7:0]	Reserved	RW	
0x30E2	0x04	[7:0]	Reserved	RW	
0x30E3	0x00	[7:0]	Reserved	RW	
0x30E4	0xC8	[7:0]	Reserved	RW	
0x30E5	0x0A	[7:0]	Reserved	RW	
0x30E6	0x01	[7:0]	Reserved	RW	
0x30E7	0x00	[7:0]	Reserved	RW	
0x30E8	0x00	[7:0]	Reserved	RW	
0x30E9	0x09	[7:0]	Reserved	RW	
0x30EA	0xAC	[7:0]	Reserved	RW	
0x30EB	0x0D	[7:0]	Reserved	RW	
0x30EC	0x8E	[7:0]	Reserved	RW	
0x30ED	0x00	[7:0]	Reserved	RW	
0x30EE	0x00	[7:0]	Reserved	RW	
0x30EF	0x00	[7:0]	Reserved	RW	
0x30F0	0x00	[7:0]	Reserved	RW	
0x30F1	0x00	[7:0]	Reserved	RW	
0x30F2	0x00	[7:0]	Reserved	RW	
0x30F3	0x0C	[7:0]	Reserved	W/flag	
0x30F4	0xCF	[7:0]	Reserved	W/flag	
0x30F5	0x00	[7:0]	Reserved	RW	
0x30F6	0x00	[7:0]	Reserved	RW	
0x30F7	0x09	[7:0]	Reserved	RW	
0x30F8	0x9F	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x30F9	0x01	[7:0]	Reserved	RW	
0x30FA	0x01	[7:0]	Reserved	RW	
0x30FB	0x01	[7:0]	Reserved	RW	
0x30FC	0x01	[7:0]	Reserved	RW	
0x30FD	0x00	[7:0]	Reserved	RW	
0x30FE	0x20	[7:0]	Reserved	RW	
0x30FF	0x20	[7:0]	Reserved	RW	
0x3100	0x00	[7:0]	Reserved	RW	
0x3101	0x20	[7:0]	Reserved	RW	
0x3102	0x00	[7:0]	Reserved	RW	
0x3103	0x20	[7:0]	Reserved	RW	
0x3104	0x00	[7:0]	Reserved	RW	
0x3105	0x20	[7:0]	Reserved	RW	
0x3106	0x00	[7:0]	Reserved	RW	
0x3107	0x20	[7:0]	Reserved	RW	
0x3108	0x00	[7:0]	Reserved	RW	
0x3109	0x00	[7:0]	Reserved	RW	
0x310A	0x00	[7:0]	Reserved	RW	
0x310B	0x00	[7:0]	Reserved	RW	
0x310C	0x40	[7:0]	Reserved	RW	
0x310D	0xA6	[7:0]	Reserved	RW	
0x310E	0x00	[7:0]	Reserved	RW	
0x310F	0x00	[7:0]	Reserved	RW	
0x3110	0x32	[7:0]	Reserved	RW	
0x3111	0xC9	[7:0]	Reserved	RW	
0x3112	0x38	[7:0]	Reserved	RW	
0x3113	0x00	[7:0]	Reserved	RW	
0x3114	0x00	[7:0]	Reserved	RW	
0x3115	0x00	[7:0]	Reserved	RW	
0x3116	0x00	[7:0]	Reserved	RW	
0x3117	0x00	[7:0]	Reserved	RW	
0x3118	0x00	[7:0]	Reserved	RO	
0x3119	0x00	[7:0]	Reserved	RO	
0x311A	0x40	[7:0]	Reserved	RO	
0x311B	0x02	[7:0]	Reserved	RO	
0x311C	0x40	[7:0]	Reserved	RO	
0x311D	0x00	[7:0]	Reserved	RO	
0x311E	0x12	[7:0]	Reserved	RO	
0x311F	0x85	[7:0]	Reserved	RO	
0x3120	0xF6	[7:0]	Reserved	RO	
0x3121	0x00	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x3122	0x00	[7:0]	Reserved	RO	
0x3123	0x00	[7:0]	Reserved	RO	
0x3124	0x00	[7:0]	Reserved	RO	
0x3125	0x95	[7:0]	Reserved	RW	
0x3126	0x02	[7:0]	Reserved	RW	
0x3127	0xB0	[7:0]	Reserved	RW	
0x3128	0x00	[7:0]	Reserved	RW	
0x3129	0x00	[7:0]	Reserved	RW	
0x312A	0x00	[7:0]	Reserved	RW	
0x3130	0x00	[7:0]	Reserved	RW	
0x3131	0x00	[7:0]	Reserved	RW	
0x3132	0x00	[7:0]	Reserved	RW	
0x3133	0x00	[7:0]	Reserved	RW	
0x3134	0x00	[7:0]	Reserved	RW	
0x3135	0x00	[7:0]	Reserved	RW	
0x3136	0x00	[7:0]	Reserved	RW	
0x3137	0x00	[7:0]	Reserved	RW	
0x3138	0x00	[7:0]	Reserved	RW	
0x3139	0x00	[7:0]	Reserved	RW	
0x313A	0x00	[7:0]	Reserved	RW	
0x313B	0x00	[7:0]	Reserved	RW	
0x313C	0x00	[7:0]	Reserved	RW	
0x313D	0x00	[7:0]	Reserved	RW	
0x313E	0x00	[7:0]	Reserved	RW	
0x313F	0x00	[7:0]	Reserved	RW	
0x3140	0x00	[7:0]	Reserved	RW	
0x3141	0x00	[7:0]	Reserved	RW	
0x3142	0x00	[7:0]	Reserved	RW	
0x3143	0x00	[7:0]	Reserved	RW	
0x3144	0x00	[7:0]	Reserved	RW	
0x3145	0x00	[7:0]	Reserved	RW	
0x3146	0x00	[7:0]	Reserved	RW	
0x3147	0x00	[7:0]	Reserved	RW	
0x3148	0x00	[7:0]	Reserved	RO	
0x3149	0x00	[7:0]	Reserved	RO	
0x314A	0x00	[7:0]	Reserved	RO	
0x314B	0x00	[7:0]	Reserved	RO	
0x314C	0x00	[7:0]	Reserved	RO	
0x3150	0x07	[7:0]	Reserved	RW	
0x3151	0xB0	[7:0]	Reserved	RW	
0x3152	0x09	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x3153	0xB0	[7:0]	Reserved	RW	
0x3154	0x05	[7:0]	Reserved	RW	
0x3155	0xB0	[7:0]	Reserved	RW	
0x3156	0x60	[7:0]	Reserved	RW	
0x3157	0x04	[7:0]	Reserved	RW	
0x3158	0x01	[7:0]	Reserved	RW	
0x3159	0x1D	[7:0]	Reserved	RW	
0x315A	0xB0	[7:0]	Reserved	RW	
0x315B	0x04	[7:0]	Reserved	RW	
0x315C	0x01	[7:0]	Reserved	RW	
0x315D	0x41	[7:0]	Reserved	RW	
0x315E	0x00	[7:0]	Reserved	RW	
0x315F	0x00	[7:0]	Reserved	RW	
0x3160	0x00	[7:0]	Reserved	RW	
0x3161	0x00	[7:0]	Reserved	RW	
0x3162	0x00	[7:0]	Reserved	RW	
0x3163	0x00	[7:0]	Reserved	RW	
0x3164	0x00	[7:0]	Reserved	RW	
0x3165	0x00	[7:0]	Reserved	RW	
0x3166	0x00	[7:0]	Reserved	RW	
0x3167	0x00	[7:0]	Reserved	RW	
0x3168	0x00	[7:0]	Reserved	RW	
0x3169	0x00	[7:0]	Reserved	RW	
0x316A	0x00	[7:0]	Reserved	RW	
0x316B	0x00	[7:0]	Reserved	RW	
0x316C	0x00	[7:0]	Reserved	RW	
0x316D	0x00	[7:0]	Reserved	RW	
0x316E	0x00	[7:0]	Reserved	RW	
0x316F	0x00	[7:0]	Reserved	RW	
0x3170	0x00	[7:0]	Reserved	RW	
0x3171	0x00	[7:0]	Reserved	RW	
0x3172	0x01	[7:0]	Reserved	RW	
0x3173	0x34	[7:0]	Reserved	RW	
0x3174	0x01	[7:0]	Reserved	RW	
0x3175	0x00	[7:0]	Reserved	RW	
0x3176	0x00	[7:0]	Reserved	RW	
0x3177	0x00	[7:0]	Reserved	RW	
0x3178	0x00	[7:0]	Reserved	RW	
0x3179	0x00	[7:0]	Reserved	RW	
0x317A	0x00	[7:0]	Reserved	RW	
0x317B	0x00	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x317C	0x00	[7:0]	Reserved	RW	
0x317D	0x00	[7:0]	Reserved	RW	
0x317E	0x00	[7:0]	Reserved	RW	
0x317F	0x00	[7:0]	Reserved	RW	
0x3180	0x67	[7:0]	Reserved	RW	
0x3181	0x9A	[7:0]	Reserved	RW	
0x3182	0x02	[7:0]	Reserved	RW	
0x3183	0x7C	[7:0]	Reserved	RW	
0x3184	0x01	[7:0]	Reserved	RW	
0x3185	0xAA	[7:0]	Reserved	RW	
0x3186	0x00	[7:0]	Reserved	RW	
0x3187	0x00	[7:0]	Reserved	RW	
0x3188	0x00	[7:0]	Reserved	RW	
0x3189	0x00	[7:0]	Reserved	RW	
0x318A	0x00	[7:0]	Reserved	RW	
0x318B	0x00	[7:0]	Reserved	RW	
0x318C	0x00	[7:0]	Reserved	RW	
0x318D	0x00	[7:0]	Reserved	RW	
0x318E	0x00	[7:0]	Reserved	RW	
0x318F	0x00	[7:0]	Reserved	RW	
0x3200	0x21	[7:0]	Reserved	RW	
0x3201	0x67	[7:0]	Reserved	RW	
0x3202	0x9A	[7:0]	Reserved	RW	
0x3203	0x02	[7:0]	Reserved	RW	
0x3204	0x7C	[7:0]	Reserved	RW	
0x3205	0x01	[7:0]	Reserved	RW	
0x3206	0xAA	[7:0]	Reserved	RW	
0x3207	0x00	[7:0]	Reserved	RW	
0x3208	0x00	[7:0]	Reserved	RW	
0x3209	0x00	[7:0]	Reserved	RW	
0x320A	0x00	[7:0]	Reserved	RW	
0x320B	0x00	[7:0]	Reserved	RW	
0x320C	0x00	[7:0]	Reserved	RW	
0x320D	0x00	[7:0]	Reserved	RW	
0x320E	0x00	[7:0]	Reserved	RW	
0x320F	0x01	[7:0]	Reserved	RW	
0x3210	0x00	[7:0]	Reserved	RW	
0x3211	0x00	[7:0]	Reserved	RW	
0x3212	0x00	[7:0]	Reserved	RW	
0x3213	0x00	[7:0]	Reserved	RW	
0x3214	0x00	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x3215	0x00	[7:0]	Reserved	RW	
0x3216	0x00	[7:0]	Reserved	RW	
0x3217	0x00	[7:0]	Reserved	RW	
0x3218	0x33	[7:0]	Reserved	RW	
0x3219	0x33	[7:0]	Reserved	RW	
0x321A	0x33	[7:0]	Reserved	RW	
0x321B	0x33	[7:0]	Reserved	RW	
0x321C	0x33	[7:0]	Reserved	RW	
0x321D	0x33	[7:0]	Reserved	RW	
0x321E	0x33	[7:0]	Reserved	RW	
0x321F	0x33	[7:0]	Reserved	RW	
0x3220	0x26	[7:0]	Reserved	RW	
0x3221	0x66	[7:0]	Reserved	RW	
0x3222	0x26	[7:0]	Reserved	RW	
0x3223	0x66	[7:0]	Reserved	RW	
0x3224	0x26	[7:0]	Reserved	RW	
0x3225	0x66	[7:0]	Reserved	RW	
0x3226	0x26	[7:0]	Reserved	RW	
0x3227	0x66	[7:0]	Reserved	RW	
0x3228	0x19	[7:0]	Reserved	RW	
0x3229	0x9A	[7:0]	Reserved	RW	
0x322A	0x19	[7:0]	Reserved	RW	
0x322B	0x9A	[7:0]	Reserved	RW	
0x322C	0x19	[7:0]	Reserved	RW	
0x322D	0x9A	[7:0]	Reserved	RW	
0x322E	0x19	[7:0]	Reserved	RW	
0x322F	0x9A	[7:0]	Reserved	RW	
0x3230	0x0C	[7:0]	Reserved	RW	
0x3231	0xCD	[7:0]	Reserved	RW	
0x3232	0x0C	[7:0]	Reserved	RW	
0x3233	0xCD	[7:0]	Reserved	RW	
0x3234	0x0C	[7:0]	Reserved	RW	
0x3235	0xCD	[7:0]	Reserved	RW	
0x3236	0x0C	[7:0]	Reserved	RW	
0x3237	0xCD	[7:0]	Reserved	RW	
0x3238	0x00	[7:0]	Reserved	RW	
0x3239	0x00	[7:0]	Reserved	RW	
0x323A	0x00	[7:0]	Reserved	RW	
0x323B	0x00	[7:0]	Reserved	RW	
0x323C	0x00	[7:0]	Reserved	RW	
0x323D	0x00	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x323E	0x00	[7:0]	Reserved	RW	
0x323F	0x00	[7:0]	Reserved	RW	
0x3240	0x00	[7:0]	Reserved	RW	
0x3241	0x00	[7:0]	Reserved	RW	
0x3242	0x00	[7:0]	Reserved	RW	
0x3243	0x00	[7:0]	Reserved	RW	
0x3244	0x00	[7:0]	Reserved	RW	
0x3245	0x00	[7:0]	Reserved	RW	
0x3246	0x00	[7:0]	Reserved	RW	
0x3247	0x00	[7:0]	Reserved	RW	
0x3248	0x00	[7:0]	Reserved	RW	
0x3249	0x00	[7:0]	Reserved	RW	
0x324A	0x00	[7:0]	Reserved	RW	
0x324B	0x00	[7:0]	Reserved	RW	
0x324C	0x00	[7:0]	Reserved	RW	
0x324D	0x00	[7:0]	Reserved	RW	
0x324E	0x00	[7:0]	Reserved	RW	
0x324F	0x00	[7:0]	Reserved	RW	
0x3250	0x00	[7:0]	Reserved	RW	
0x3251	0x00	[7:0]	Reserved	RW	
0x3252	0x00	[7:0]	Reserved	RW	
0x3253	0x00	[7:0]	Reserved	RW	
0x3254	0x00	[7:0]	Reserved	RW	
0x3255	0x00	[7:0]	Reserved	RW	
0x3256	0x00	[7:0]	Reserved	RW	
0x3257	0x00	[7:0]	Reserved	RW	
0x3258	0x00	[7:0]	Reserved	RW	
0x3259	0x00	[7:0]	Reserved	RW	
0x325A	0x00	[7:0]	Reserved	RW	
0x325B	0x00	[7:0]	Reserved	RW	
0x325C	0x00	[7:0]	Reserved	RW	
0x325D	0x00	[7:0]	Reserved	RW	
0x325E	0x00	[7:0]	Reserved	RW	
0x325F	0x00	[7:0]	Reserved	RW	
0x3260	0x00	[7:0]	Reserved	RW	
0x3261	0x00	[7:0]	Reserved	RW	
0x3262	0x00	[7:0]	Reserved	RW	
0x3263	0x00	[7:0]	Reserved	RW	
0x3264	0x00	[7:0]	Reserved	RW	
0x3265	0x00	[7:0]	Reserved	RW	
0x3266	0x00	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x3267	0x00	[7:0]	Reserved	RW	
0x3268	0x00	[7:0]	Reserved	RW	
0x3269	0x00	[7:0]	Reserved	RW	
0x326A	0x00	[7:0]	Reserved	RW	
0x326B	0x00	[7:0]	Reserved	RW	
0x326C	0x00	[7:0]	Reserved	RW	
0x326D	0x00	[7:0]	Reserved	RW	
0x326E	0x00	[7:0]	Reserved	RW	
0x326F	0x00	[7:0]	Reserved	RW	
0x3270	0x00	[7:0]	Reserved	RW	
0x3271	0x00	[7:0]	Reserved	RW	
0x3272	0x00	[7:0]	Reserved	RW	
0x3273	0x00	[7:0]	Reserved	RW	
0x3274	0x00	[7:0]	Reserved	RW	
0x3275	0x00	[7:0]	Reserved	RW	
0x3276	0x00	[7:0]	Reserved	RW	
0x3277	0x00	[7:0]	Reserved	RW	
0x3278	0x00	[7:0]	Reserved	RW	
0x3279	0x00	[7:0]	Reserved	RW	
0x320A	0x00	[7:0]	Reserved	RW	
0x327B	0x00	[7:0]	Reserved	RW	
0x327C	0x00	[7:0]	Reserved	RW	
0x327D	0x00	[7:0]	Reserved	RW	
0x327E	0x00	[7:0]	Reserved	RW	
0x327F	0x00	[7:0]	Reserved	RW	
0x3280	0x00	[7:0]	Reserved	RW	
0x3281	0x00	[7:0]	Reserved	RW	
0x3282	0x00	[7:0]	Reserved	RW	
0x3283	0x00	[7:0]	Reserved	RW	
0x3284	0x00	[7:0]	Reserved	RW	
0x3285	0x00	[7:0]	Reserved	RW	
0x3286	0x00	[7:0]	Reserved	RW	
0x3287	0x00	[7:0]	Reserved	RW	
0x3288	0x00	[7:0]	Reserved	RW	
0x3289	0x00	[7:0]	Reserved	RW	
0x328A	0x00	[7:0]	Reserved	RW	
0x328B	0x00	[7:0]	Reserved	RW	
0x328C	0x00	[7:0]	Reserved	RW	
0x328D	0x00	[7:0]	Reserved	RW	
0x328E	0x00	[7:0]	Reserved	RW	
0x328F	0x00	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x3290	0x00	[7:0]	Reserved	RW	
0x3291	0x00	[7:0]	Reserved	RW	
0x3292	0x00	[7:0]	Reserved	RW	
0x3293	0x00	[7:0]	Reserved	RW	
0x3294	0x00	[7:0]	Reserved	RW	
0x3295	0x00	[7:0]	Reserved	RW	
0x3296	0x00	[7:0]	Reserved	RW	
0x3297	0x00	[7:0]	Reserved	RW	
0x3298	0x00	[7:0]	Reserved	RW	
0x3299	0x00	[7:0]	Reserved	RW	
0x329A	0x00	[7:0]	Reserved	RW	
0x329B	0x00	[7:0]	Reserved	RW	
0x329C	0x00	[7:0]	Reserved	RW	
0x329D	0x00	[7:0]	Reserved	RW	
0x329E	0x00	[7:0]	Reserved	RW	
0x329F	0x00	[7:0]	Reserved	RW	
0x32A0	0x00	[7:0]	Reserved	RW	
0x32A1	0x00	[7:0]	Reserved	RW	
0x32A2	0x00	[7:0]	Reserved	RW	
0x32A3	0x00	[7:0]	Reserved	RW	
0x32A4	0x00	[7:0]	Reserved	RW	
0x32A5	0x00	[7:0]	Reserved	RW	
0x32A6	0x00	[7:0]	Reserved	RW	
0x32A7	0x00	[7:0]	Reserved	RW	
0x32A8	0x00	[7:0]	Reserved	RW	
0x32A9	0x00	[7:0]	Reserved	RW	
0x32AA	0x00	[7:0]	Reserved	RW	
0x32AB	0x00	[7:0]	Reserved	RW	
0x32AC	0x00	[7:0]	Reserved	RW	
0x32AD	0x00	[7:0]	Reserved	RW	
0x32AE	0x00	[7:0]	Reserved	RW	
0x32AF	0x00	[7:0]	Reserved	RW	
0x32B0	0x00	[7:0]	Reserved	RW	
0x32B1	0x00	[7:0]	Reserved	RW	
0x32B2	0x00	[7:0]	Reserved	RW	
0x32B3	0x00	[7:0]	Reserved	RW	
0x32B4	0x00	[7:0]	Reserved	RW	
0x32B5	0x00	[7:0]	Reserved	RW	
0x32B6	0x00	[7:0]	Reserved	RW	
0x32B7	0x00	[7:0]	Reserved	RW	
0x32B8	0x00	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x32B9	0x00	[7:0]	Reserved	RW	
0x32BA	0x00	[7:0]	Reserved	RW	
0x32BB	0x00	[7:0]	Reserved	RW	
0x32BC	0x00	[7:0]	Reserved	RW	
0x32BD	0x00	[7:0]	Reserved	RW	
0x32BE	0x00	[7:0]	Reserved	RW	
0x32BF	0x00	[7:0]	Reserved	RW	
0x32C0	0x00	[7:0]	Reserved	RW	
0x32C1	0x00	[7:0]	Reserved	RW	
0x32C2	0x00	[7:0]	Reserved	RW	
0x32C3	0x00	[7:0]	Reserved	RW	
0x32C4	0x00	[7:0]	Reserved	RW	
0x32C5	0x00	[7:0]	Reserved	RW	
0x32C6	0x00	[7:0]	Reserved	RW	
0x32C7	0x00	[7:0]	Reserved	RW	
0x32C8	0x00	[7:0]	Reserved	RW	
0x32C9	0x00	[7:0]	Reserved	RW	
0x32CA	0x00	[7:0]	Reserved	RW	
0x32CB	0x00	[7:0]	Reserved	RW	
0x32CC	0x00	[7:0]	Reserved	RW	
0x32CD	0x00	[7:0]	Reserved	RW	
0x32CE	0x00	[7:0]	Reserved	RW	
0x32CF	0x00	[7:0]	Reserved	RW	
0x32D0	0x00	[7:0]	Reserved	RW	
0x32D1	0x00	[7:0]	Reserved	RW	
0x32D2	0x00	[7:0]	Reserved	RW	
0x32D3	0x00	[7:0]	Reserved	RW	
0x32D4	0x00	[7:0]	Reserved	RW	
0x32D5	0x00	[7:0]	Reserved	RW	
0x32D6	0x00	[7:0]	Reserved	RW	
0x32D7	0x00	[7:0]	Reserved	RW	
0x32D8	0x00	[7:0]	Reserved	RW	
0x32D9	0x00	[7:0]	Reserved	RW	
0x32DA	0x00	[7:0]	Reserved	RW	
0x32DB	0x00	[7:0]	Reserved	RW	
0x32DC	0x00	[7:0]	Reserved	RW	
0x32DD	0x00	[7:0]	Reserved	RW	
0x32DE	0x00	[7:0]	Reserved	RW	
0x32DF	0x00	[7:0]	Reserved	RW	
0x32E0	0x00	[7:0]	Reserved	RW	
0x32E1	0x00	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x32E2	0x00	[7:0]	Reserved	RW	
0x32E3	0x00	[7:0]	Reserved	RW	
0x32E4	0x00	[7:0]	Reserved	RW	
0x32E5	0x00	[7:0]	Reserved	RW	
0x32E6	0x00	[7:0]	Reserved	RW	
0x32E7	0x00	[7:0]	Reserved	RW	
0x32E8	0x00	[7:0]	Reserved	RW	
0x32E9	0x00	[7:0]	Reserved	RW	
0x32EA	0x00	[7:0]	Reserved	RW	
0x32EB	0x00	[7:0]	Reserved	RW	
0x32EC	0x00	[7:0]	Reserved	RW	
0x32ED	0x00	[7:0]	Reserved	RW	
0x32EE	0x00	[7:0]	Reserved	RW	
0x32EF	0x00	[7:0]	Reserved	RW	
0x32F0	0x00	[7:0]	Reserved	RW	
0x32F1	0x00	[7:0]	Reserved	RW	
0x32F2	0x00	[7:0]	Reserved	RW	
0x32F3	0x00	[7:0]	Reserved	RW	
0x32F4	0x00	[7:0]	Reserved	RW	
0x32F5	0x00	[7:0]	Reserved	RW	
0x32F6	0x00	[7:0]	Reserved	RW	
0x32F7	0x00	[7:0]	Reserved	RW	
0x32F8	0x00	[7:0]	Reserved	RW	
0x32F9	0x00	[7:0]	Reserved	RW	
0x32FA	0x00	[7:0]	Reserved	RW	
0x32FB	0x00	[7:0]	Reserved	RW	
0x32FC	0x00	[7:0]	Reserved	RW	
0x32FD	0x00	[7:0]	Reserved	RW	
0x32FE	0x00	[7:0]	Reserved	RW	
0x32FF	0x00	[7:0]	Reserved	RW	
0x3300	0x00	[7:0]	Reserved	RW	
0x3301	0x00	[7:0]	Reserved	RW	
0x3302	0x00	[7:0]	Reserved	RW	
0x3303	0x00	[7:0]	Reserved	RW	
0x3304	0x00	[7:0]	Reserved	RW	
0x3305	0x00	[7:0]	Reserved	RW	
0x3306	0x00	[7:0]	Reserved	RW	
0x3307	0x00	[7:0]	Reserved	RW	
0x3308	0x00	[7:0]	Reserved	RW	
0x3309	0x00	[7:0]	Reserved	RW	
0x330A	0x00	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x330B	0x00	[7:0]	Reserved	RW	
0x330C	0x00	[7:0]	Reserved	RW	
0x330D	0x00	[7:0]	Reserved	RW	
0x330E	0x00	[7:0]	Reserved	RW	
0x330F	0x00	[7:0]	Reserved	RW	
0x3310	0x00	[7:0]	Reserved	RW	
0x3311	0x00	[7:0]	Reserved	RW	
0x3312	0x00	[7:0]	Reserved	RW	
0x3313	0x00	[7:0]	Reserved	RW	
0x3314	0x00	[7:0]	Reserved	RW	
0x3315	0x00	[7:0]	Reserved	RW	
0x3316	0x00	[7:0]	Reserved	RW	
0x3317	0x00	[7:0]	Reserved	RW	
0x3318	0x00	[7:0]	Reserved	RW	
0x3319	0x00	[7:0]	Reserved	RW	
0x331A	0x00	[7:0]	Reserved	RW	
0x331B	0x00	[7:0]	Reserved	RW	
0x331C	0x00	[7:0]	Reserved	RW	
0x331D	0x00	[7:0]	Reserved	RW	
0x331E	0x00	[7:0]	Reserved	RW	
0x331F	0x00	[7:0]	Reserved	RW	
0x3320	0x00	[7:0]	Reserved	RW	
0x3321	0x00	[7:0]	Reserved	RW	
0x3322	0x00	[7:0]	Reserved	RW	
0x3323	0x00	[7:0]	Reserved	RW	
0x3324	0x00	[7:0]	Reserved	RW	
0x3325	0x00	[7:0]	Reserved	RW	
0x3326	0x00	[7:0]	Reserved	RW	
0x3327	0x00	[7:0]	Reserved	RW	
0x3328	0x00	[7:0]	Reserved	RW	
0x3329	0x00	[7:0]	Reserved	RW	
0x332A	0x00	[7:0]	Reserved	RW	
0x332B	0x00	[7:0]	Reserved	RW	
0x332C	0x00	[7:0]	Reserved	RW	
0x332D	0x00	[7:0]	Reserved	RW	
0x332E	0x00	[7:0]	Reserved	RW	
0x332F	0x00	[7:0]	Reserved	RW	
0x3330	0x00	[7:0]	Reserved	RW	
0x3331	0x00	[7:0]	Reserved	RW	
0x3332	0x00	[7:0]	Reserved	RW	
0x3333	0x00	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x3334	0x00	[7:0]	Reserved	RW	
0x3335	0x00	[7:0]	Reserved	RW	
0x3336	0x00	[7:0]	Reserved	RW	
0x3337	0x00	[7:0]	Reserved	RW	
0x3338	0x00	[7:0]	Reserved	RW	
0x3339	0x00	[7:0]	Reserved	RW	
0x333A	0x00	[7:0]	Reserved	RW	
0x333B	0x00	[7:0]	Reserved	RW	
0x333C	0x00	[7:0]	Reserved	RW	
0x333D	0x00	[7:0]	Reserved	RW	
0x333E	0x00	[7:0]	Reserved	RW	
0x333F	0x00	[7:0]	Reserved	RW	
0x3340	0x00	[7:0]	Reserved	RW	
0x3341	0x00	[7:0]	Reserved	RW	
0x3342	0x00	[7:0]	Reserved	RW	
0x3343	0x00	[7:0]	Reserved	RW	
0x3344	0x00	[7:0]	Reserved	RW	
0x3345	0x00	[7:0]	Reserved	RW	
0x3346	0x00	[7:0]	Reserved	RW	
0x3347	0x00	[7:0]	Reserved	RW	
0x3348	0x00	[7:0]	Reserved	RW	
0x3349	0x00	[7:0]	Reserved	RW	
0x334A	0x00	[7:0]	Reserved	RW	
0x334B	0x00	[7:0]	Reserved	RW	
0x334C	0x00	[7:0]	Reserved	RW	
0x334D	0x00	[7:0]	Reserved	RW	
0x334E	0x00	[7:0]	Reserved	RW	
0x334F	0x00	[7:0]	Reserved	RW	
0x3350	0x00	[7:0]	Reserved	RW	
0x3351	0x00	[7:0]	Reserved	RW	
0x3352	0x00	[7:0]	Reserved	RW	
0x3353	0x00	[7:0]	Reserved	RW	
0x3354	0x00	[7:0]	Reserved	RW	
0x3355	0x00	[7:0]	Reserved	RW	
0x3356	0x00	[7:0]	Reserved	RW	
0x3357	0x00	[7:0]	Reserved	RW	
0x3358	0x00	[7:0]	Reserved	RW	
0x3359	0x00	[7:0]	Reserved	RW	
0x335A	0x00	[7:0]	Reserved	RW	
0x335B	0x00	[7:0]	Reserved	RW	
0x335C	0x00	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x335D	0x00	[7:0]	Reserved	RW	
0x335E	0x00	[7:0]	Reserved	RW	
0x335F	0x00	[7:0]	Reserved	RW	
0x3360	0x00	[7:0]	Reserved	RW	
0x3361	0x00	[7:0]	Reserved	RW	
0x3362	0x00	[7:0]	Reserved	RW	
0x3363	0x00	[7:0]	Reserved	RW	
0x3364	0x00	[7:0]	Reserved	RW	
0x3365	0x00	[7:0]	Reserved	RW	
0x3366	0x00	[7:0]	Reserved	RW	
0x3367	0x00	[7:0]	Reserved	RW	
0x3368	0x00	[7:0]	Reserved	RW	
0x3369	0x00	[7:0]	Reserved	RW	
0x336A	0x00	[7:0]	Reserved	RW	
0x336B	0x00	[7:0]	Reserved	RW	
0x336C	0x00	[7:0]	Reserved	RW	
0x336D	0x00	[7:0]	Reserved	RW	
0x336E	0x00	[7:0]	Reserved	RW	
0x336F	0x00	[7:0]	Reserved	RW	
0x3370	0x00	[7:0]	Reserved	RW	
0x3371	0x00	[7:0]	Reserved	RW	
0x3372	0x00	[7:0]	Reserved	RW	
0x3373	0x00	[7:0]	Reserved	RW	
0x3374	0x00	[7:0]	Reserved	RW	
0x3375	0x00	[7:0]	Reserved	RW	
0x3376	0x00	[7:0]	Reserved	RW	
0x3377	0x00	[7:0]	Reserved	RW	
0x3378	0x00	[7:0]	Reserved	RW	
0x3379	0x00	[7:0]	Reserved	RW	
0x337A	0x00	[7:0]	Reserved	RW	
0x337B	0x00	[7:0]	Reserved	RW	
0x337C	0x00	[7:0]	Reserved	RW	
0x337D	0x00	[7:0]	Reserved	RW	
0x337E	0x00	[7:0]	Reserved	RW	
0x337F	0x00	[7:0]	Reserved	RW	
0x3380	0x00	[7:0]	Reserved	RW	
0x3381	0x00	[7:0]	Reserved	RW	
0x3382	0x00	[7:0]	Reserved	RW	
0x3383	0x00	[7:0]	Reserved	RW	
0x3384	0x00	[7:0]	Reserved	RW	
0x3385	0x00	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x3386	0x00	[7:0]	Reserved	RW	
0x3387	0x00	[7:0]	Reserved	RW	
0x3388	0x00	[7:0]	Reserved	RW	
0x3389	0x00	[7:0]	Reserved	RW	
0x338A	0x00	[7:0]	Reserved	RW	
0x338B	0x00	[7:0]	Reserved	RW	
0x338C	0x00	[7:0]	Reserved	RW	
0x338D	0x00	[7:0]	Reserved	RW	
0x338E	0x00	[7:0]	Reserved	RW	
0x338F	0x00	[7:0]	Reserved	RW	
0x3390	0x00	[7:0]	Reserved	RW	
0x3391	0x00	[7:0]	Reserved	RW	
0x3392	0x00	[7:0]	Reserved	RW	
0x3393	0x00	[7:0]	Reserved	RW	
0x3394	0x00	[7:0]	Reserved	RW	
0x3395	0x00	[7:0]	Reserved	RW	
0x3396	0x00	[7:0]	Reserved	RW	
0x3397	0x00	[7:0]	Reserved	RW	
0x3398	0x00	[7:0]	Reserved	RW	
0x3399	0x00	[7:0]	Reserved	RW	
0x339A	0x00	[7:0]	Reserved	RW	
0x339B	0x00	[7:0]	Reserved	RW	
0x339C	0x00	[7:0]	Reserved	RW	
0x339D	0x00	[7:0]	Reserved	RW	
0x339E	0x00	[7:0]	Reserved	RW	
0x339F	0x00	[7:0]	Reserved	RW	
0x33A0	0x00	[7:0]	Reserved	RW	
0x33A1	0x00	[7:0]	Reserved	RW	
0x33A2	0x00	[7:0]	Reserved	RW	
0x33A3	0x00	[7:0]	Reserved	RW	
0x33A4	0x00	[7:0]	Reserved	RW	
0x33A5	0x00	[7:0]	Reserved	RW	
0x33A6	0x00	[7:0]	Reserved	RW	
0x33A7	0x00	[7:0]	Reserved	RW	
0x33A8	0x00	[7:0]	Reserved	RW	
0x33A9	0x00	[7:0]	Reserved	RW	
0x33AA	0x00	[7:0]	Reserved	RW	
0x33AB	0x00	[7:0]	Reserved	RW	
0x33AC	0x00	[7:0]	Reserved	RW	
0x33AD	0x00	[7:0]	Reserved	RW	
0x33AE	0x00	[7:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x33AF	0x00	[7:0]	Reserved	RW	
0x3D00	0x01	[7:0]	Reserved	RW	
0x3D01	0x44	[7:0]	Reserved	RW	
0x3D02	0xFF	[7:0]	Reserved	RW	
0x3D03	0xA5	[7:0]	Reserved	RW	
0x3D04	0x00	[7:0]	Reserved	RW	
0x3D05	0x17	[7:0]	Reserved	RW	
0x3D06	0xFF	[7:0]	Reserved	RW	
0x3D07	0x81	[7:0]	Reserved	RW	
0x3D08	0x02	[7:0]	Reserved	RW	
0x3D09	0x2E	[7:0]	Reserved	RW	
0x3D0A	0xFF	[7:0]	Reserved	RW	
0x3D0B	0x51	[7:0]	Reserved	RW	
0x3D0C	0x00	[7:0]	Reserved	RW	
0x3D0D	0x02	[7:0]	Reserved	RW	
0x3D0E	0xFF	[7:0]	Reserved	RW	
0x3D0F	0xB2	[7:0]	Reserved	RW	
0x3D10	0x01	[7:0]	Reserved	RW	
0x3D11	0x4C	[7:0]	Reserved	RW	



