

S5K6AAFX13

1/6" 1.3Mp CMOS Image Sensor SoC with an Embedded
Image Processor

Technical Data Sheet
(EVT3.2 - R03)

SAMSUNG ELECTRONICS PROPRIETARY
Copyright © 2006-2009 Samsung Electronics, Inc. All Rights Reserved

REVISION HISTORY

Revision	Date	Author	Amendment
R03	19-Feb-09	Yoel Yaffe	- Product code updated S5K6AAFX13 for mobile applications. - Datasheet updated with latest EVT updates.
R02	23-Aug-08	Mickey Bahar	RGB565 format change.
R01	7-Jul-08	Liza Farachdel	Tech writer proofreading
R01	7-Jul-08	Yoel Yaffe	- Update 720p support. Comment on 2.8V regulator support. Update feature list.
R00	27-Feb-08	Ayal Keisar	Initial draft copied from EVT0-R07 - SW registers updated - Remove configuration bit I2C_8bit_add_det_mode (From i2c_mode). - Update description for HW registers: sw_reset, sw_load_complete, I2C indirect access pointers (Mem_Rd/Wr_addH/L, Command_Rd/Wr_addH/L). - Update table of SW registers (new table)

Table of Contents

1	FEATURES	1-5
1.1	IMAGE SENSOR	1-5
1.2	IMAGE PROCESSOR	1-6
1.3	DEVICE	1-6
2	GENERAL DESCRIPTION	2-7
3	LOGICAL SYMBOL DIAGRAM.....	3-8
4	PAD CONFIGURATION.....	4-9
5	PAD DESCRIPTION.....	5-10
6	PIXEL ARRAY INFORMATION	6-13
7	VIDEO OUTPUT INTERFACE DESCRIPTION.....	7-14
8	CONTROL INTERFACE DESCRIPTION	8-23
9	FUNCTIONAL DESCRIPTION	9-30
9.1	ANALOG TO DIGITAL CONVERTER (ADC)	9-30
9.1.1	<i>Correlated Double Sampling (CDS)</i>	9-30
9.1.2	<i>Programmable Gain</i>	9-31
9.1.3	<i>Programmable Offset</i>	9-31
9.2	TIMING GENERATOR FUNCTIONS	9-31
9.2.1	<i>CIS Raw Data Output</i>	9-31
9.3	PIXEL ARRAY ADDRESSES	9-31
9.4	MIRROR/FLIP.....	9-32
9.5	STANDARD READOUT.....	9-32
9.6	HORIZONTALLY MIRRORED AND VERTICALLY FLIPPED READOUT	9-33
9.7	SUB-SAMPLED READOUT	9-34
9.8	FRAME RATE CONTROL (VIRTUAL FRAME)	9-34
9.9	INTEGRATION TIME CONTROL (ELECTRONIC SHUTTER CONTROL)	9-35
9.9.1	<i>LED and Xenon Flash Control</i>	9-35
9.9.2	<i>Register-Based Host Interface</i>	9-35
9.10	IMAGE SIGNAL PROCESSOR	9-39
9.10.1	<i>Auto Exposure</i>	9-39
9.10.2	<i>Auto White Balance</i>	9-39
9.10.3	<i>Auto Flicker Correction</i>	9-39



9.10.4	<i>Lens Shading Correction</i>	9-39
9.10.5	<i>Color Demosaicking</i>	9-39
9.10.6	<i>Color Correction</i>	9-39
9.10.7	<i>Despeckle</i>	9-39
9.10.8	<i>Denoising</i>	9-39
9.10.9	<i>Gamma Correction</i>	9-40
9.10.10	<i>Image Downscaling</i>	9-40
9.10.11	<i>Special Effects</i>	9-40
9.10.12	<i>Output Formatting</i>	9-40
9.10.13	<i>Image Properties Controls</i>	9-40
10	SYSTEM STATE DIAGRAM	10-41
11	POWER-UP/DOWN SEQUENCE	11-42
12	STANDBY SEQUENCE	12-43
13	ELECTRICAL CHARACTERISTICS	13-44
14	IMAGING CHARACTERISTICS	14-46
15	REGISTER DESCRIPTION	15-47
15.1	REGISTER ADDRESS MAPPING	15-47
16	H/W REGISTER INTERFACE – GENERAL REGISTERS (0XD0000000 – 0XD0000FFF)	16-48
17	HOST SW REGISTER INTERFACE (0X7000000 – 0X70002000)	17-52

1 Features

1.1 Image Sensor

- Optical format : 1/6 inch
- Unit pixel size : 1.75um
- Effective resolution : 1280 (H) x 1024 (V)
- Active resolution : 1284 (H) x 1028 (V)
- Color filter : RGB Bayer pattern
- Shutter type : Electronic rolling shutter
- Max. capture frame rate : 15fps @full resolution, 24fps@720p
- Max. video frame rate : 30fps @VGA, 24fps@720p
- Max. pixel clock Frequency : 56MHz
- Min. pixel clock Frequency: 48Mhz (full resolution@15fps)
- Max. pixel rate : 28Mp/s
- ADC accuracy : 10-bit
- Progressive scan readout
- Window panning and cropping
- Vertical flip and horizontal mirror mode
- Continuous and single frame capture mode
- Frame rate control
- LED and flash strobe mode
- Parallel output format: ITU-R. 656/601 YUV422, ITU-R 601 RGB565, RGB888 (Up to VGA), RAW10
- Serial output format: MIPI CSI2 (single lane) YUV422, RGB565, RGB888 (Up to VGA), RAW10

1.2 Image Processor

- Color recovery and correction
- False color suppression
- Lens shading correction
- Noise removal
- Edge enhancement
- 720p, SVGA or any size smaller than SVGA down scaling
- Programmable gamma correction
- Auto defect correction
- Auto dark level compensation
- Auto flicker correction (50/60Hz)
- Auto exposure (AE)
- Auto white balance (AWB)
- Built-in test image generation

1.3 Device

- Host control interface: I²C bus
- Internal PLL (6MHz to 27MHz input frequency)
- Stand-by mode for power saving
- Operating temperature: -20°C to +60°C
- Supply voltage: 2.8V for analog, 1.5V for digital core (with internal regulator off), 1.8V - 2.8V for I/O
- 1.8V (or 2.8V) to 1.5V internal regulator

2 General Description

The S5K6AAF13 is a highly integrated 1.3Mp camera chip that includes a CMOS image sensor, an image processor and both 8-bit ITU-R 656/601 parallel interface and MIPI CSI2 compliant serial interface. It is fabricated by the SAMSUNG 0.13 μ m CMOS image sensor process developed for imaging applications to realize high-efficiency and low-power photo sensor.

The CMOS image sensor consists of the 1284x1028 Active Pixel Sensor (APS) array, which has a 1/6-inch optical format, on-chip 10-bit ADC array to digitize the analog pixel output, and on-chip Correlated Double Sampling (CDS) to reduce Fixed Pattern Noise (FPN) drastically.

The image processor performs sophisticated image processing functions, including color recovery and correction, false color suppression, lens shading correction, noise removal, edge enhancement, programmable gamma correction, image down scaling, auto defect correction, auto dark level compensation, auto flicker correction (50/60Hz), auto exposure (AE), auto white balance (AWB). The auto functions are performed by F/W on an embedded RISC processor. The host controller is able to access and control this device via general IIC bus.

3 Logical Symbol Diagram

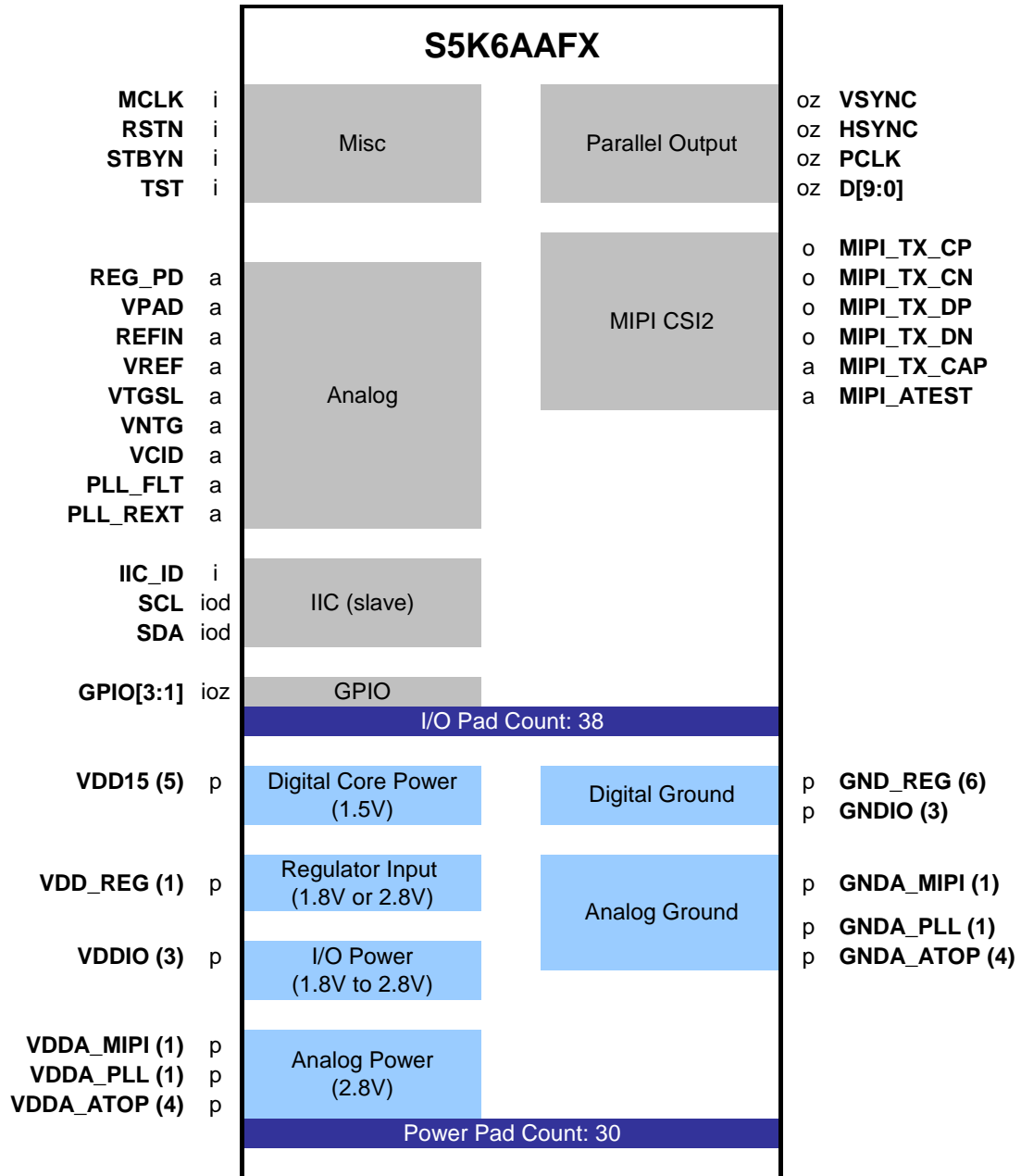


Figure 1: Logical Symbol Diagram

5 Pad Description

Table 1: Pad Description

Pad No	Pad Name	I/O	Description
62	MCLK	Input	Master clock. 6M to 27MHz. 27MHz is default. If lower frequencies are used, the PLL register settings must be changed.
66	RSTN	Input	Master reset (Active low)
63	STBYN	Input	Hardware standby mode (Active low). Set to '1' if not used. All parallel outputs go to Hi-Z state when STBYN is asserted.
1	TST	Input	Test mode. Set to '0' in normal mode.
43	REG_PD	Analog	Internal regulator power-down: 0:operation, 1:power-down
42	VPAD	Analog	Analog test. Open in normal mode.
41	REFIN	Analog	Analog test. Open in normal mode.
40	VREF	Analog	Analog pad. 0.1uF external capacitor between pin and ground.
39	VTGSL	Analog	Analog pad. 0.1uF external capacitor between pin and ground.
38	VNTG	Analog	Analog pad. 0.1uF external capacitor between pin and ground.
27	VCID	Analog	Analog test. Connect to 2.8V.
56	PLL_FLT	Analog	PLL test. Open in normal.
59	PLL_REXT	Analog	PLL reference resistor: PLL_REG[13]='0' : external R (12Kohm) PLL_REG[13]='1' : internal R (open, default)
2	IIC_ID	Input	IIC slave address selection: IIC_ID= 0: 0111_100b, 1: 0101_101b
64	SCL	In/Out	IIC slave clock for host control. Open drain.
65	SDA	In/Out	IIC slave data for host control. Open drain.
24	GPIO_1	In/Out	General purpose I/Os: [NOTE]
25	GPIO_2	In/Out	

Pad No	Pad Name	I/O	Description
26	GPIO_3	In/Out	GPIO_1: flash strobe output GPIO_2: flash strobe input Hi-z.
21	VSYNC	Output	Vertical sync output for parallel interface. Hi-z.
20	HSYNC	Output	Horizontal sync output for parallel interface. Hi-z.
19	PCLK	Output	Pixel clock output for parallel interface. Hi-z.
3	D0	Output	Pixel data output for parallel interface. D9: MSB, D0: LSB D[9:0] for 10-bit data D[9:2] for 8-bit data Hi-z.
4	D1	Output	
7	D2	Output	
8	D3	Output	
9	D4	Output	
12	D5	Output	
13	D6	Output	
16	D7	Output	
17	D8	Output	
18	D9	Output	
50	MIPI_TX_CP	Output	CSI-2 Tx clock positive. Open if not used.
51	MIPI_TX_CN	Output	CSI-2 Tx clock negative. Open if not used.
52	MIPI_TX_DP	Output	CSI-2 Tx data positive. Open if not used.
53	MIPI_TX_DN	Output	CSI-2 Tx data negative. Open if not used.
54	MIPI_TX_ATEST	Analog	Analog test. Open in normal mode or if not used.
55	MIPI_TX_CAP	Analog	CSI-2 Tx capacitor. 0.1uF external capacitor between pin and ground. Open if not used.
5 15 33 46 61	VDD15_1 VDD15_6 VDD15_14 VDD15_21 VDD15_28	Power	Digital Core Power 1.5V (1.4V to 1.6V) [NOTE] a) Regulator on (REG_PD=0): 0.47uF capacitor between VDD15 and ground. b) Regulator off (REG_PD=1): 1.5V with 0.47uF power capacitor.

Pad No	Pad Name	I/O	Description
44	VDD_REG_19	Power	Regulator input power 1.8V (1.7V to 1.9V) or 2.8V (2.6V to 3.0) [NOTE] a) Regulator on (REG_PD=0): 1.8V or 2.8V b) Regulator off (REG_PD=1): 1.5V c) Using 2.8V is not recommended due to increased system power.
11 23 67	VDDIO_4 VDDIO_8 VDDIO_29	Power	I/O power 1.8V (1.65V to 1.95V) or 2.8V (2.5V to 3.1V) with 0.1uF power capacitor
6 14 32 45 49 60	GND_REG_2 GND_REG_5 GND_REG_13 GND_REG_20 GND_REG_24 GND_REG_27	Power	Digital ground
10 22 68	GNDIO_3 GNDIO_7 GNDIO_30		
48 58 28 29 36 37	VDDA_MIPI_23 VDDA_PLL_26 VDDA_ATOP_9 VDDA_ATOP_10 VDDA_ATOP_17 VDDA_ATOP_18	Power	Analog power 2.8V (2.6V to 3.0V) with 0.1uF power capacitor
47 57 30 31 34 35	GND_A_MIPI_22 GND_A_PLL_25 GND_A_ATOP_11 GND_A_ATOP_12 GND_A_ATOP_15 GND_A_ATOP_16	Power	Analog ground

6 Pixel Array Information

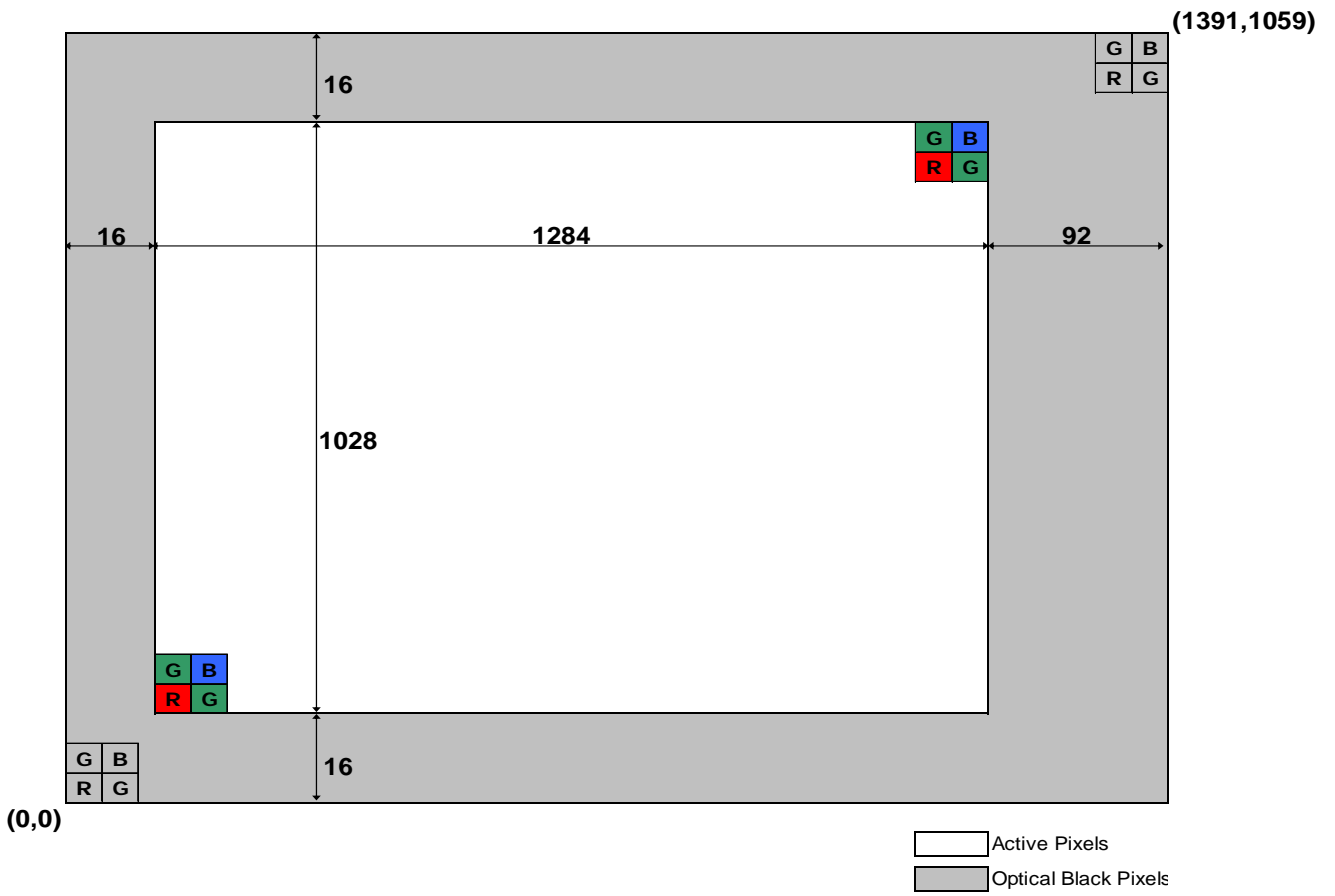


Figure 3: Pixel Array Information

7 Video Output Interface Description

Parallel Output Interface

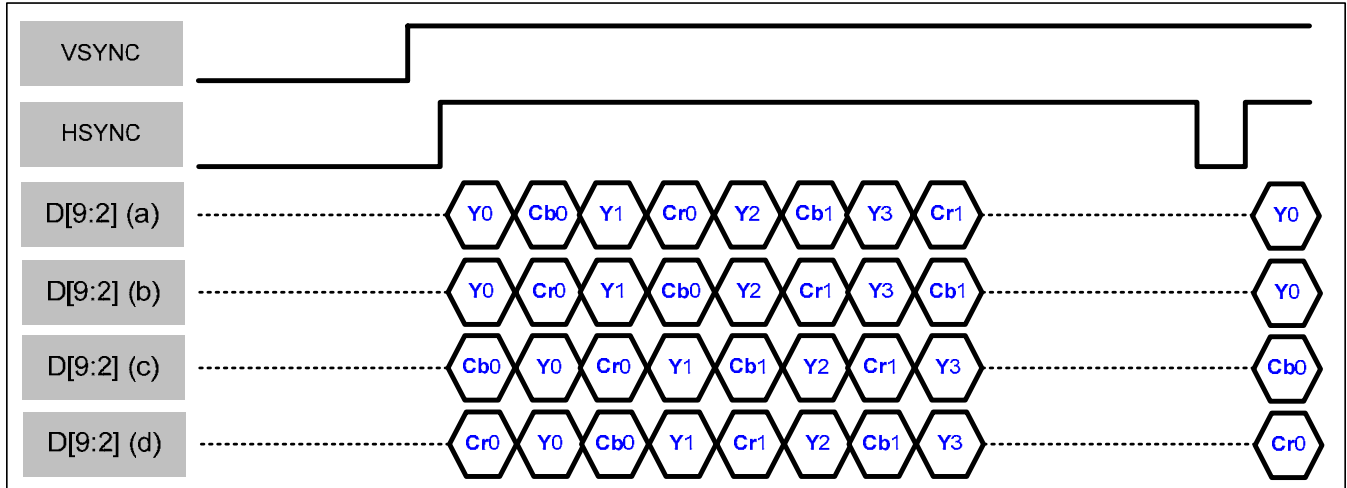


Figure 4: ITU-R.601 YCbCr Data Output Timing

[NOTE] The data output sequence, (a) to (d) can be selected by register setting.

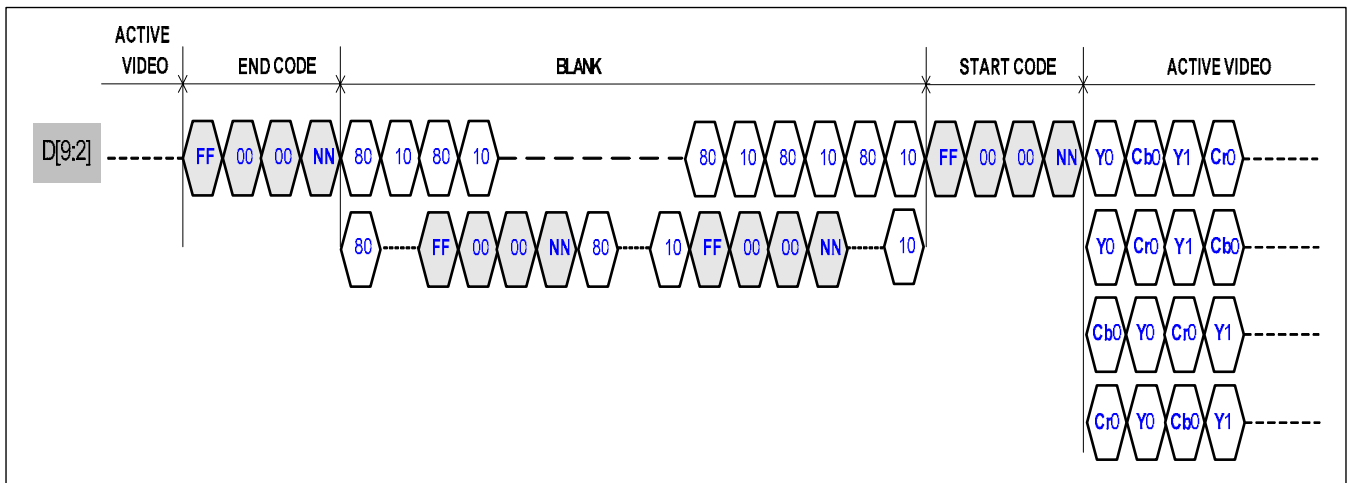


Figure 5: ITU-R.656 YCbCr Data Output Timing

[NOTE]

- (1) The video data is in compliance with Recommendation 656.
- (2) The data words 0 and 255 (00 and FF in hex notation) are reserved for data identification purposes and consequently only 254 of the possible 256 words may be used to express a signal value.
- (3) Each timing reference code consists of a four-word sequence in the following format: FF 00 00 NN.
- (4) The fourth word (NN) contains information, the state of field blanking, and the state of line blanking.
- (5) NN consist of 1(MSB, fixed), F, V, H, P3, P2, P1, P0 (LSB) bits

(F = 0 during field 1, 1 during field 2, V = 0 elsewhere, 1 during field blanking,

H = 0 in SAV (Start of Active Video), 1 in EAV (End of Active Video), P3,P2,P1,P0 : protection bits)

(6) RGB565 is not supported in ITU-R656

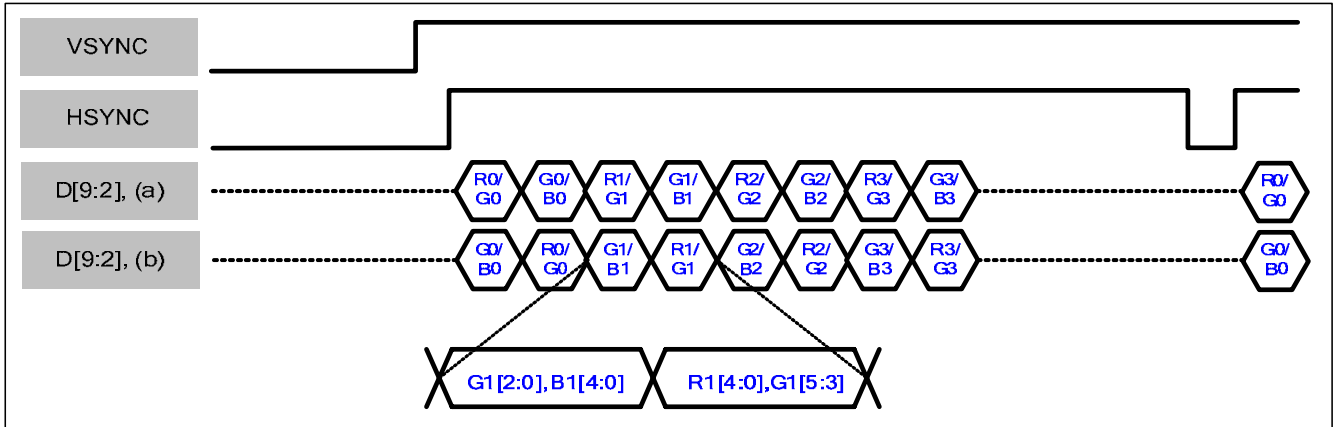


Figure 6: 565RGB Data Output Timing

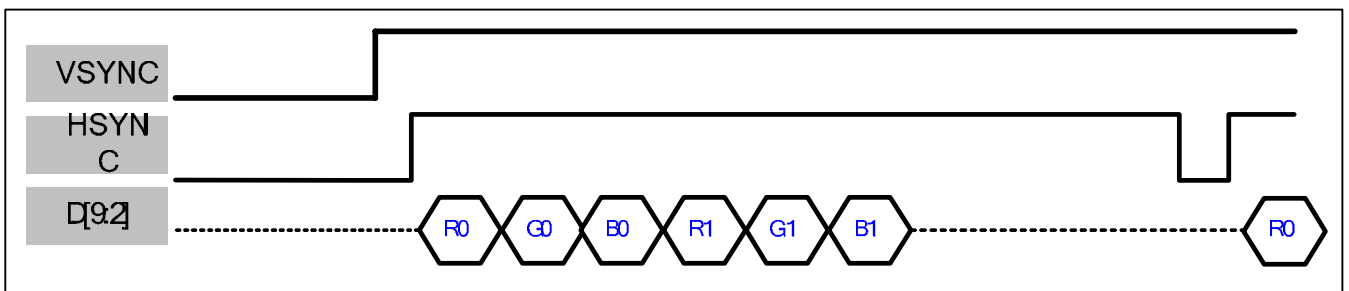


Figure 7: 888RGB Data Output Timing

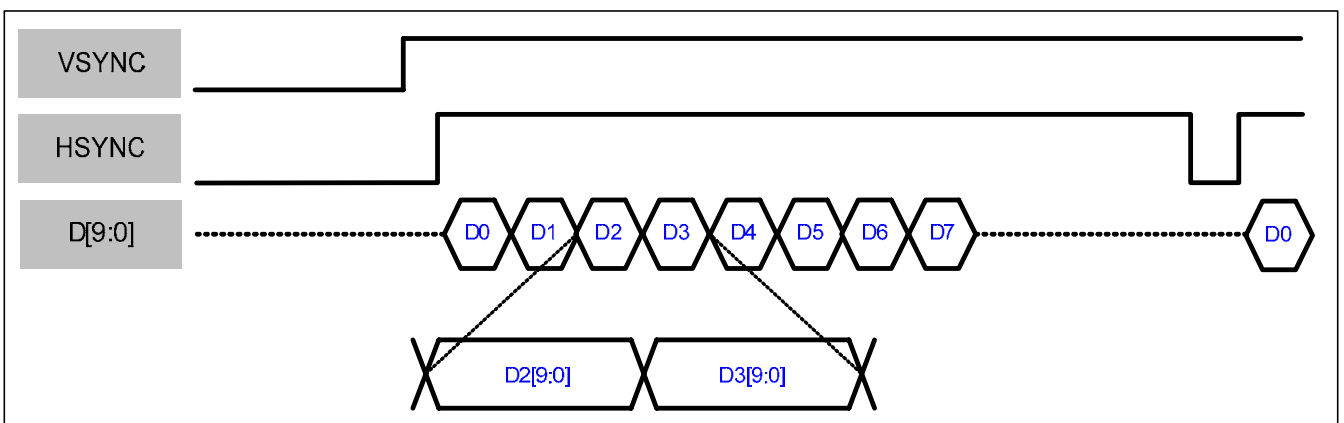


Figure 8: CIS Raw Data Output Timing – RAW10

[NOTE] 10-bit parallel data pads should be bonded for RAW10 interface.

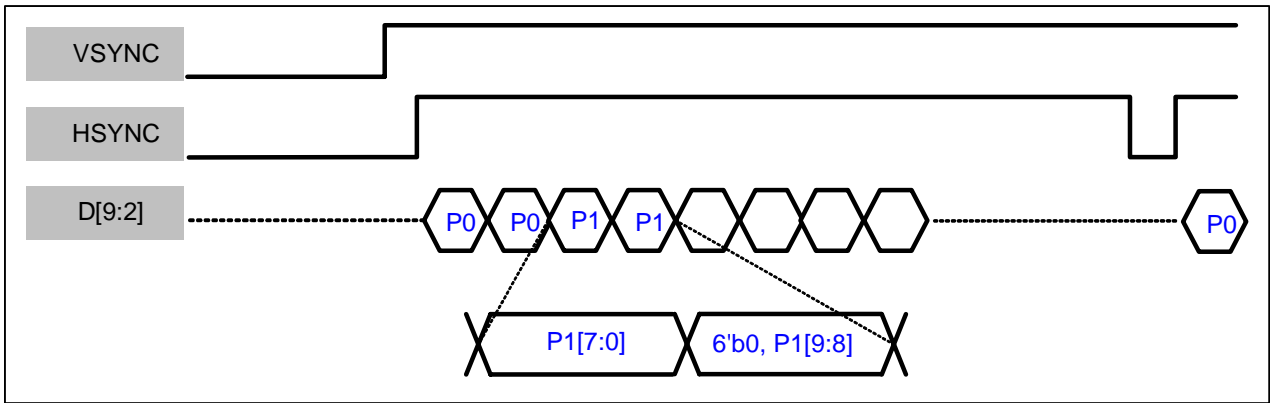
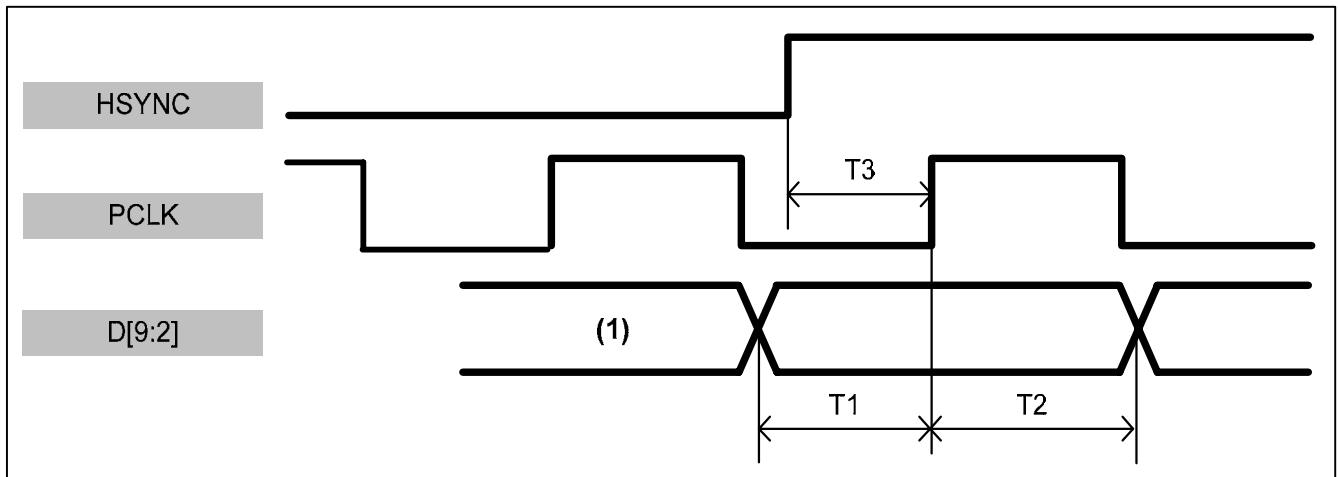


Figure 9: CIS Raw Data Output Timing – RAW10 (8+2)



[NOTE] (1): Blank and start code, otherwise '0' for ITU-R.656 output format:

Symbol	Parameter	Min	Max	Unit
T1	Data Setup Time to PCLK	4	-	ns
T2	Data Hold Time to PCLK	4	-	ns
T3	HSYNC↑ to PCLK↑ delay	4	-	ns

Figure 10: Output Data and Pixel Clock Timing

Serial Output Interface (MIPI CSI-2) with 1-Lane

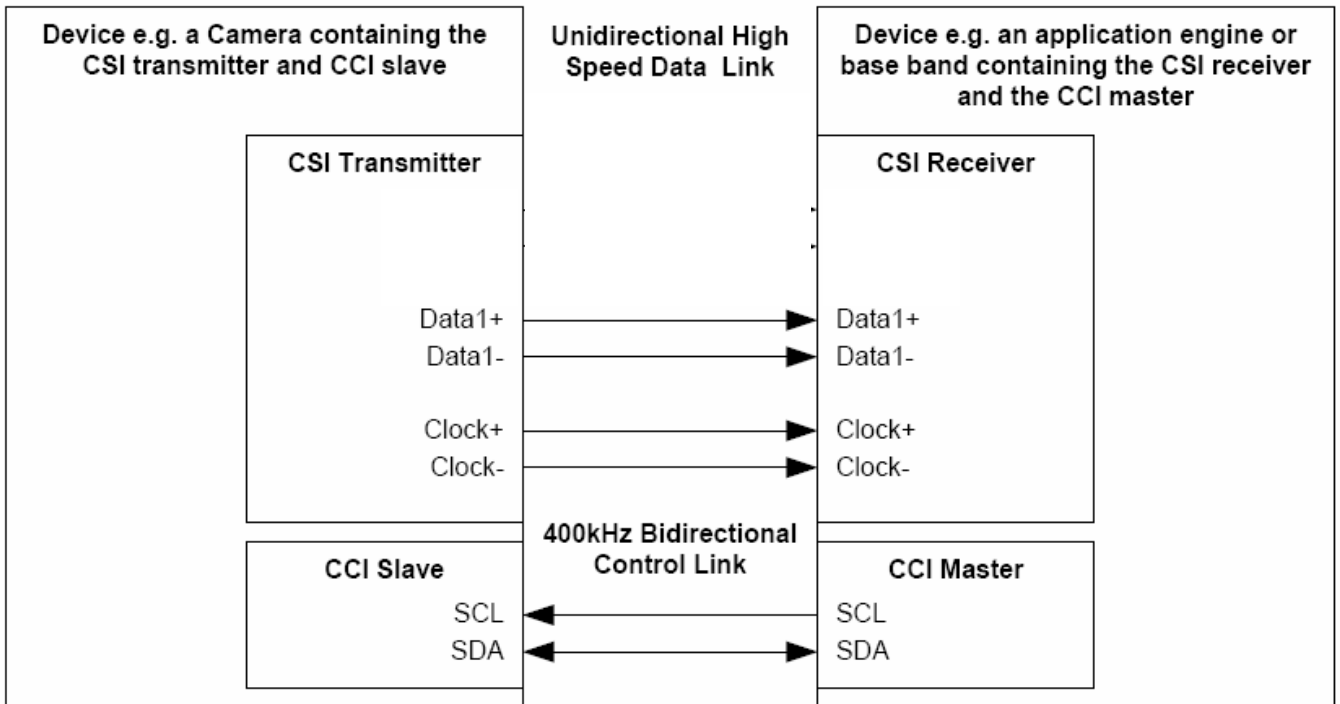


Figure 11: CSI-2 and CCI Transmitter and Receiver Interface

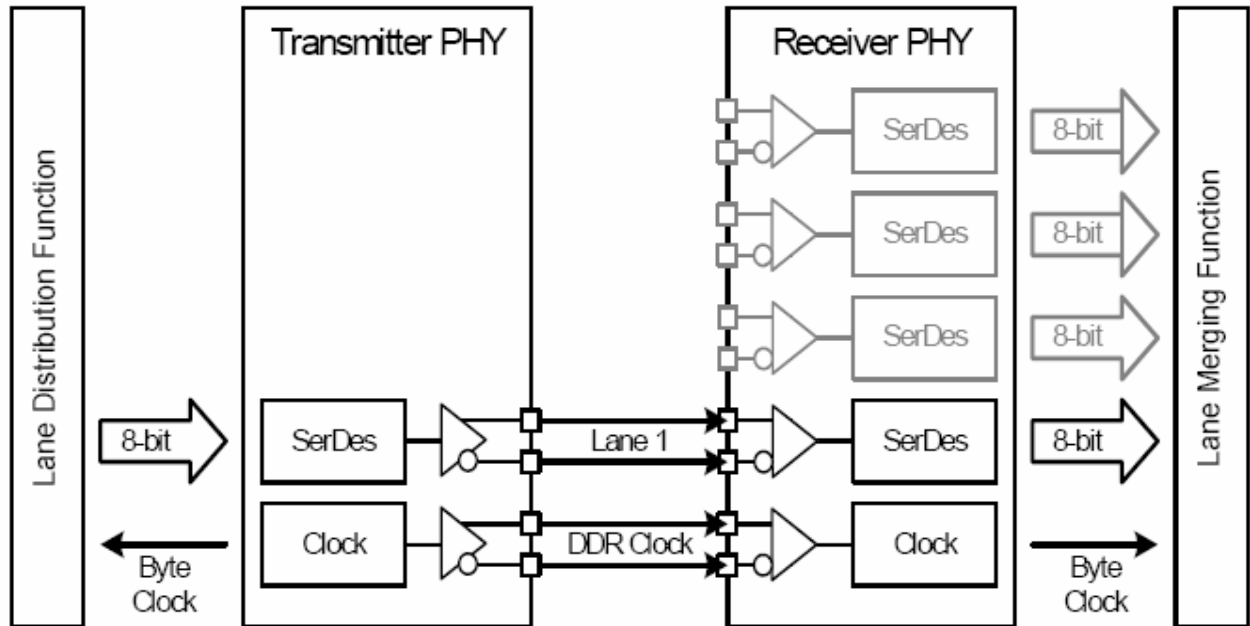


Figure 12: One Lane Transmitter and Four Lane Receiver Example

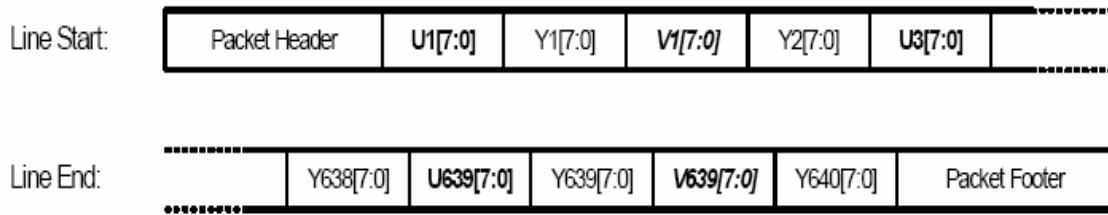


Figure 15: YUV422 Transmission

[NOTE] Byte values transmitted LSB first.

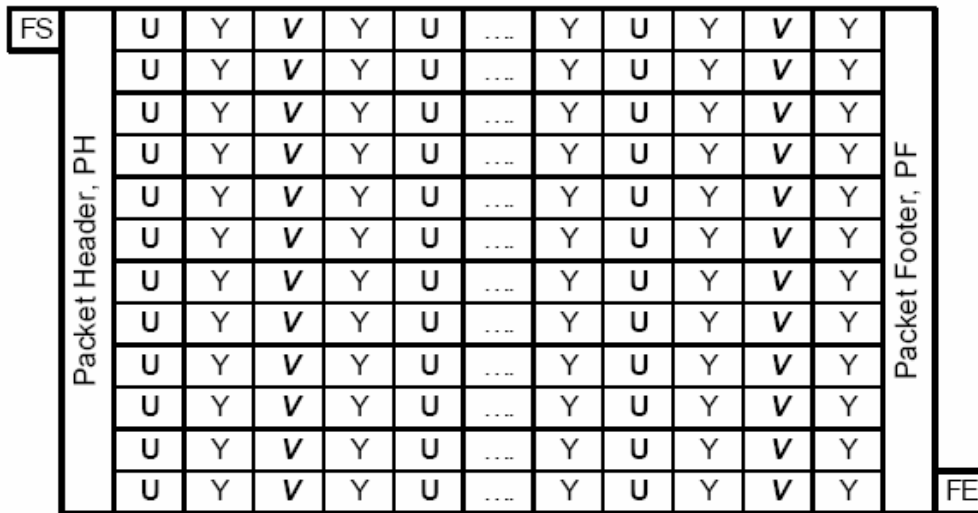


Figure 16: YUV422 Frame Format

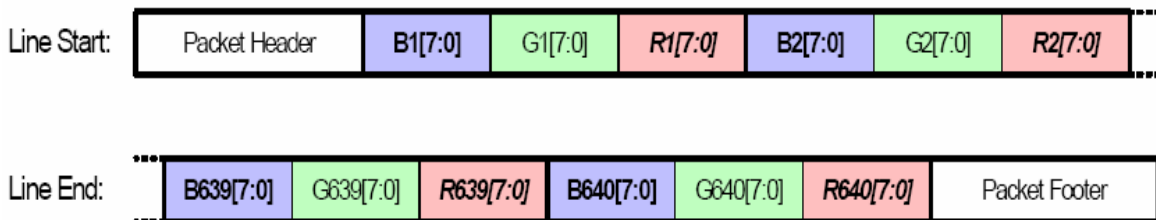


Figure 17: RGB888 Transmission

[NOTE] Byte values transmitted LSB first.

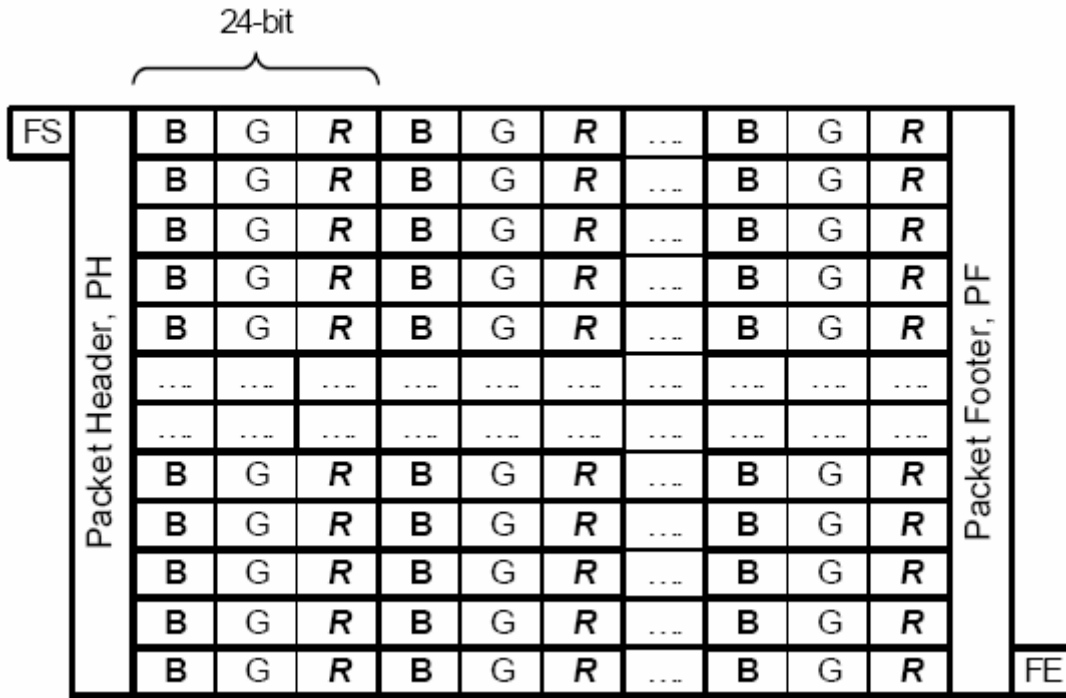
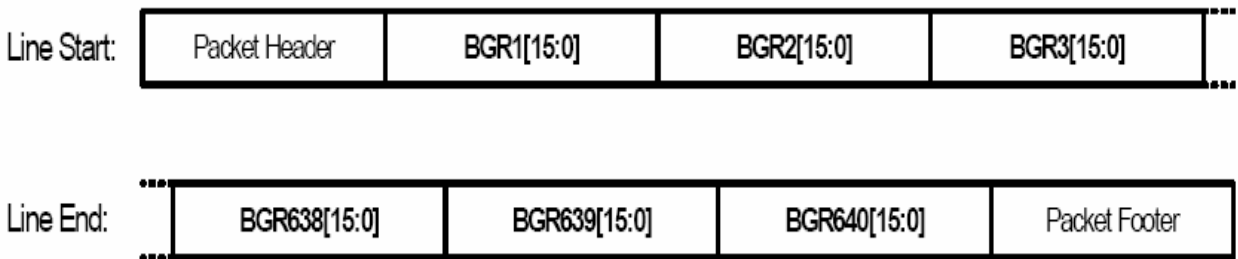


Figure 18: RGB888 Frame Format



[NOTE] Byte values transmitted LSB first.

Figure 19: RGB565 Transmission

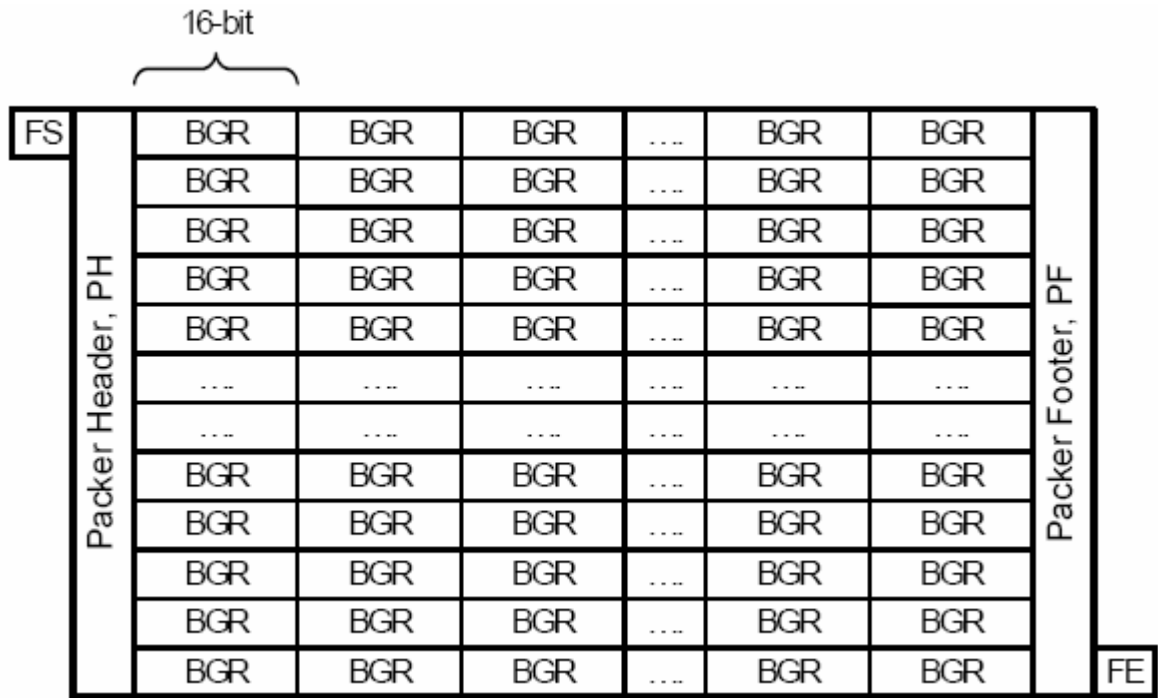


Figure 20: RGB566 Frame Format

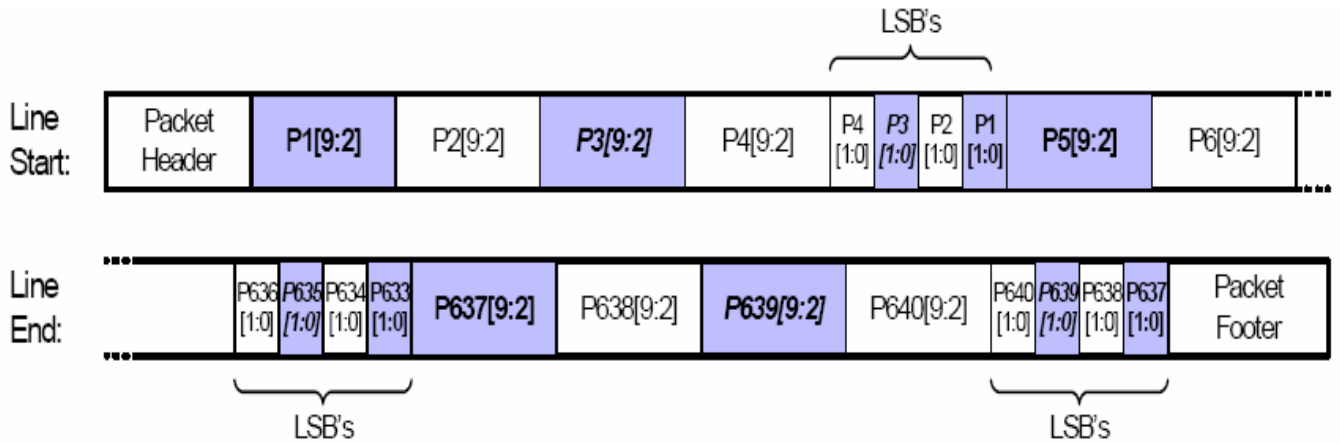


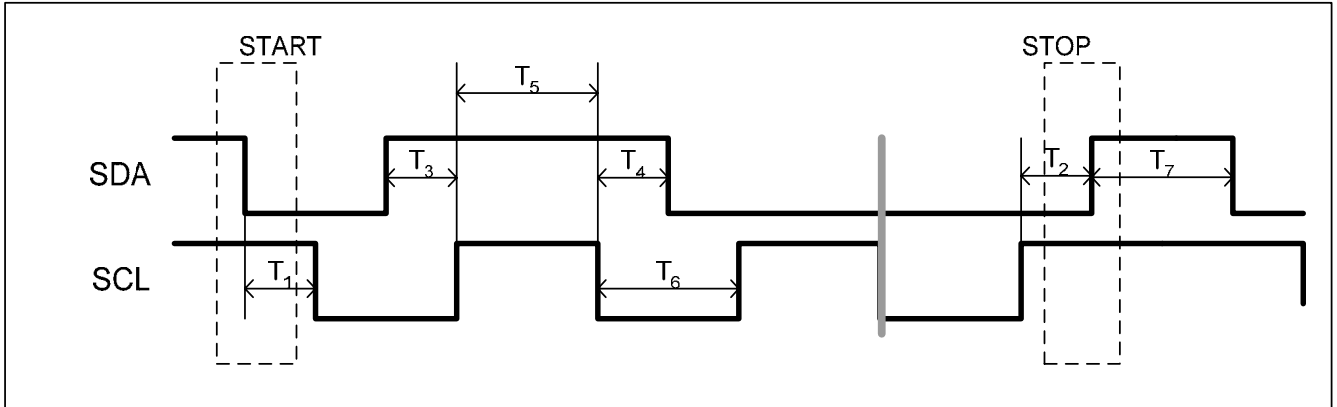
Figure 21: RAW10 Transmission

[NOTE] Byte values transmitted LSB first.

Packer Header, PH	FS	P1	P2	P3	P4	LSBs	P5	...	P637	P638	P639	P640	LSBs	Packer Footer, PF
	P1	P2	P3	P4	LSBs	P5	...	P637	P638	P639	P640	LSBs		
	P1	P2	P3	P4	LSBs	P5	...	P637	P638	P639	P640	LSBs		
	P1	P2	P3	P4	LSBs	P5	...	P637	P638	P639	P640	LSBs		
	P1	P2	P3	P4	LSBs	P5	...	P637	P638	P639	P640	LSBs		
	P1	P2	P3	P4	LSBs	P5	...	P637	P638	P639	P640	LSBs		
	P1	P2	P3	P4	LSBs	P5	...	P637	P638	P639	P640	LSBs		
	P1	P2	P3	P4	LSBs	P5	...	P637	P638	P639	P640	LSBs		
	P1	P2	P3	P4	LSBs	P5	...	P637	P638	P639	P640	LSBs		
	P1	P2	P3	P4	LSBs	P5	...	P637	P638	P639	P640	LSBs		
	P1	P2	P3	P4	LSBs	P5	...	P637	P638	P639	P640	LSBs		
	P1	P2	P3	P4	LSBs	P5	...	P637	P638	P639	P640	LSBs	FE	

Figure 22: RAW10 Frame Format

8 Control Interface Description



Symbol	Parameter	Min	Max	Unit
	SCL clock frequency	0	100	kHz
T1	Hold time for START condition	0.4	-	us
T2	Setup time for STOP condition	4.0	-	us
T3	Data setup time	250	-	ns
T4	Data hold time	0	3.45	us
T5	High period of the SCL clock	4.0	-	us
T6	Low period of the SCL clock	4.7	-	us
T7	Bus free time between STOP and START condition	4.7	-	us
	Rise time for both SDA and SCL signals		1000	ns
	Fall time for both SDA and SCL signals		300	ns
C_B	Capacitive load for each bus line		400	pF

(a) Standard Mode

Symbol	Parameter	Min	Max	Unit
	SCL clock frequency	0	400	kHz
T1	Hold time for START condition	0.6	-	us
T2	Setup time for STOP condition	0.6	-	us
T3	Data setup time	100	-	ns
T4	Data hold time	0	0.9	us
T5	High period of the SCL clock	0.6	-	us
T6	Low period of the SCL clock	1.3	-	us
T7	Bus free time between STOP and START condition	1.3	-	us
	Rise time for both SDA and SCL signals		300	ns



Symbol	Parameter	Min	Max	Unit
	Fall time for both SDA and SCL signals		300	ns
C_B	Capacitive load for each bus line		400	pF

(b) Fast Mode

Figure 23: I²C General Timing Specification

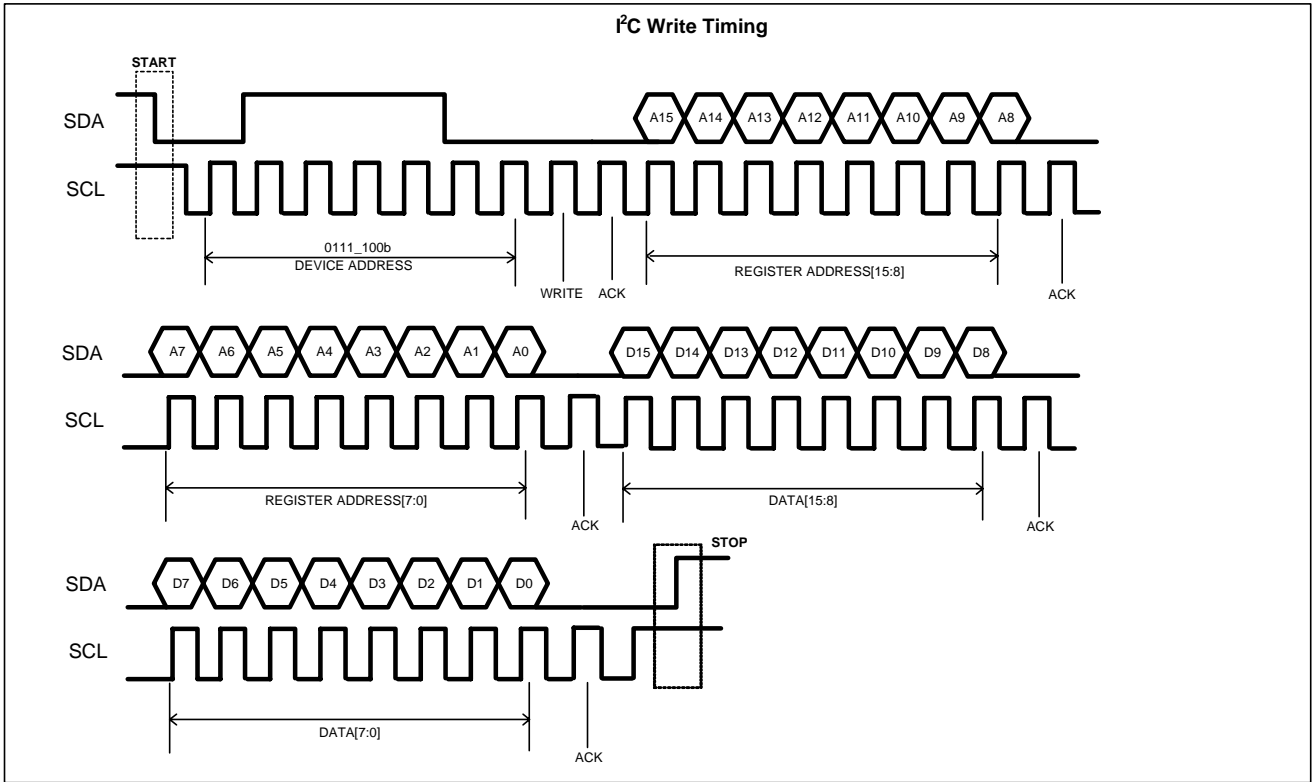
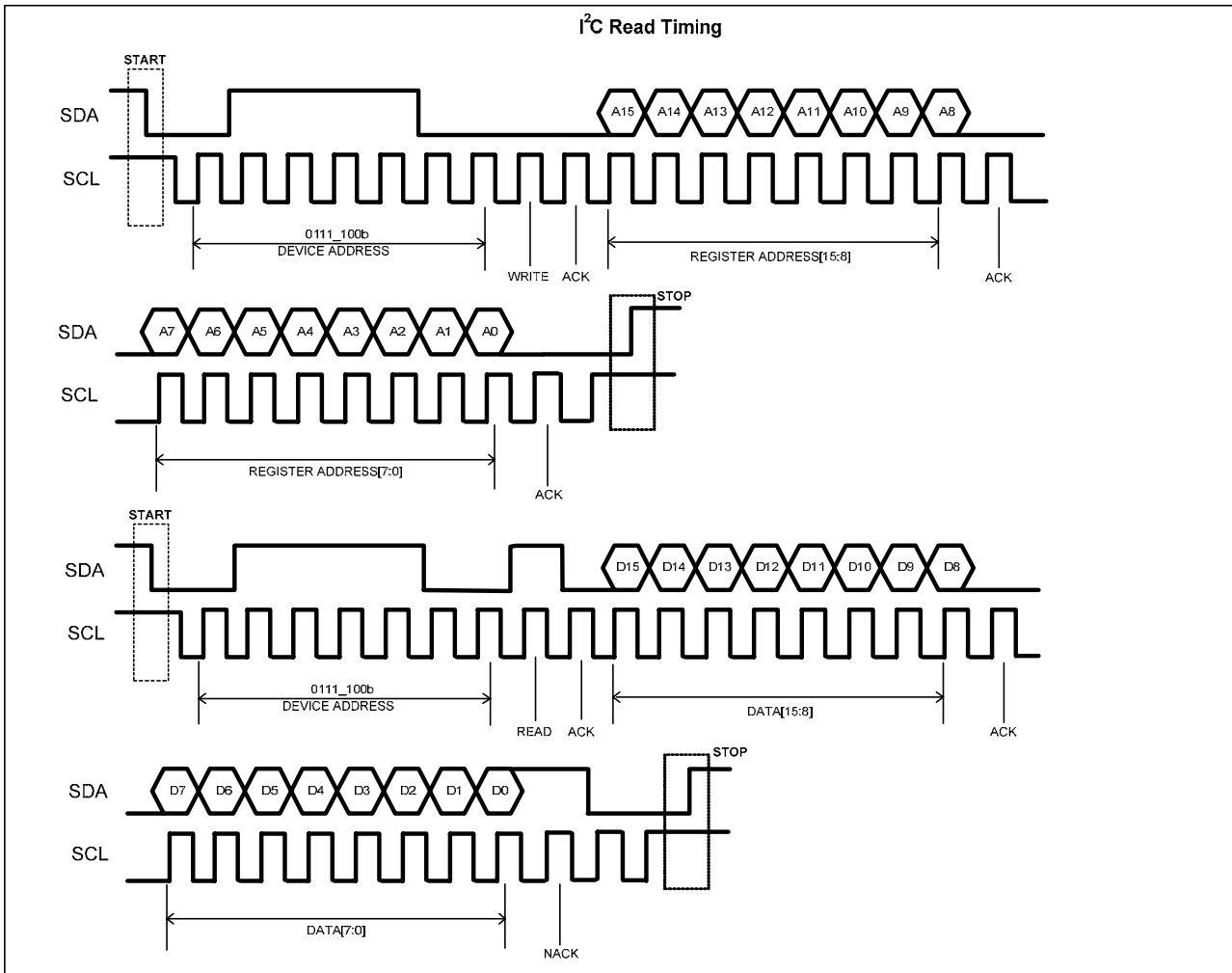


Figure 24: I²C Write Timing Example

[NOTE] The 7bit I2C device address is 0111_100b/78h (write) / 79h (read)



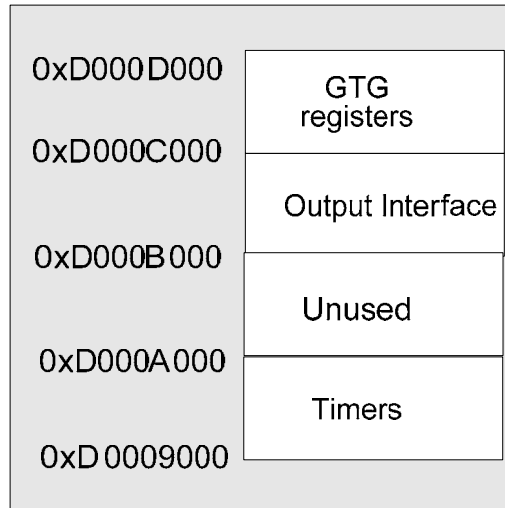
[NOTE] The 7bit I2C device address is 0111_100b/78h (write) / 79h (read)

Figure 25: I²C Read Timing Example

IIC Writing Example

IIC_ID	Device Address
0	0111_100b/78h
1	0101_101b/5Ah

Configure IIC_ID=0, for device address, 0111_100b.



When accessing one of the GTG Registers, its page address is C0. You can access it in either 8-bit access mode or 16-bit access mode.

ex) Writing data(AAh) to register (04h) of page C0 in 8-bit access mode;

```
write(78h, FEh, C0h) // set page C0
write(78h, 04h, 00h) // upper byte
write(78h, 05h, AAh) // lower byte
```

[NOTE] write(device address & R/W bit, register address, data, ...)

[NOTE] All data are regarded as 16-bits.

ex) Writing a series of data to continuous registers of a page (C0h) in 8-bit access mode;

```
data(AAh) -> register(04h)
data(BBh) -> register(06h)
data(CCh) -> register(08h)
data(DDh) -> register(0Ah)
write(78h, FEh, C0h) // set page C0
write(78h, 04h, 00h, AAh, 00h, BBh, 00h, CCh, 00h, DDh)
```

ex) Writing a series of data to continuous registers of a page (C0h) in 16-bit access mode;

```
write(78h, C0h, 04h, 00h, AAh, 00h, BBh, 00h, CCh, 00h, DDh)
```




9 Functional Description

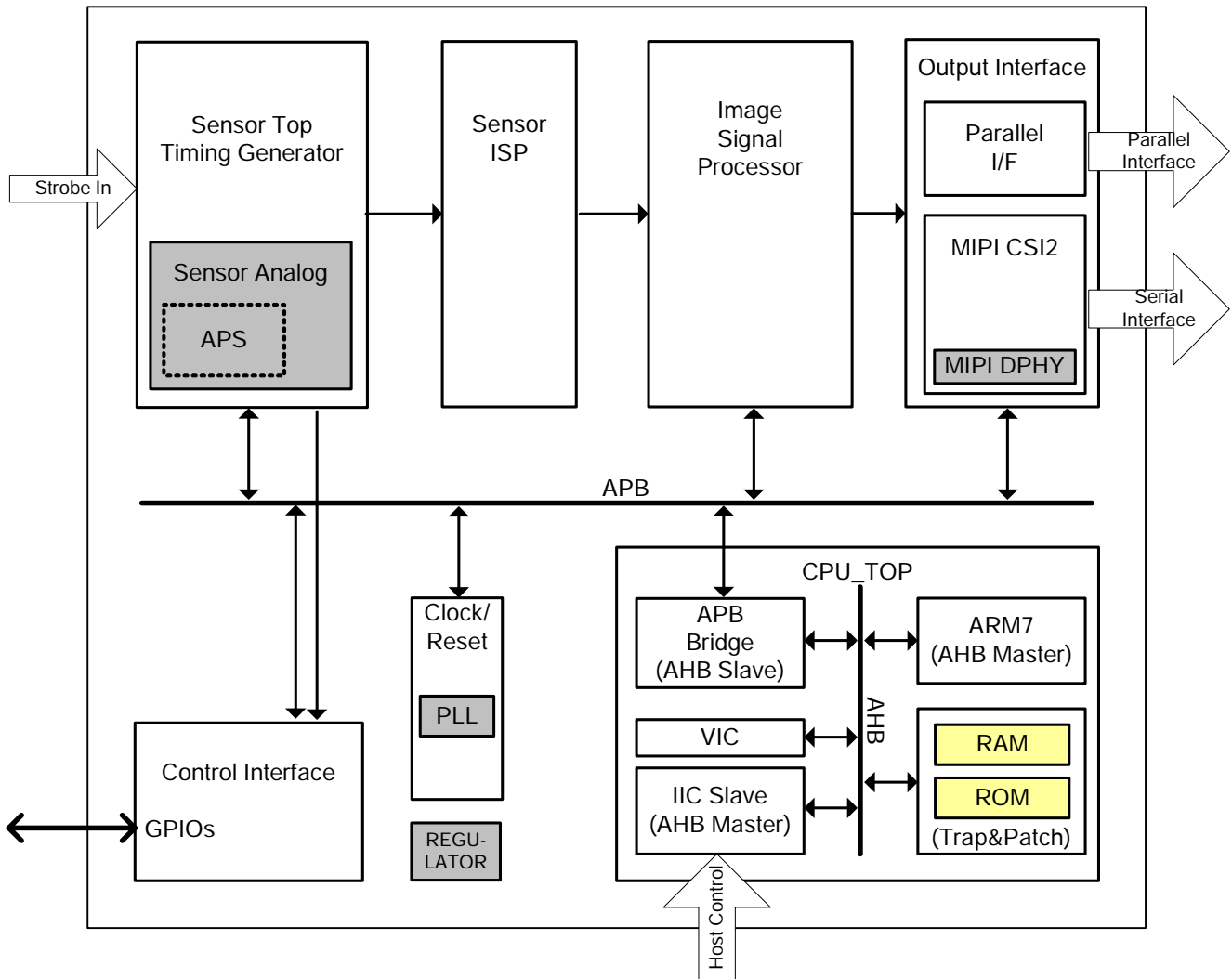


Figure 26: Functional Block Diagram

9.1 Analog to Digital Converter (ADC)

The image sensor has an on-chip ADC. A column parallel ADC scheme is used for low power analog processing.

9.1.1 Correlated Double Sampling (CDS)

The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action and some fixed pattern noise by the in-pixel amplifier offset deviation. To eliminate those noise components, a correlated double sampling (CDS) circuit is used before converting to digital code. The input signal level of each pixel is determined as the differential value between the pre-reset pixel value and its current charged one. Therefore, its value is sampled twice during a pixel period, once for the reference (reset) level detection, and then for the actual signal level.

9.1.2 Programmable Gain

The user can control pixel signal gain using the Gain Control Register. When increasing the signal gain control register, the ADC conversion range slope decreases and its output code value is increased. The gain increases as the following equation:

Analog Gain				
	register gain[7:0]			
	$(\text{Analogue gain}) = 2^{\text{GAIN}[7:5]} \times \left(1 + \frac{\text{GAIN}[4 : 0]}{32} \right)$			

Figure 27: Relative Channel Gain

9.1.3 Programmable Offset

The user can control the offset of pixel signal by dedicated control registers.

9.2 Timing Generator Functions

9.2.1 CIS Raw Data Output

The timing generator supports configurable-bit CIS raw data.

9.3 Pixel Array Addresses

An addressable pixel array is defined as the pixel address range to be read. The addressable pixel array can be assigned anywhere on the pixel array. The addressed region of the pixel array is controlled by the **x_addr_start**, **x_addr_start**, **x_addr_end** and **x_addr_end** registers.

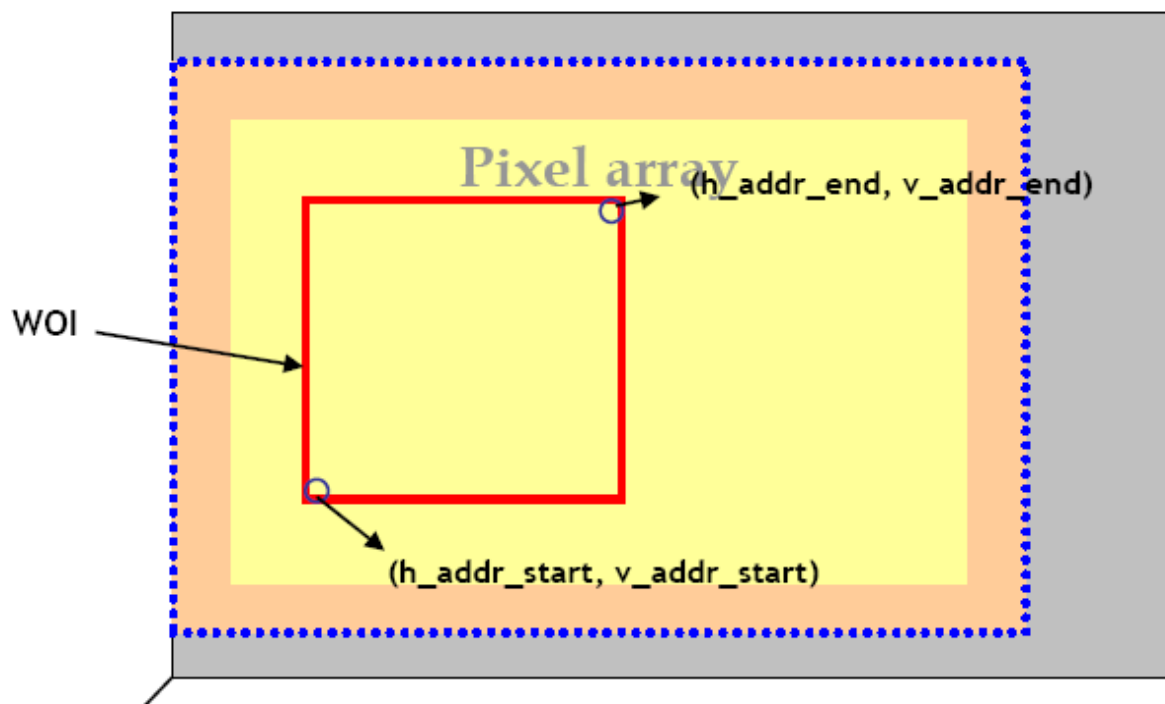


Figure 28: Window of Interest of Pixel Array

9.4 Mirror/Flip

The pixel data is normally read out from left to right in the horizontal direction and from top to bottom in the vertical direction. By changing the *mirror/flip* mode, the read-out sequence can be reversed, and the resulting image can be flipped like a mirror image. Pixel data is then read out from right to left in horizontal mirror mode and from bottom to top in vertical flip mode. The horizontal mirror and the vertical flip mode can be programmed by the image orientation register.

The sensor module supports four possible pixel readout orders, as described in the sections below.

9.5 Standard Readout

The addressed region of the horizontal pixel data output is controlled by the *x_addr_start*, *x_addr_end* register, and the addressed region of the vertical pixel data output is controlled by the *y_addr_start*, *y_addr_end* register.

9.6 Horizontally Mirrored and Vertically Flipped Readout

The addressed region of the horizontal pixel data output is controlled by the *x_addr_end*, *x_addr_start* registers, and that of the vertical pixel data output is controlled by the *y_addr_end*, *y_addr_start* registers.

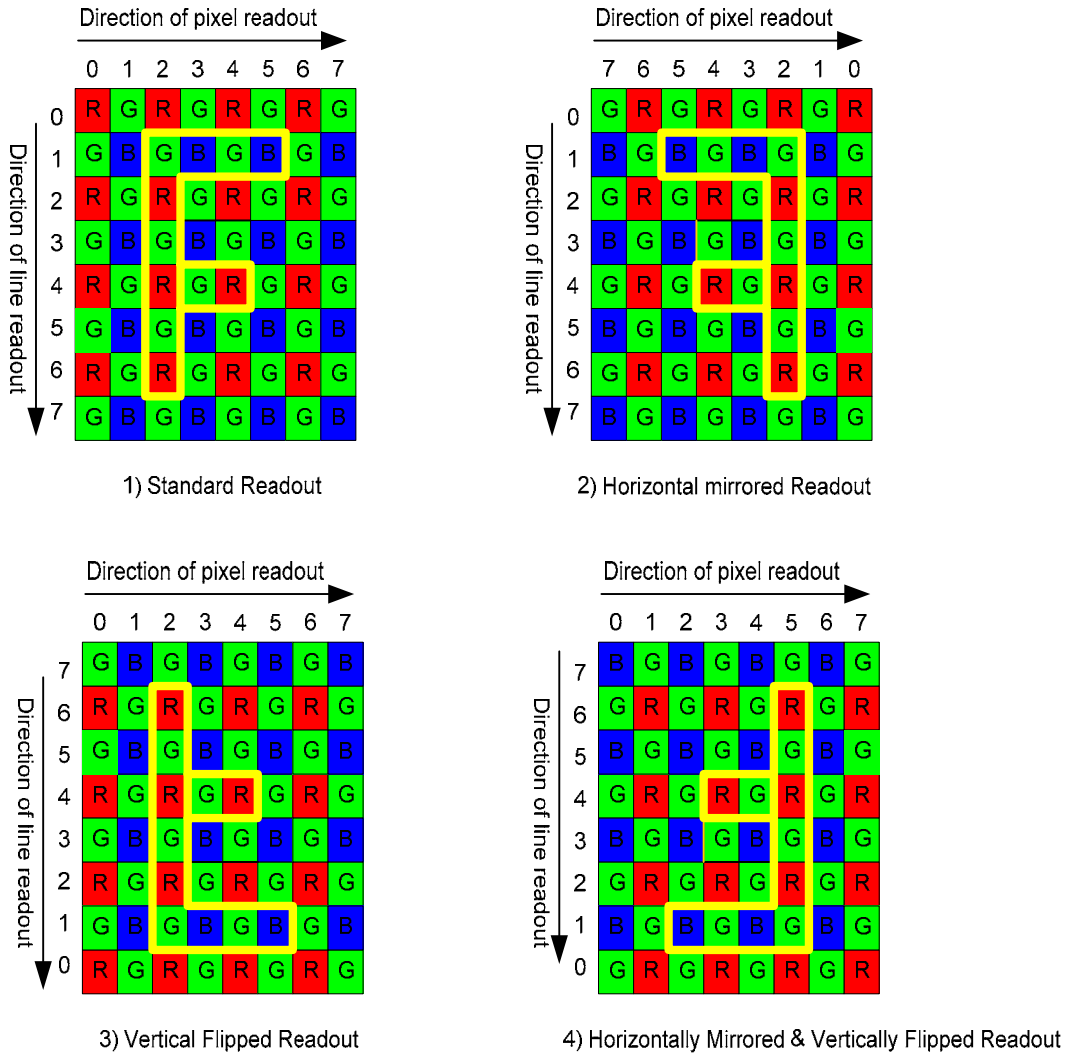


Figure 29: Horizontal Mirror and Vertical Flip

9.7 Sub-Sampled Readout

By programming the x and y odd and even increment registers (x_even_inc, x_odd_inc, y_even_inc, y_odd_inc), the sensor can be configured to read out sub-sampled pixel data.

[NOTE] All figure examples are related to the red first array structure. The timing generator also supports green first array structures.

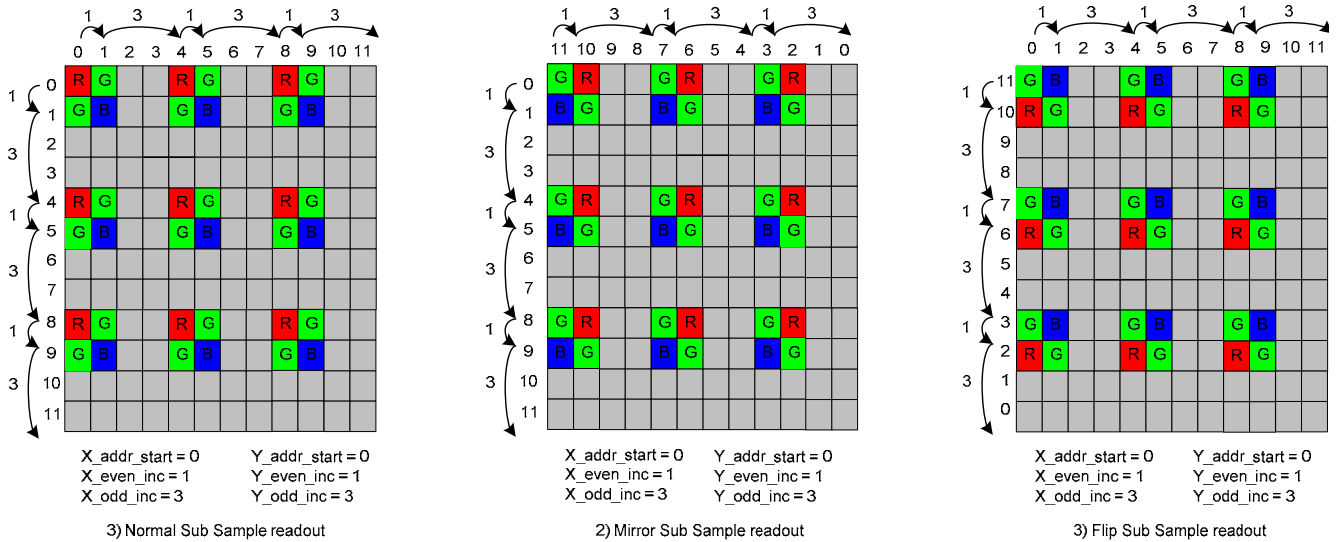


Figure 30: Sub-Sampled Readout

9.8 Frame Rate Control (Virtual Frame)

The line rate and the frame rate can be changed by varying the size of the virtual frame. The virtual frame's width and depth are controlled by the line_length_pck and frame_length_lines register. The horizontal and vertical blanking times (horizontal blanking time: line_length_pck – x_output_size, vertical blanking time: frame_length_lines – y_output_size) should meet system requirements.

$$\text{Frame rate} = \text{TGCLK} / (\text{frame_length_lines} * \text{line_length_pck})$$

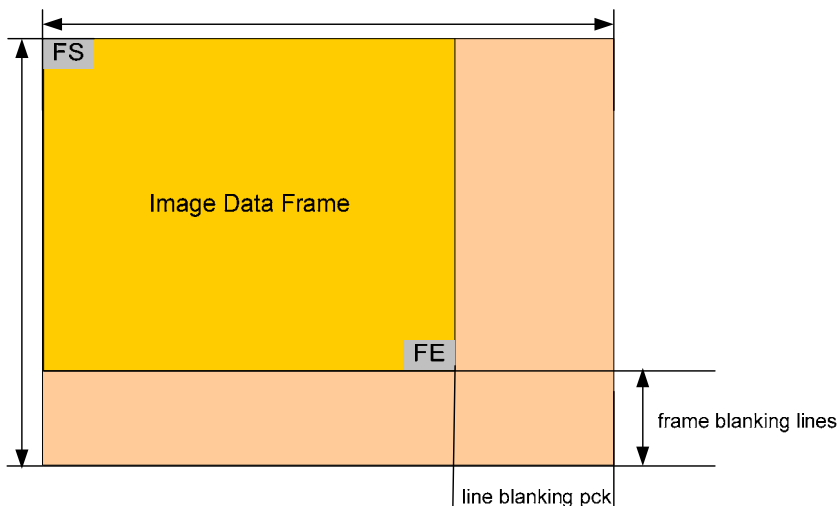


Figure 31: Virtual Frame Timing

9.9 Integration Time Control (Electronic Shutter Control)

The pixel integration time is controlled by the shutter operation. During the shutter operation, the amount of time – integration time – is determined by the column Step Integration Time Control Register (fine_integration_time) and the line Step Integration Time Control Register (coarse_integration_time). The total integration time of the sensor module can be calculated using the following formula:

$$\text{Total_integration_time} = \{(\text{coarse_integration_time} * \text{line_length_pck}) + \text{fine_integration_time} + \text{const}\} * \text{pclk period [sec]}$$

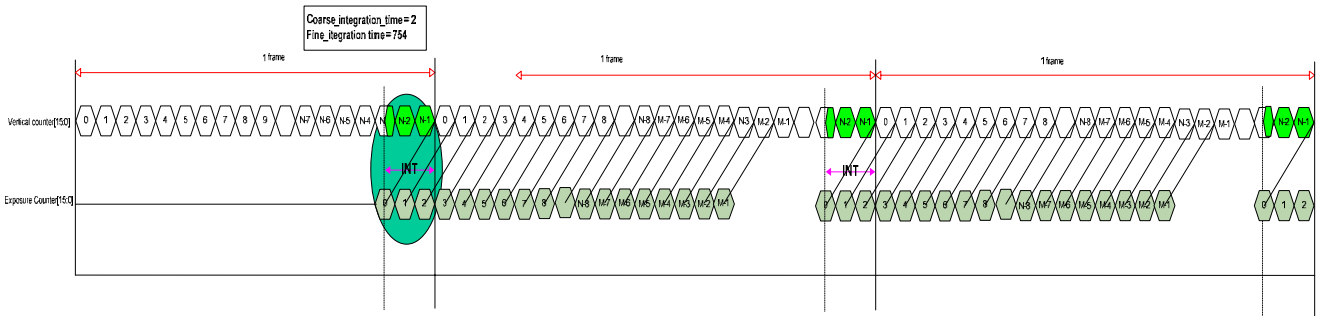


Figure 32: Integration Time Counter Diagram

9.9.1 LED and Xenon Flash Control

Both devices are controlled by the firmware and activated directly by the sensor. If the Xenon flash is used, it is the host’s responsibility to charge the flash device prior to its activation using the register-based interface.

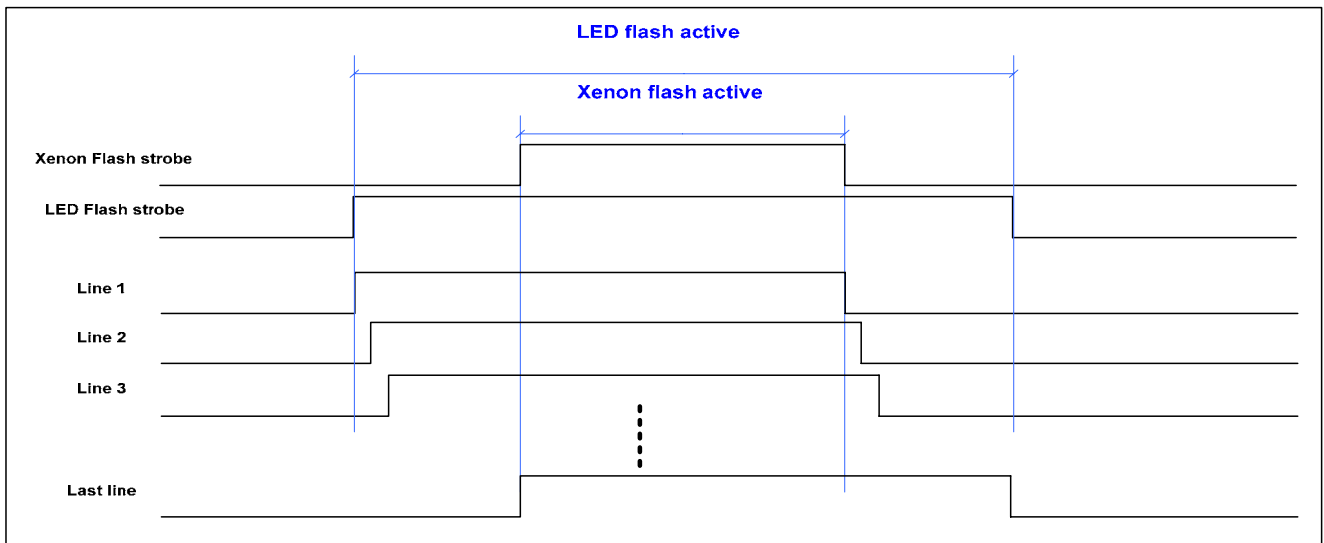
9.9.2 Register-Based Host Interface

The following registers control the flash status and functionality:

REG_TC_FLS_Mode	Sets flash mode according to TC_FlashSt_type enum.
REG_TC_FLS_Threshold	Sets flash activation threshold in normalized brightness units.
REG_TC_FLS_Polarity	Sets flash device polarity. 1: active high, 0: active low
REG_TC_FLS_XenonMode	Sets Xenon flash mode according to TC_XenonMode_type enum.
REG_TC_FLS_XenonPreFlashCnt	Number of Xenon pre-flash strobes (minimum 1).

[NOTE]

- There is no guarantee for the quality of AE or any other algorithm convergence before the flash capture. There is typically only one frame for convergence. This time frame is too short, and the results may not be perfect.
- Using an extra frame for AE or AWB convergence extends the preview to capture time. Typically, it doubles this period.
- Xenon strobe is done when all the frame lines are exposed simultaneously. If the exposure time is too short, there might not be such a time period. For this reason, Xenon flash will only be activated if long exposure is required (i.e. dark scenes). In some cases, using the Xenon device may extend the exposure time in order to allow for a longer strobe period.



Following are application examples for each flash device type. Please note that when LED is used, the host is responsible for algorithm convergence prior to capture, whereas when Xenon is used, the FW is responsible for algorithm convergence. The reason for this is that Xenon activation requires tight FW synchronization that cannot involve the host. Dedicated flash algorithm convergence code can be added to the FW using a special SW hook function that is loaded to the FW during initialization.

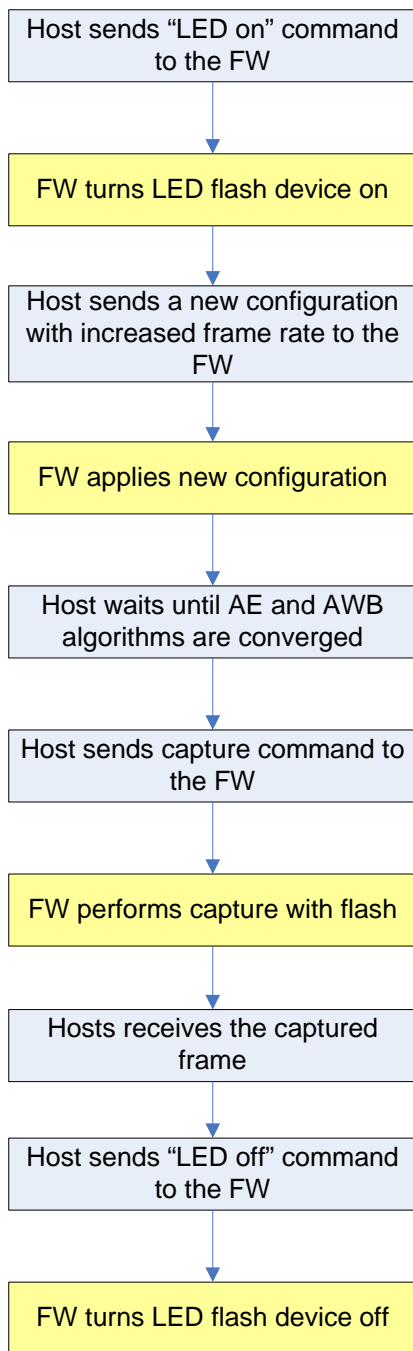


Figure 33: LED Flash Capture Sequence

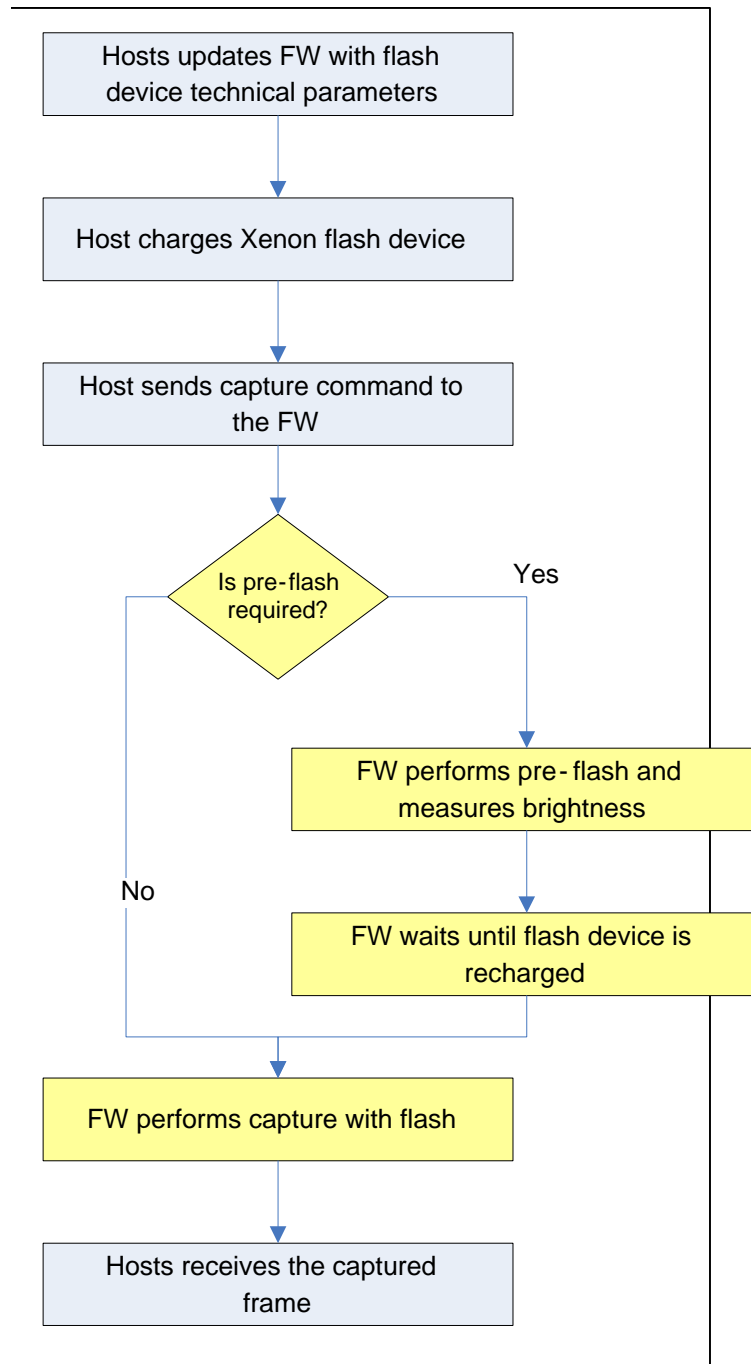


Figure 34: Xenon Flash Capture Sequence

9.10 Image Signal Processor

9.10.1 Auto Exposure

The embedded AE control algorithm tracks the change of the luminance in selected windows, and then compares it to the AE target value. The target value varies according to the scene type. The image brightness is adjusted by controlling analog and digital gains, and image sensor integration time. The AE algorithm is designed for fast convergence and may adapt very quickly to dynamic illumination changes.

9.10.2 Auto White Balance

The AWB algorithm alters the color components of the image in order to ensure that the white color appears white under all illumination types. The algorithm uses three different statistics channels – one per illumination group (warm, outdoor and general). Each channel filters the image pixels based on R-gain / B-gain plane polygon.

The algorithm includes a scene type detector (six scene types).

9.10.3 Auto Flicker Correction

Flicker may occur when the sensor integration time is not an integer multiple of the frequency of electrical network, for example under a 50Hz or 60Hz fluorescent lamp. The flicker is detected using a dynamic algorithm and can be corrected by adjusting the integration time to some limited values. If the exposure value is smaller than 1/100 of a second (or 1/120, depending on the lighting frequency), flicker band noise may be seen in an office environment.

9.10.4 Lens Shading Correction

Two different methods of shading correction are used –one uses parabolic shading compensation, and the other removes residual effects and is based on a grid model. Shading correction dynamically changes based on illumination type.

9.10.5 Color Demosaicking

Each Bayer color pixel from the image sensor is converted into an RGB pixel, and the missing color information of a Bayer pixel is derived from the value of adjacent pixels. The algorithm uses several special-purpose approaches such as text and natural modes. Separate decisions are made for each pixel in the image.

9.10.6 Color Correction

Variable color profiles are used for color representation improvement. The decision about the profile is taken based on scene brightness and illumination type. Color correction is done using non-linear transformation, parameterized by 18 coefficients, based on ICC device-link technology.

9.10.7 Despeckle

This algorithm detects and replaces isolated bad pixels and pixel pairs on the raw image data based on their neighbors' pattern and average.

9.10.8 Denoising

The denoising algorithm implements the "edge-preserving smoothing" algorithm. It averages pixels that are close in value to the central pixel. Neighboring pixels are equalized before averaging.

9.10.9 Gamma Correction

Five Gamma correction tables are used for the following color components:

- R, G and B – Contrast and device correction
- Y – Luminance correction
- UV – For color saturation correction

9.10.10 Image Downscaling

The image from the sensor can be downscaled to an arbitrary size with even X and Y dimensions. The downscaling accuracy ensures any output size up to a 3-5 pixel variance. More precise output sizes can be achieved by cropping. Among other resolutions, 720p, SVGA, VGA, QVGA, QQVGA, CIF, and QCIF resolutions are supported. In order to increase the frame rate, vertical sub-sampling (with horizontal scaling) is supported for output sizes of VGA and below.

9.10.11 Special Effects

The special effects may be used to create a Sepia (warm tone), Aqua (cool tone), Monochrome, Negative or Sketch effect on Image.

9.10.12 Output Formatting

The ISP outputs 8-bit processed video data in the form of standard YUV ITU-R.656/601 or RGB data. Raw sensor data in Bayer format may also be outputted with 8-10 bit accuracy.

9.10.13 Image Properties Controls

The user may dynamically control the following image properties independently: Brightness, Contrast, Saturation, Sharpness, Glamour.

10 System State Diagram

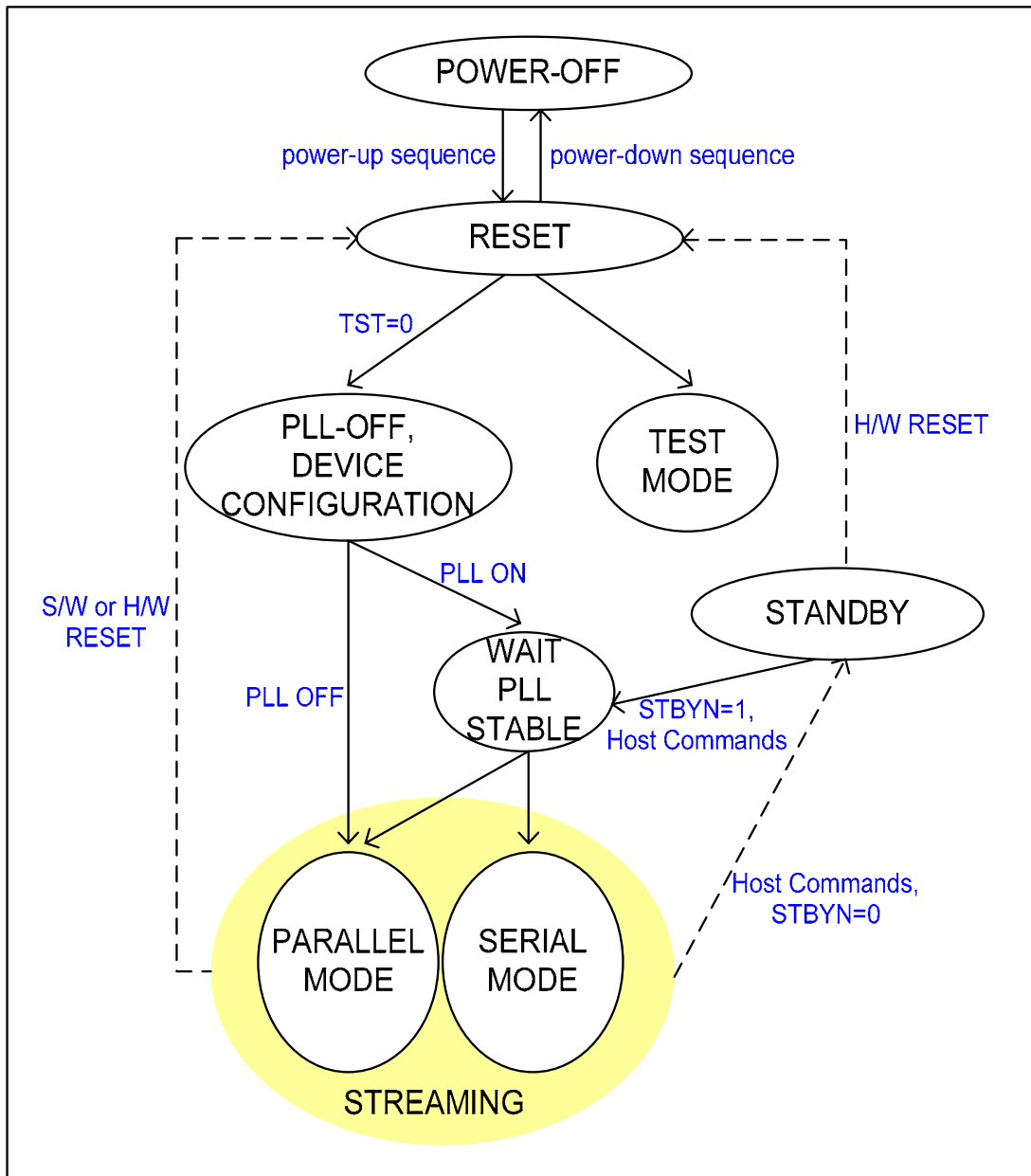


Figure 35: System State Diagram

11 Power-Up/Down Sequence

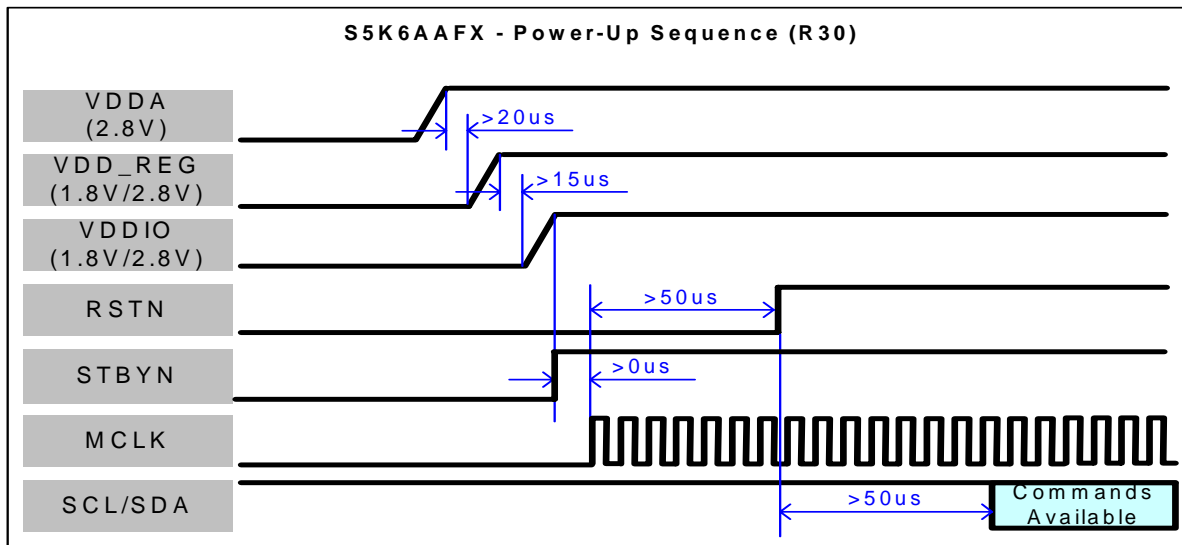


Figure 36: Power-Up Sequence

[NOTE] If an internal regulator is not used, open VDD_REG and apply VDD15, where the power-up sequence is the same as VDD_REG.

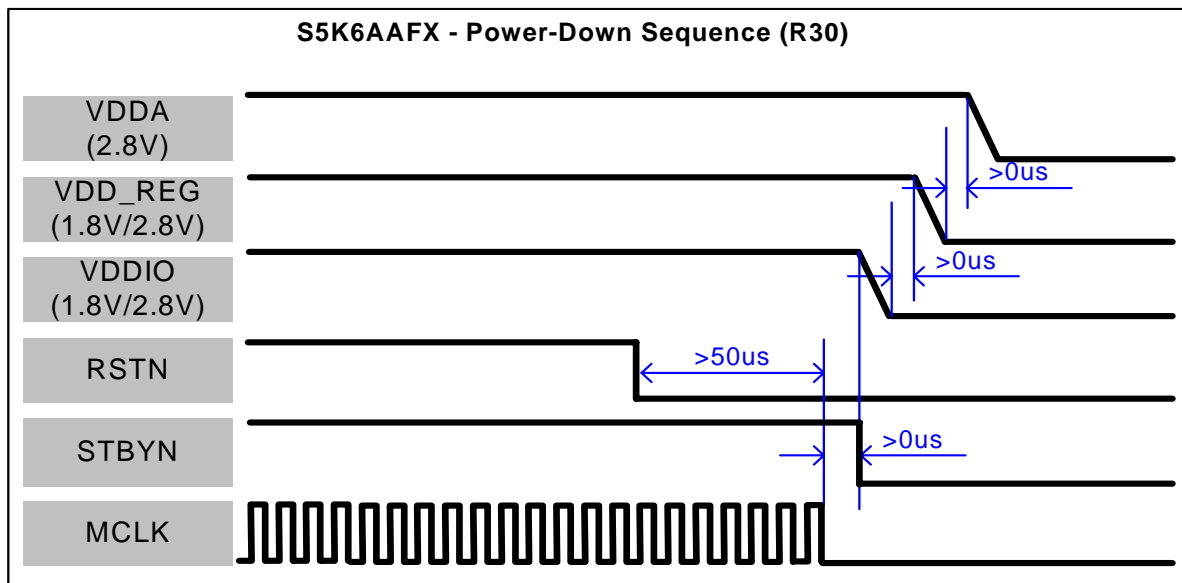


Figure 37: Power-Down Sequence

[NOTE] If an internal regulator is not used, open VDD_REG and apply VDD15, where the power-down sequence is the same as VDD_REG.

12 Standby Sequence

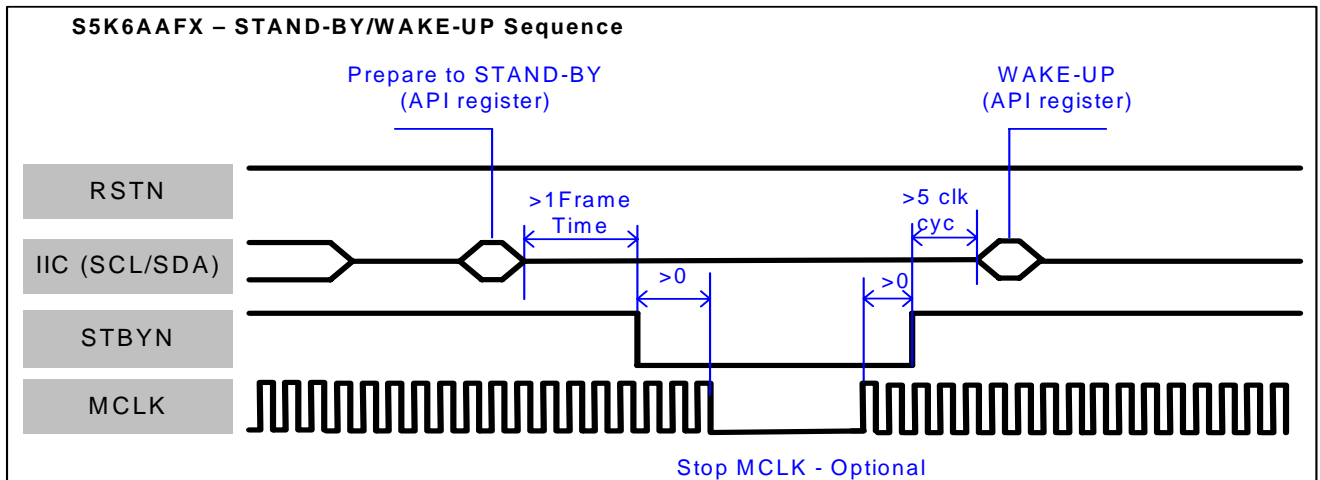


Figure 38: Standby/Wakeup-Sequences

Enter STAND-BY:

- Write via IIC API register: prepare to STAND-BY (Refer to application notes)
- Assert STBYN pin ('0')
- Stop MCLK (Optional)

Exit STAND-BY (WAKE-UP):

- Provide MCLK
- De-assert STBYN pin ('1')
- Write via IIC API register: Wake up (Refer to application notes)

13 Electrical Characteristics

Table 2: Absolute Maximum Rating

Parameter	Symbol	Value	Unit
I/O Digital Power (2.8V or 1.8V)	V_{DDIO}	-0.3 to 3.8	V
Analog Power (2.8V)	V_{DDA}	-0.3 to 3.8	
Core Digital Power (1.5V)	V_{DDD}	-0.3 to 2.0	
Input Voltage	V_I	-0.3 to 3.8	
Ambient Temperature	T_A	-20 to +60	°C
Storage Temperature	T_S	-40 to +85	

Table 3: DC Characteristics

($V_{DDIO1} = 2.8V \pm 0.2V$, $V_{DDIO2} = 1.8V \pm 0.15V$, $V_{DDD} = 1.5V \pm 0.1V$, $T_a = -20$ to $+60$ °C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DDA}		2.6	2.8	3.0	V
	V_{DDD}		1.40	1.5	1.60	
	V_{DDIO1}		2.6	2.8	3.0	
	V_{DDIO2}		1.65	1.8	1.95	
High-Level Input Voltage	V_{IH}		0.7* V_{DDIO}	-	-	V
Low-Level Input Voltage	V_{IL}		-	-	0.2* V_{DDIO}	
High Level Output Voltage	V_{OH}		$V_{DDIO}-0.2$	-	-	
Low-Level Output Voltage	V_{OL}		-	-	0.2	
High-Level Input Current	I_{IH}	$V_I = V_{DDIO}$	-10	-	10	uA
		$V_I = V_{DDIO}$ (with Pull-Down)	-	-	72	
Low-Level Input Current	I_{IL}	$V_I = V_{SS}$	-10	-	10	
		$V_I = V_{SS}$ (with Pull-Up)	-72	-	-	
Standby Current	I_{STBY}	STBYN = Low, MCLK = Low (0 lux Illumination)	-	35	200	
Supply Current (Digital)	I_{DDD}	Parallel Output Mode @15fps	-	110	120	

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Current (Analog)	I_{DDA}	Parallel Output Mode @15fps	-	35	45	
Supply Current (Analog)	I_{DDIO} (2)	Parallel Output Mode @15fps	-	35	45	
Power Consumption	P_{DD}	Parallel Output Mode @15fps	-	359	423	mW
Input Capacitance	C_{IN}		-	-	5	pF

[Notes]

- (1) 2.8V input to regulator is not recommended due to increased power consumption.
- (2) I_{DDIO} is affected by external PCB capacitance.

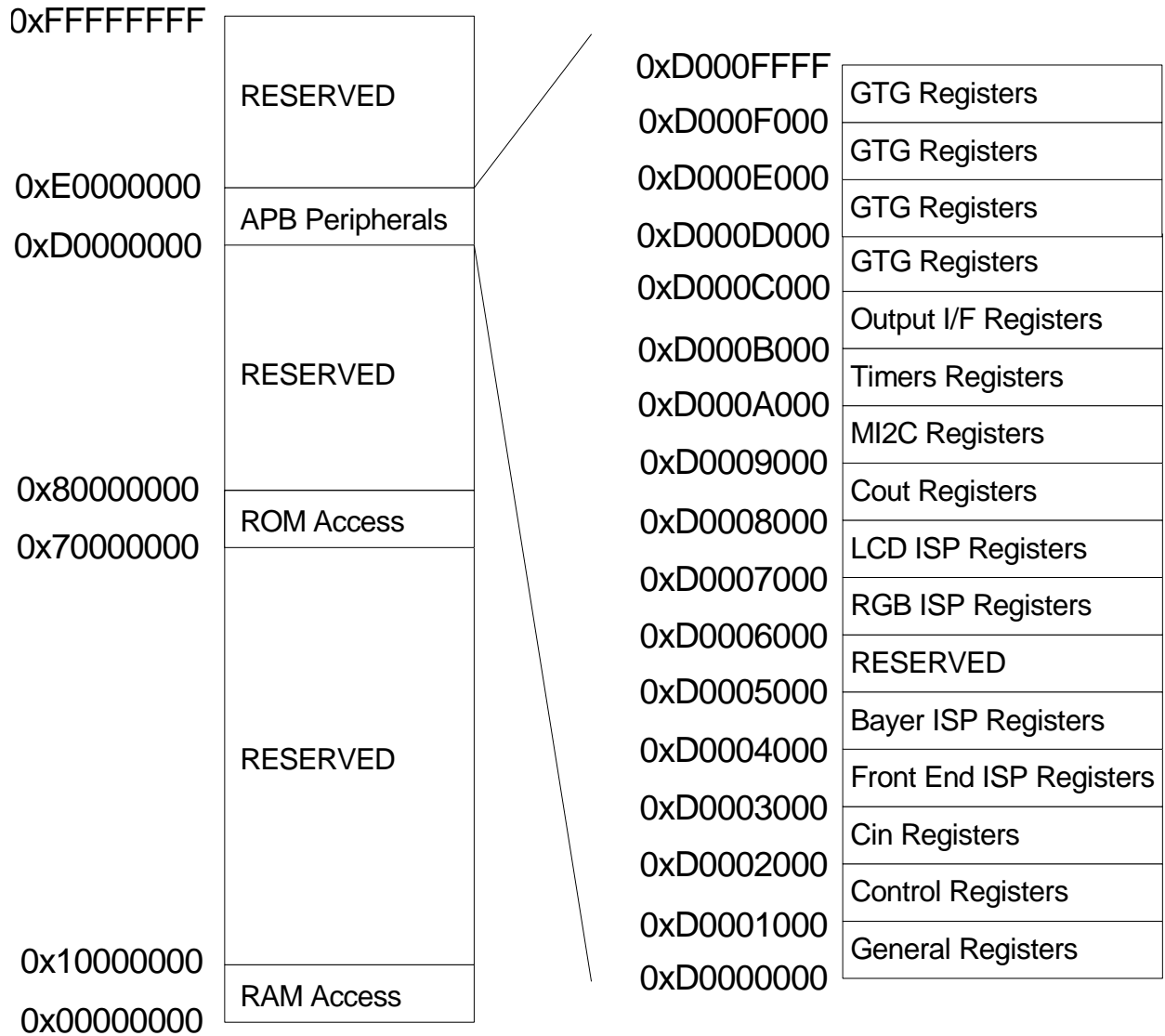
14 Imaging Characteristics

Table 4: Imaging Characteristics

Parameter	Unit	Value	Remark
Effective resolution	pixel	1280 x 1024	
Active resolution	pixel	1284 x 1028	
Optical format	Inch	1/6	
Pixel size	Um	1.75um	
Shutter type	-	Electronic rolling shutter	
Full saturation	mV	>900	
ADC saturation	mV	750	
Sensitivity@Green	mV/lux.sec	600	
Dark current	mV/sec	<5	
Random noise	e-	3	
Dynamic range	dB	>60	
Max. SNR	dB	38.3	
Max. Gr/Gb ratio		<2%	
Max. frame rate	fps	15fps@full resolution 30fps@VGA	
Max. CRA	degree	23.4	+/- 1.5 (21.9 ~ 24.9)
ADC resolution	bit	10	

15 Register Description

15.1 REGISTER ADDRESS MAPPING



[NOTE] Most H/W registers are not accessible to users.

Addr	Reset Value	Mnemonic	Attr	Bits	Description
				[1] [0]	<p>I2c_clock_stretch_dis – When the bit is reset, clock stretching in the read cycle is enabled, and lasts as long as defined in the clk_str_delay_reg register.</p> <p>When this bit is set, it disables clock stretching on the read cycle in Slave I²C. It can be set only if the system guarantees an immediate response, from AHB request to AHB response (and readback data).</p> <p>I2C_msbfirst – Communicate with a data width of two bytes. The default is that the MSByte of the I²C transaction (address and data) is received on the interface. The byte order of the data transaction can be changed to LSByte-first by lowering the I2C_msbfirst register to zero.</p>
0x0002	0x00	Reset_I2C_mode	Read/Write	[7:1] [0]	<p>Reserved</p> <p>Reset_I2C_mode – Setting this register resets the I²C slave to MSB first and 16-bit address/data mode.</p>
0x0004	0x1	I2C_dis_addr_inc	Read/Write	[7:1] [0]	<p>Reserved</p> <p>I2C_dis_addr_inc – This bit must be set for every memory access, in order to prevent the auto increment of the I²C address.</p>
0x0006	0x19	I2c_clk_str_delay_cnt	Read/Write	[8:0]	<p>I2c_clk_str_delay_reg – This 9-bit register defines the duration of clock stretching delay in read cycle of the slave I²C (in terms of internal clock cycles). In other words, it represents the time between readback data set up on I²C data signal, SDIN, and the release point of the I²C clock signal, SCLK.</p> <p>It should be configured to ensure a minimum setup time of 250nsec between SDIN and SCLK signals, as required by I²C BUS SPECIFICATION version 2.1.</p> <p>Default value is 25 decimal, based on an internal clock cycle of 10nsec (to ensure set up time of 250nsec).</p>
0x0008	0xd000	I2c_ahb_msb_addr_ptr	Read/Write	[15:0]	<p>I2c_ahb_msb_addr_ptr - This register contains the 16-bit MSB of the 32-bit address in accessing the AHB bus.</p> <p>It can be accessed (read/write) in two different ways:</p> <ul style="list-style-type: none"> • Via a specifically reserved address - ahb_msb_addr_ptr that is configured to 0xfcf. • Approached as a general register that contains the APB peripherals start address (0xd000).



Addr	Reset Value	Mnemonic	Attr	Bits	Description
0x0010	0x0	sw_reset	Write-Only	[7:1] [0]	<p>Not used – must be zero.</p> <p>Sw_reset – When sw_reset is equal to zero, normal operation of the device is enabled. When the host sets this bit to one, the internal reset signal is activated for seven clk cycles. The device operation is stopped, all units are put into idle state and all registers are reset to their default state.</p> <p>On power-up, the ARM is automatically starts run. When need to halt the ARM (i.e. for FW update with Trap and Patch), then this bit should be used according to application notes.</p>
0x0012	0x1	sw_core_reset	Write-Only	[7:1] [0]	<p>Not used – must be zero.</p> <p>Sw_core_reset – When sw_core_reset is equal to zero, normal operation of the CONT core is enabled. When the host sets this bit to one, the internal reset signal to the CONT core is activated for seven clk cycles.</p>
0x0014	0x0	sw_load_complete	Write-Only	[7:1] [0]	<p>Not used – must be zero.</p> <p>Sw_load_complete – When the host finishes the loading process of the program memory, an access to this register, asserting the Sw_load_complete bit, disables the reset signal to the CONT.</p> <p>On power-up, the ARM is automatically starts run. When need to halt the ARM (i.e. for FW update with Trap and Patch), and then rerun the ARM, this bit should be used according to application notes.</p>
0x0020	0x0000	Mem_Wr_add H	Read/ Write	[15:0]	<p>Mem_wr_add[31:16] - This register defines the MSB start-address (Byte address) for indirect access to Memory. This register is part of 1st set of pointers.</p> <p>The CONT unit automatically increments the address after each memory access by the host.</p>
0x0022	0x0000	Mem_Wr_add L	Read/ Write	[15:0]	<p>Mem_wr_add[15:0] - This register defines the LSB start-address (Byte address) for indirect access to Memory. This register is part of 1st set of pointers.</p> <p>The CONT unit automatically increments the address after each memory access by the host.</p>
0x0024	0x0000	Mem_Rd_add H	Read/ Write	[15:0]	<p>Mem_rd_add[31:16] - This register defines the MSB start-address (Byte address) for the host indirect READ access to memory. This register is part of 1st set of pointers.</p> <p>The CONT unit increments the address after each memory access by the host.</p>

Addr	Reset Value	Mnemonic	Attr	Bits	Description
0x0026	0x0000	Mem_Rd_addL	Read/Write	[15:0]	Mem_rd_add[15:0] - This register defines the LSB start-address (Byte address) for the host indirect READ access to memory. This register is part of 1 st set of pointers. The CONT unit increments the address after each memory access by the host.
The second set of host access registers to main memory follows.					
0x0028	0x0000	Command_Wr_addH	Read/Write	[15:0]	Mem_wr_add[31:16] – Same as Mem_Wr_addH, but part of 2 nd set of pointers.
0x002A	0x0000	Command_Wr_addL	Read/Write	[15:0]	Mem_wr_add[15:0] - Same as Mem_Wr_addL, but part of 2 nd set of pointers.
0x002C	0x0000	Command_Rd_addH	Read/Write	[15:0]	Mem_rd_add[31:16] – Same as Mem_Rd_addH, but part of 2 nd set of pointers.
0x002E	0x0000	Command_Rd_addL	Read/Write	[15:0]	Mem_rd_add[15:0] - Same as Mem_Rd_addL, but part of 2 nd set of pointers.
0x0030	1 0	adr_tg_sw_stby_n	Read/Write	[7:3] [2] [1] [0]	Reserved reg_sw_stby_n – Disconnected for future use. atop_sw_stby_n – Software standby bit for ATOP block. tg_sw_stby_n – Software standby bit (Move clock system to SW-STBY mode). This wire does not connect to TG stand-by bit.
0x0032	0x00			[7:0]	Reserved
0x0034	0x00			[7:0]	Reserved
0x0036	0x00	adr_fw_wait	Read/Write	[7:1] [0]	Reserved Fw_wait – When writing '1' to this bit, the clock system enters the Firmware Wait state as defined in the power management table.



17 HOST SW REGISTER INTERFACE (0x7000000 – 0x70002000)

The software register interface is based on video streaming configurations that are defined prior to compilation. The interface requires the definition of at least one video preview configuration (or using one of the default configurations by using the register's default values). Each configuration depends on user requirements (frame rate, preview size, etc.) and system limitations (output rate limits, image format, etc.). Video streaming configurations must be defined with user requirements in mind in order to achieve optimal camera operation.

There are five optional preview configurations and five capture configurations that can be used throughout the sensor operation. At any time during the preview, the host may switch the sensor to work with another configuration (out of the set of five possible configurations). This is done by filling the required configuration with valid data and then applying the registers in the following order:

[Note] All addresses below should be applied with 0x70000000 offset (for example, instead of 0x01C0, use 0x700001C0 address).

Initialization Parameters	Address	Default	Attr	Description
REG_TC_IPRM_InClockLSBs	0x01C0	0x5DC0	R/W	Input clock in KHz (lower 16 bits)
REG_TC_IPRM_InClockMSBs	0x01C2	0x0000	R/W	Input clock in KHz (upper 16 bits)
REG_TC_IPRM_PllFreqDiv4	0x01C4	0x1770	R/W	Reserved
REG_TC_IPRM_AddHeader	0x01C6	0x0000	R/W	Reserved
REG_TC_IPRM_ValidVActiveLow	0x01C8	0x0000	R/W	Reserved
REG_TC_IPRM_SenI2CAAdr	0x01CA	0x0011	R/W	Reserved
REG_TC_IPRM_MI2CDrSciMan	0x01CC	0x0001	R/W	Reserved
REG_TC_IPRM_UseNPviClocks	0x01CE	0x0001	R/W	Number of PLL configurations to be computed (1-3)
REG_TC_IPRM_UseNMipiClocks	0x01D0	0x0000	R/W	Number of MIPI configurations to be computed (1-3)
REG_TC_IPRM_bBlockInternalPllCalc	0x01D2	0x0000	R/W	Use external PLL settings rather than internal FW calculation
REG_TC_IPRM_OpClk4KHz_0	0x01D4	0x1770	R/W	First system clock frequency in KHz divided by 4
REG_TC_IPRM_MinOutRate4KHz_0	0x01D6	0x05DC	R/W	Minimal output rate of first clock in KHz divided by 4
REG_TC_IPRM_MaxOutRate4KHz_0	0x01D8	0x1770	R/W	Maximal output rate of first clock in KHz divided by 4

Initialization Parameters	Address	Default	Attr	Description	
REG_TC_IPRM_OpClk4KHz_1	0x01DA	0x1770	R/W	Second system clock frequency in KHz divided by 4	
REG_TC_IPRM_MinOutRate4KHz_1	0x01DC	0x1770	R/W	Minimal output rate of second clock in KHz divided by 4	
REG_TC_IPRM_MaxOutRate4KHz_1	0x01DE	0x2328	R/W	Maximal output rate of second clock in KHz divided by 4	
REG_TC_IPRM_OpClk4KHz_2	0x01E0	0x0BB8	R/W	Third system clock frequency in KHz divided by 4	
REG_TC_IPRM_MinOutRate4KHz_2	0x01E2	0x05DC	R/W	Minimal output rate of third clock in KHz divided by 4	
REG_TC_IPRM_MaxOutRate4KHz_2	0x01E4	0x1770	R/W	Maximal output rate of third clock in KHz divided by 4	
REG_TC_IPRM_UseRegsAPI	0x01E6	0x0001	R/W	Reserved	
REG_TC_IPRM_InitParamsUpdated	0x01E8	0x0000	R/W	Update values in FW and invoke FW initialization	
REG_TC_IPRM_ErrorInfo	0x01EA	0x0000	R	Error code received from FW (0: no error)	

Preview Configurations	Address	Default	Attr	Description	Configuration Number
REG_0TC_PCFG_usWidth	0x024A	0x0500	R/W	Output width (Up to 1280 in increments of 2)	0
REG_0TC_PCFG_usHeight	0x024C	0x0400	R/W	Output height (Up to 1024 in increments of 2)	0
REG_0TC_PCFG_Format	0x024E	0x0005	R/W	Output format	0
REG_0TC_PCFG_usMaxOut4KHzRate	0x0250	0x1770	R/W	Maximal output rate in KHz divided by 4	0
REG_0TC_PCFG_usMinOut4KHzRate	0x0252	0x05DC	R/W	Minimal output rate in KHz divided by 4	0
REG_0TC_PCFG_PVIMask	0x0254	0x0042	R/W	PVI configuration flags	0
REG_0TC_PCFG_uClockInd	0x0256	0x0000	R/W	System clock index (1-3)	0
REG_0TC_PCFG_usFrTimeType	0x0258	0x0000	R/W	Frame rate type: fixed FR/dynamic FR	0

Preview Configurations	Address	Default	Attr	Description	Configuration Number
REG_0TC_PCFG_FrRateQualityType	0x025A	0x0000	R/W	Frame rate quality: high FR, high quality, dynamic	0
REG_0TC_PCFG_usMaxFrTimeMsecMult10	0x025C	0x1964	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (for example, 333 for 33.3 ms)	0
REG_0TC_PCFG_usMinFrTimeMsecMult10	0x025E	0x0000	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)	0
REG_0TC_PCFG_sSaturation	0x0260	0x0000	R/W	Device correction saturation control	0
REG_0TC_PCFG_sSharpBlur	0x0262	0x0000	R/W	Device correction sharpness control	0
REG_0TC_PCFG_sGlamour	0x0264	0x0000	R/W	Device correction glamour control	0
REG_0TC_PCFG_sColorTemp	0x0266	0x0000	R/W	Device correction color temperature control	0
REG_0TC_PCFG_uDeviceGammaIndex	0x0268	0x0000	R/W	Device correction Gamma table index	0
REG_0TC_PCFG_uPrevMirror	0x026A	0x0000	R/W	Preview mirror mode (X/Y) - Bit mask	0
REG_0TC_PCFG_uCaptureMirror	0x026C	0x0000	R/W	Capture mirror mode (X/Y) - Bit mask	0
REG_0TC_PCFG_uRotation	0x026E	0x0000	R/W	Reserved	0
REG_1TC_PCFG_usWidth	0x0270	0x0400	R/W	Output width (Up to 1280 in increments of 2)	1
REG_1TC_PCFG_usHeight	0x0272	0x0300	R/W	Output height (Up to 1024 in increments of 2)	1
REG_1TC_PCFG_Format	0x0274	0x0005	R/W	Output format	1
REG_1TC_PCFG_usMaxOut4KHzRate	0x0276	0x1770	R/W	Maximal output rate in KHz divided by 4	1
REG_1TC_PCFG_usMinOut4KHzRate	0x0278	0x05DC	R/W	Minimal output rate in KHz divided by 4	1

Preview Configurations	Address	Default	Attr	Description	Configuration Number
REG_1TC_PCFG_PVIMask	0x027A	0x0042	R/W	PVI configuration flags	1
REG_1TC_PCFG_uClockInd	0x027C	0x0000	R/W	System clock index (1-3)	1
REG_1TC_PCFG_usFrTimeType	0x027E	0x0000	R/W	Frame rate type: fixed FR/dynamic FR	1
REG_1TC_PCFG_FrRateQualityType	0x0280	0x0000	R/W	Frame rate quality: high FR, high quality, dynamic	1
REG_1TC_PCFG_usMaxFrTimeMsecMult10	0x0282	0x1964	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (for example, 333 for 33.3 ms)	1
REG_1TC_PCFG_usMinFrTimeMsecMult10	0x0284	0x0000	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)	1
REG_1TC_PCFG_sSaturation	0x0286	0x0000	R/W	Device correction saturation control	1
REG_1TC_PCFG_sSharpBlur	0x0288	0x0000	R/W	Device correction sharpness control	1
REG_1TC_PCFG_sGlamour	0x028A	0x0000	R/W	Device correction glamour control	1
REG_1TC_PCFG_sColorTemp	0x028C	0x0000	R/W	Device correction color temperature control	1
REG_1TC_PCFG_uDeviceGammaIndex	0x028E	0x0000	R/W	Device correction Gamma table index	1
REG_1TC_PCFG_uPrevMirror	0x0290	0x0000	R/W	Preview mirror mode (X/Y) - Bit mask	1
REG_1TC_PCFG_uCaptureMirror	0x0292	0x0000	R/W	Capture mirror mode (X/Y) - Bit mask	1
REG_1TC_PCFG_uRotation	0x0294	0x0000	R/W	Reserved	1
REG_2TC_PCFG_usWidth	0x0296	0x0320	R/W	Output width (Up to 1280 in steps of 2)	2
REG_2TC_PCFG_usHeight	0x0298	0x0258	R/W	Output height (Up to 1024 in steps of 2)	2
REG_2TC_PCFG_Format	0x029A	0x0005	R/W	Output format	2

Preview Configurations	Address	Default	Attr	Description	Configuration Number
REG_2TC_PCFG_usMaxOut4KHzRate	0x029C	0x1770	R/W	Maximal output rate in KHz divided by 4	2
REG_2TC_PCFG_usMinOut4KHzRate	0x029E	0x05DC	R/W	Minimal output rate in KHz divided by 4	2
REG_2TC_PCFG_PVIMask	0x02A0	0x0042	R/W	PVI configuration flags	2
REG_2TC_PCFG_uClockInd	0x02A2	0x0000	R/W	System clock index (1-3)	2
REG_2TC_PCFG_usFrTimeType	0x02A4	0x0000	R/W	Frame rate type: fixed FR/dynamic FR	2
REG_2TC_PCFG_FrRateQualityType	0x02A6	0x0000	R/W	Frame rate quality: high FR, high quality, dynamic	2
REG_2TC_PCFG_usMaxFrTimeMsecMult10	0x02A8	0x1964	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (for example, 333 for 33.3 ms)	2
REG_2TC_PCFG_usMinFrTimeMsecMult10	0x02AA	0x0000	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)	2
REG_2TC_PCFG_sSaturation	0x02AC	0x0000	R/W	Device correction saturation control	2
REG_2TC_PCFG_sSharpBlur	0x02AE	0x0000	R/W	Device correction sharpness control	2
REG_2TC_PCFG_sGlamour	0x02B0	0x0000	R/W	Device correction glamour control	2
REG_2TC_PCFG_sColorTemp	0x02B2	0x0000	R/W	Device correction color temperature control	2
REG_2TC_PCFG_uDeviceGammaIndex	0x02B4	0x0000	R/W	Device correction Gamma table index	2
REG_2TC_PCFG_uPrevMirror	0x02B6	0x0000	R/W	Preview mirror mode (X/Y) - Bit mask	2
REG_2TC_PCFG_uCaptureMirror	0x02B8	0x0000	R/W	Capture mirror mode (X/Y) - Bit mask	2
REG_2TC_PCFG_uRotation	0x02BA	0x0000	R/W	Reserved	2

Preview Configurations	Address	Default	Attr	Description	Configuration Number
REG_3TC_PCFG_usWidth	0x02BC	0x0280	R/W	Output width (Up to 1280 in increments of 2)	3
REG_3TC_PCFG_usHeight	0x02BE	0x01E0	R/W	Output height (Up to 1024 in increments of 2)	3
REG_3TC_PCFG_Format	0x02C0	0x0005	R/W	Output format	3
REG_3TC_PCFG_usMaxOut4K HzRate	0x02C2	0x1770	R/W	Maximal output rate in KHz divided by 4	3
REG_3TC_PCFG_usMinOut4K HzRate	0x02C4	0x05DC	R/W	Minimal output rate in KHz divided by 4	3
REG_3TC_PCFG_PVIMask	0x02C6	0x0042	R/W	PVI configuration flags	3
REG_3TC_PCFG_uClockInd	0x02C8	0x0000	R/W	System clock index (1-3)	3
REG_3TC_PCFG_usFrTimeType	0x02CA	0x0000	R/W	Frame rate type: fixed FR/dynamic FR	3
REG_3TC_PCFG_FrRateQualityType	0x02CC	0x0000	R/W	Frame rate quality: high FR, high quality, dynamic	3
REG_3TC_PCFG_usMaxFrTimeMsecMult10	0x02CE	0x1964	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (for example, 333 for 33.3 ms)	3
REG_3TC_PCFG_usMinFrTimeMsecMult10	0x02D0	0x0000	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)	3
REG_3TC_PCFG_sSaturation	0x02D2	0x0000	R/W	Device correction saturation control	3
REG_3TC_PCFG_sSharpBlur	0x02D4	0x0000	R/W	Device correction sharpness control	3
REG_3TC_PCFG_sGlamour	0x02D6	0x0000	R/W	Device correction glamour control	3
REG_3TC_PCFG_sColorTemp	0x02D8	0x0000	R/W	Device correction color temperature control	3
REG_3TC_PCFG_uDeviceGammaIndex	0x02DA	0x0000	R/W	Device correction Gamma table index	3



Preview Configurations	Address	Default	Attr	Description	Configuration Number
REG_3TC_PCFG_uPrevMirror	0x02DC	0x0000	R/W	Preview mirror mode (X/Y) - Bit mask	3
REG_3TC_PCFG_uCaptureMirror	0x02DE	0x0000	R/W	Capture mirror mode (X/Y) - Bit mask	3
REG_3TC_PCFG_uRotation	0x02E0	0x0000	R/W	Reserved	3
REG_4TC_PCFG_usWidth	0x02E2	0x0140	R/W	Output width (Up to 1280 in increments of 2)	4
REG_4TC_PCFG_usHeight	0x02E4	0x00F0	R/W	Output height (Up to 1024 in increments of 2)	4
REG_4TC_PCFG_Format	0x02E6	0x0005	R/W	Output format	4
REG_4TC_PCFG_usMaxOut4KHzRate	0x02E8	0x1770	R/W	Maximal output rate in KHz divided by 4	4
REG_4TC_PCFG_usMinOut4KHzRate	0x02EA	0x05DC	R/W	Minimal output rate in KHz divided by 4	4
REG_4TC_PCFG_PVIMask	0x02EC	0x0042	R/W	PVI configuration flags	4
REG_4TC_PCFG_uClockInd	0x02EE	0x0000	R/W	System clock index (1-3)	4
REG_4TC_PCFG_usFrTimeType	0x02F0	0x0000	R/W	Frame rate type: fixed FR/dynamic FR	4
REG_4TC_PCFG_FrRateQualityType	0x02F2	0x0000	R/W	Frame rate quality: high FR, high quality, dynamic	4
REG_4TC_PCFG_usMaxFrTimeMsecMult10	0x02F4	0x1964	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (for example, 333 for 33.3 ms)	4
REG_4TC_PCFG_usMinFrTimeMsecMult10	0x02F6	0x0000	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)	4
REG_4TC_PCFG_sSaturation	0x02F8	0x0000	R/W	Device correction saturation control	4
REG_4TC_PCFG_sSharpBlur	0x02FA	0x0000	R/W	Device correction sharpness control	4

Preview Configurations	Address	Default	Attr	Description	Configuration Number
REG_4TC_PCFG_sGlamour	0x02FC	0x0000	R/W	Device correction glamour control	4
REG_4TC_PCFG_sColorTemp	0x02FE	0x0000	R/W	Device correction color temperature control	4
REG_4TC_PCFG_uDeviceGammaIndex	0x0300	0x0000	R/W	Device correction Gamma table index	4
REG_4TC_PCFG_uPrevMirror	0x0302	0x0000	R/W	Preview mirror mode (X/Y) - Bit mask	4
REG_4TC_PCFG_uCaptureMirror	0x0304	0x0000	R/W	Capture mirror mode (X/Y) - Bit mask	4
REG_4TC_PCFG_uRotation	0x0306	0x0000	R	Reserved	4
REG_AC_TC_PCFG_usWidth	0x12AC	0x0000	R	Output width (Up to 1280 in increments of 2)	Actual
REG_AC_TC_PCFG_usHeight	0x12AE	0x0000	R	Output height (Up to 1024 in increments of 2)	Actual
REG_AC_TC_PCFG_Format	0x12B0	0x0000	R	Output format	Actual
REG_AC_TC_PCFG_usMaxOutput4KHzRate	0x12B2	0x0000	R	Maximal output rate in KHz divided by 4	Actual
REG_AC_TC_PCFG_usMinOutput4KHzRate	0x12B4	0x0000	R	Minimal output rate in KHz divided by 4	Actual
REG_AC_TC_PCFG_PVIMask	0x12B6	0x0000	R	PVI configuration flags	Actual
REG_AC_TC_PCFG_uClockIndex	0x12B8	0x0000	R	System clock index (1-3)	Actual
REG_AC_TC_PCFG_usFrameRateType	0x12BA	0x0000	R	Frame rate type: fixed FR/dynamic FR	Actual
REG_AC_TC_PCFG_FrameRateQualityType	0x12BC	0x0000	R	Frame rate quality: high FR, high quality, dynamic	Actual
REG_AC_TC_PCFG_usMaxFrameTimeMsecMult10	0x12BE	0x0000	R	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (for example, 333 for 33.3 ms)	Actual

Preview Configurations	Address	Default	Attr	Description	Configuration Number
REG_AC_TC_PCFG_usMinFrTimeMsecMult10	0x12C0	0x0000	R	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)	Actual
REG_AC_TC_PCFG_sSaturation	0x12C2	0x0000	R	Device correction saturation control	Actual
REG_AC_TC_PCFG_sSharpBlur	0x12C4	0x0000	R	Device correction sharpness control	Actual
REG_AC_TC_PCFG_sGlamour	0x12C6	0x0000	R	Device correction glamour control	Actual
REG_AC_TC_PCFG_sColorTemp	0x12C8	0x0000	R	Device correction color temperature control	Actual
REG_AC_TC_PCFG_uDeviceGammaIndex	0x12CA	0x0000	R	Device correction Gamma table index	Actual
REG_AC_TC_PCFG_uPrevMirror	0x12CC	0x0000	R	Preview mirror mode (X/Y) - Bit mask	Actual
REG_AC_TC_PCFG_uCaptureMirror	0x12CE	0x0000	R	Capture mirror mode (X/Y) - Bit mask	Actual
REG_AC_TC_PCFG_uRotation	0x12D0	0x0000		Reserved	Actual

Capture Configurations	Address	Default	Attr	Description	Configuration Number
REG_0TC_CCFG_uCaptureMode	0x0314	0x0000	R/W	Capture type: single, multishot, etc.	0
REG_0TC_CCFG_usWidth	0x0316	0x0500	R/W	Capture width (Up to 1280 in increments of 2)	0
REG_0TC_CCFG_usHeight	0x0318	0x0400	R/W	Capture height (Up to 1024 in increments of 2)	0
REG_0TC_CCFG_Format	0x031A	0x0009	R/W	Capture format	0
REG_0TC_CCFG_usMaxOut4KHzRate	0x031C	0x1770	R/W	Maximal output rate in KHz divided by 4	0
REG_0TC_CCFG_usMinOut4KHzRate	0x031E	0x05DC	R/W	Minimal output rate in KHz divided by 4	0
REG_0TC_CCFG_PVIMask	0x0320	0x0042	R/W	PVI configuration flags	0
REG_0TC_CCFG_uClockInd	0x0322	0x0000	R/W	System clock index (1-3)	0

Capture Configurations	Address	Default	Attr	Description	Configuration Number
REG_0TC_CCFG_usFrTimeType	0x0324	0x0000		Frame rate type: fixed FR/dynamic FR	0
REG_0TC_CCFG_FrRateQualityType	0x0326	0x0002	R/W	Frame rate quality: high FR, high quality, dynamic	0
REG_0TC_CCFG_usMaxFrTimeMsecMult10	0x0328	0x1964	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (for example, 333 for 33.3 ms)	0
REG_0TC_CCFG_usMinFrTimeMsecMult10	0x032A	0x0000	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)	0
REG_0TC_CCFG_sSaturation	0x032C	0x0000	R/W	Device correction saturation control	0
REG_0TC_CCFG_sSharpBlur	0x032E	0x0000		Device correction sharpness control	0
REG_0TC_CCFG_sGlamour	0x0330	0x0000	R/W	Device correction glamour control	0
REG_0TC_CCFG_sColorTemp	0x0332	0x0000	R/W	Device correction color temperature control	0
REG_0TC_CCFG_uDeviceGammaIndex	0x0334	0x0000	R/W	Device correction Gamma table index	0
REG_1TC_CCFG_uCaptureMode	0x0336	0x0000	R/W		1
REG_1TC_CCFG_usWidth	0x0338	0x0500	R/W	Capture width (Up to 1280 in increments of 2)	1
REG_1TC_CCFG_usHeight	0x033A	0x03C0	R/W	Capture height (Up to 1024 in increments of 2)	1
REG_1TC_CCFG_Format	0x033C	0x0009	R/W	Capture format	1
REG_1TC_CCFG_usMaxOut4KHzRate	0x033E	0x1770	R/W	Maximal output rate in KHz divided by 4	1
REG_1TC_CCFG_usMinOut4KHzRate	0x0340	0x05DC	R/W	Minimal output rate in KHz divided by 4	1
REG_1TC_CCFG_PVIMask	0x0342	0x0042	R/W	PVI configuration flags	1



Capture Configurations	Address	Default	Attr	Description	Configuration Number
REG_1TC_CCFG_uClockInd	0x0344	0x0000	R/W	System clock index (1-3)	1
REG_1TC_CCFG_usFrTimeType	0x0346	0x0000	R/W	Frame rate type: fixed FR/dynamic FR	1
REG_1TC_CCFG_FrRateQualityType	0x0348	0x0002	R/W	Frame rate quality: high FR, high quality, dynamic	1
REG_1TC_CCFG_usMaxFrTimeMsecMult10	0x034A	0x1964	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (for example, 333 for 33.3 ms)	1
REG_1TC_CCFG_usMinFrTimeMsecMult10	0x034C	0x0000	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)	1
REG_1TC_CCFG_sSaturation	0x034E	0x0000	R/W	Device correction saturation control	1
REG_1TC_CCFG_sSharpBlur	0x0350	0x0000	R/W	Device correction sharpness control	1
REG_1TC_CCFG_sGlamour	0x0352	0x0000	R/W	Device correction glamour control	1
REG_1TC_CCFG_sColorTemp	0x0354	0x0000	R/W	Device correction color temperature control	1
REG_1TC_CCFG_uDeviceGammaIndex	0x0356	0x0000	R/W	Device correction Gamma table index	1
REG_2TC_CCFG_uCaptureMode	0x0358	0x0000	R/W	Capture type: single, multishot, etc.	2
REG_2TC_CCFG_usWidth	0x035A	0x0320	R/W	Capture width (Up to 1280 in increments of 2)	2
REG_2TC_CCFG_usHeight	0x035C	0x0258	R/W	Capture height (Up to 1024 in increments of 2)	2
REG_2TC_CCFG_Format	0x035E	0x0009	R/W	Capture format	2
REG_2TC_CCFG_usMaxOut4KHzRate	0x0360	0x1770	R/W	Maximal output rate in KHz divided by 4	2

Capture Configurations	Address	Default	Attr	Description	Configuration Number
REG_2TC_CCFG_usMinOut4KHzRate	0x0362	0x05DC	R/W	Minimal output rate in KHz divided by 4	2
REG_2TC_CCFG_PVIMask	0x0364	0x0042	R/W	PVI configuration flags	2
REG_2TC_CCFG_uClockInd	0x0366	0x0000	R/W	System clock index (1-3)	2
REG_2TC_CCFG_usFrTimeType	0x0368	0x0000	R/W	Frame rate type: fixed FR/dynamic FR	2
REG_2TC_CCFG_FrRateQualityType	0x036A	0x0002	R/W	Frame rate quality: high FR, high quality, dynamic	2
REG_2TC_CCFG_usMaxFrTimeMsecMult10	0x036C	0x1964	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (for example, 333 for 33.3 ms)	2
REG_2TC_CCFG_usMinFrTimeMsecMult10	0x036E	0x0000	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)	2
REG_2TC_CCFG_sSaturation	0x0370	0x0000	R/W	Device correction saturation control	2
REG_2TC_CCFG_sSharpBlur	0x0372	0x0000	R/W	Device correction sharpness control	2
REG_2TC_CCFG_sGlamour	0x0374	0x0000	R/W	Device correction glamour control	2
REG_2TC_CCFG_sColorTemp	0x0376	0x0000	R/W	Device correction color temperature control	2
REG_2TC_CCFG_uDeviceGammaIndex	0x0378	0x0000	R/W	Device correction Gamma table index	2
REG_3TC_CCFG_uCaptureMode	0x037A	0x0000	R/W	Capture type: single, multishot, etc.	3
REG_3TC_CCFG_usWidth	0x037C	0x0280	R/W	Capture width (Up to 1280 in increments of 2)	3
REG_3TC_CCFG_usHeight	0x037E	0x01E0	R/W	Capture height (Up to 1024 in increments of 2)	3
REG_3TC_CCFG_Format	0x0380	0x0009	R/W	Capture format	3



Capture Configurations	Address	Default	Attr	Description	Configuration Number
REG_3TC_CCFG_usMaxOut4KHzRate	0x0382	0x1770	R/W	Maximal output rate in KHz divided by 4	3
REG_3TC_CCFG_usMinOut4KHzRate	0x0384	0x05DC	R/W	Minimal output rate in KHz divided by 4	3
REG_3TC_CCFG_PVIMask	0x0386	0x0042	R/W	PVI configuration flags	3
REG_3TC_CCFG_uClockInd	0x0388	0x0000	R/W	System clock index (1-3)	3
REG_3TC_CCFG_usFrTimeType	0x038A	0x0000	R/W	Frame rate type: fixed FR/dynamic FR	3
REG_3TC_CCFG_FrRateQualityType	0x038C	0x0002	R/W	Frame rate quality: high FR, high quality, dynamic	3
REG_3TC_CCFG_usMaxFrTimeMsecMult10	0x038E	0x1964	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (for example, 333 for 33.3 ms)	3
REG_3TC_CCFG_usMinFrTimeMsecMult10	0x0390	0x0000	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)	3
REG_3TC_CCFG_sSaturation	0x0392	0x0000	R/W	Device correction saturation control	3
REG_3TC_CCFG_sSharpBlur	0x0394	0x0000	R/W	Device correction sharpness control	3
REG_3TC_CCFG_sGlamour	0x0396	0x0000	R/W	Device correction glamour control	3
REG_3TC_CCFG_sColorTemp	0x0398	0x0000	R/W	Device correction color temperature control	3
REG_3TC_CCFG_uDeviceGammaIndex	0x039A	0x0000	R/W	Device correction Gamma table index	3
REG_4TC_CCFG_uCaptureMode	0x039C	0x0000	R/W	Capture type: single, multishot, etc.	4
REG_4TC_CCFG_usWidth	0x039E	0x0140	R/W	Capture width (Up to 1280 in increments of 2)	4

Capture Configurations	Address	Default	Attr	Description	Configuration Number
REG_4TC_CCFG_usHeight	0x03A0	0x00F0	R/W	Capture height (Up to 1024 in increments of 2)	4
REG_4TC_CCFG_Format	0x03A2	0x0009	R/W	Capture format	4
REG_4TC_CCFG_usMaxOut4K HzRate	0x03A4	0x1770	R/W	Maximal output rate in KHz divided by 4	4
REG_4TC_CCFG_usMinOut4K HzRate	0x03A6	0x05DC	R/W	Minimal output rate in KHz divided by 4	4
REG_4TC_CCFG_PVIMask	0x03A8	0x0042	R/W	PVI configuration flags	4
REG_4TC_CCFG_uClockInd	0x03AA	0x0000	R/W	System clock index (1-3)	4
REG_4TC_CCFG_usFrTimeType	0x03AC	0x0000	R/W	Frame rate type: fixed FR/dynamic FR	4
REG_4TC_CCFG_FrRateQualityType	0x03AE	0x0002	R/W	Frame rate quality: high FR, high quality, dynamic	4
REG_4TC_CCFG_usMaxFrTimeMsecMult10	0x03B0	0x1964	R/W	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (for example, 333 for 33.3 ms)	4
REG_4TC_CCFG_usMinFrTimeMsecMult10	0x03B2	0x0000	R/W	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)	4
REG_4TC_CCFG_sSaturation	0x03B4	0x0000	R/W	Device correction saturation control	4
REG_4TC_CCFG_sSharpBlur	0x03B6	0x0000	R/W	Device correction sharpness control	4
REG_4TC_CCFG_sGlamour	0x03B8	0x0000	R/W	Device correction glamour control	4
REG_4TC_CCFG_sColorTemp	0x03BA	0x0000	R/W	Device correction color temperature control	4
REG_4TC_CCFG_uDeviceGammaIndex	0x03BC	0x0000	R/W	Device correction Gamma table index	4
REG_AC_TC_CCFG_uCapture Mode	0x12F8	0x0000	R	Capture type: single, multishot, etc.	Actual



Capture Configurations	Address	Default	Attr	Description	Configuration Number
REG_AC_TC_CCFG_usWidth	0x12FA	0x0000	R	Capture width (Up to 1280 in increments of 2)	Actual
REG_AC_TC_CCFG_usHeight	0x12FC	0x0000	R	Capture height (Up to 1024 in increments of 2)	Actual
REG_AC_TC_CCFG_Format	0x12FE	0x0000	R	Capture format	Actual
REG_AC_TC_CCFG_usMaxOut4KHzRate	0x1300	0x0000	R	Maximal output rate in KHz divided by 4	Actual
REG_AC_TC_CCFG_usMinOut4KHzRate	0x1302	0x0000	R	Minimal output rate in KHz divided by 4	Actual
REG_AC_TC_CCFG_PVIMask	0x1304	0x0000	R	PVI configuration flags	Actual
REG_AC_TC_CCFG_uClockInd	0x1306	0x0000	R	System clock index (1-3)	Actual
REG_AC_TC_CCFG_usFrTimeType	0x1308	0x0000	R	Frame rate type: fixed FR/dynamic FR	Actual
REG_AC_TC_CCFG_FrRateQualityType	0x130A	0x0000	R	Frame rate quality: high FR, high quality, dynamic	Actual
REG_AC_TC_CCFG_usMaxFrTimeMsecMult10	0x130C	0x0000	R	Required frame time for fixed FR / maximal frame time for dynamic FR [333 – 6500] (Units are in 0.1 ms) (for example, 333 for 33.3 ms)	Actual
REG_AC_TC_CCFG_usMinFrTimeMsecMult10	0x130E	0x0000	R	Minimal frame time for dynamic FR. Not valid for fixed FR [333 – 6500] (Units are in 0.1 ms)	Actual
REG_AC_TC_CCFG_sSaturation	0x1310	0x0000	R	Device correction saturation control	Actual
REG_AC_TC_CCFG_sSharpBlur	0x1312	0x0000	R	Device correction sharpness control	Actual
REG_AC_TC_CCFG_sGlamour	0x1314	0x0000	R	Device correction glamour control	Actual
REG_AC_TC_CCFG_sColorTemp	0x1316	0x0000	R	Device correction color temperature control	Actual
REG_AC_TC_CCFG_uDeviceGammaIndex	0x1318	0x0000	R	Device correction Gamma table index	Actual

General Purpose Parameters	Address	Default	Attr	Description	
REG_TC_GP_SpecialEffects	0x01F6	0x0000	R/W	Special effects selection	
REG_TC_GP_EnablePreview	0x01F8	0x0000	R/W	Enable/disable preview output	
REG_TC_GP_EnablePreviewChanged	0x01FA	0x0000	R/W	Synchronize FW with Enable preview request	
REG_TC_GP_EnableCapture	0x01FC	0x0000	R/W	Invoke capture request	
REG_TC_GP_EnableCaptureChanged	0x01FE	0x0000	R/W	Synchronize FW with capture request	
REG_TC_GP_NewConfigSync	0x0200	0x0000	R/W	Set this flag when sending a new configuration. The FW clears the flag once a configuration has been applied.	
REG_TC_GP_PrevReqInputWidth	0x0202	0x0500	R/W	Preview input window width: Equal or greater than output width and up to 1280	
REG_TC_GP_PrevReqInputHeight	0x0204	0x0400	R/W	Preview window height: Equal or greater than output height and up to 1024	
REG_TC_GP_PrevInputWidthOfs	0x0206	0x0000	R/W	Preview input window X offset	
REG_TC_GP_PrevInputHeightOfs	0x0208	0x0000	R/W	Preview input window Y offset	
REG_TC_GP_CapReqInputWidth	0x020A	0x0500	R/W	Capture input window width: Equal or greater than output width and up to 1280	
REG_TC_GP_CapReqInputHeight	0x020C	0x0400	R/W	Capture window height: Equal or greater than output height and up to 1024	
REG_TC_GP_CapInputWidthOfs	0x020E	0x0000	R/W	Capture input window X offset	
REG_TC_GP_CapInputHeightOfs	0x0210	0x0000	R/W	Capture input window Y offset	

General Purpose Parameters	Address	Default	Attr	Description	
REG_TC_GP_PrevZoomReqInputWidth	0x0212	0x0500	R/W	Preview zoom window width: Equal or greater than output width and up to 1280	
REG_TC_GP_PrevZoomReqInputHeight	0x0214	0x0400	R/W	Preview zoom window height: Equal or greater than output height and up to 1024	
REG_TC_GP_PrevZoomReqInputWidthOfs	0x0216	0x0000	R/W	Preview zoom window X offset	
REG_TC_GP_PrevZoomReqInputHeightOfs	0x0218	0x0000	R/W	Preview zoom window Y offset	
REG_TC_GP_CapZoomReqInputWidth	0x021A	0x0500	R/W	Capture zoom window width: Equal or greater than output width and up to 1280	
REG_TC_GP_CapZoomReqInputHeight	0x021C	0x0400	R/W	Capture zoom window height: Equal or greater than output height and up to 1024	
REG_TC_GP_CapZoomReqInputWidthOfs	0x021E	0x0000	R/W	Capture zoom window X offset	
REG_TC_GP_CapZoomReqInputHeightOfs	0x0220	0x0000	R/W	Capture zoom window Y offset	
REG_TC_GP_InputsChangeRequest	0x0222	0x0000	R/W	Synchronize FW with input values	
REG_TC_GP_ActivePrevConfig	0x0224	0x0000	R/W	Index number of active preview configuration	
REG_TC_GP_PrevConfigChanged	0x0226	0x0000	R/W	Synchronize FW with new preview configuration	
REG_TC_GP_PrevOpenAfterChange	0x0228	0x0001	R/W	A flag that signals if, after the configuration change, the output should be enabled or not	
REG_TC_GP_ErrorPrevConfig	0x022A	0x0000	R	Error code received from FW for preview calculation (0: no error)	
REG_TC_GP_ActiveCapConfig	0x022C	0x0000	R/W	Index number of active capture configuration	

General Purpose Parameters	Address	Default	Attr	Description	
REG_TC_GP_CapConfigChanged	0x022E	0x0000	R/W	Synchronize FW with new capture configuration	
REG_TC_GP_ErrorCapConfig	0x0230	0x0000	R	Error code received from FW for capture calculation (0: no error)	
REG_TC_GP_PrevConfigBypassChanged	0x0232	0x0000	R/W	Synchronize FW with preview configuration bypass/usage request	
REG_TC_GP_CapConfigBypassChanged	0x0234	0x0000	R/W	Synchronize FW with capture configuration bypass/usage request	
REG_TC_GP_SleepMode	0x0236	0x0000	R/W	Set sleep mode (1: sleep, 0: wake-up)	
REG_TC_GP_SleepModeChanged	0x0238	0x0000	R/W	Synchronize FW with sleep mode change	
REG_TC_GP_SRA_AddLow	0x023A	0x0000	R/W	Reserved	
REG_TC_GP_SRA_AddHigh	0x023C	0x0000	R/W	Reserved	
REG_TC_GP_SRA_AccessType	0x023E	0x0000	R/W	Reserved	
REG_TC_GP_SRA_Changed	0x0240	0x0000	R/W	Reserved	
REG_TC_GP_PrevMinFrTimeMsecMult10	0x0242	0x0000	R	Get actual maximal preview frame rate in 0.1 mSec units	
REG_TC_GP_PrevOutKHzRate	0x0244	0x0000	R	Get actual preview output rate in KHz	
REG_TC_GP_CapMinFrTimeMsecMult10	0x0246	0x0000	R	Get actual maximal capture frame rate in 0.1 mSec units	
REG_TC_GP_CapOutKHzRate	0x0248	0x0000	R	Get actual capture output rate in KHz	

Image Property Controls	Address	Default	Attr	Description	
REG_TC_UserBrightness	0x01EC	0x0000	R/W	Control brightness value	
REG_TC_UserContrast	0x01EE	0x0000	R/W	Control contrast value	
REG_TC_UserSaturation	0x01F0	0x0000	R/W	Control saturation value	
REG_TC_UserSharpBlur	0x01F2	0x0000	R/W	Control sharpness value	
REG_TC_UserGlamour	0x01F4	0x0000	R/W	Control glamour value	

Flash Controls	Address	Default	Attr	Description	
REG_TC_FLS_Mode	0x03BE	0x0000	R/W	Set flash mode: 0: TC_FLASH_DISABLE, 1: TC_FLASH_CONT_E NABLE, // Always on 2: TC_FLASH_PULSE_E NABLE, // Use burst pulse on every capture 3: TC_FLASH_PULSE_A UTO // Sensor controls the Flash status (burst mode)	
REG_TC_FLS_Threshold	0x03C0	0x0050	R/W	Set flash activation threshold in normalized brightness units	
REG_TC_FLS_Polarity	0x03C2	0x0001	R/W	Set flash device polarity. 1: active high, 0: active low	
REG_TC_FLS_XenonMode	0x03C4	0x0000	R/W	Set Xenon flash mode: 0: TC_XENON_ DISABLE, 1: TC_XENON_ONE_ST ROBE, // Use one strobe 2: TC_XENON_PRE_FL ASH // Use n strobes for pre-flash and another one, full	
REG_TC_FLS_XenonPreFlash Cnt	0x03C6	0x0001	R/W	Number of Xenon pre-flash strobes	

Extended Image Property Controls	Address	Default	Attr	Description	
REG_SF_USER_LeiLow	0x03C8	0x0000	R/W	Set LEI low limit	
REG_SF_USER_LeiHigh	0x03CA	0x0000	R/W	Set LEI high limit	
REG_SF_USER_LeiChanged	0x03CC	0x0000	R/W	Synchronize FW with LEI limits change	
REG_SF_USER_Exposure	0x03CE	0x0000	R/W	Set manual exposure value	
REG_SF_USER_ExposureCha nged	0x03D2	0x0000	R/W	Synchronize FW with exposure settings change	
REG_SF_USER_TotalGain	0x03D4	0x0000	R/W	Set total gain value	

Extended Image Property Controls	Address	Default	Attr	Description	
REG_SF_USER_TotalGainChanged	0x03D6	0x0000	R/W	Synchronize FW with total gain change	
REG_SF_USER_Rgain	0x03D8	0x0000	R/W	Set red gain value	
REG_SF_USER_RgainChanged	0x03DA	0x0000	R/W	Synchronize FW with red gain change	
REG_SF_USER_Ggain	0x03DC	0x0000	R/W	Set green gain value	
REG_SF_USER_GgainChanged	0x03DE	0x0000	R/W	Synchronize FW with green gain change	
REG_SF_USER_Bgain	0x03E0	0x0000	R/W	Set blue gain value	
REG_SF_USER_BgainChanged	0x03E2	0x0000	R/W	Synchronize FW with blue gain change	
REG_SF_USER_FlickerQuant	0x03E4	0x0000	R/W	Set flicker quantization: 0: no AFC, 1: 50 Hz, 2: 60 Hz	
REG_SF_USER_FlickerQuantChanged	0x03E6	0x0000	R/W	Synchronize FW with flicker quantization change	
REG_SF_USER_GASRAAlphaVal	0x03E8	0x0000	R/W	Set grid anti-shading red alpha coefficient	
REG_SF_USER_GASRAAlphaChanged	0x03EA	0x0000	R/W	Synchronize FW with GAS red Alpha change	
REG_SF_USER_GASGAlphaVal	0x03EC	0x0000	R/W	Set grid anti-shading green alpha coefficient	
REG_SF_USER_GASGAlphaChanged	0x03EE	0x0000	R/W	Synchronize FW with GAS green Alpha change	
REG_SF_USER_GASBAlphaVal	0x03F0	0x0000	R/W	Set grid anti-shading blue alpha coefficient	
REG_SF_USER_GASBAlphaChanged	0x03F2	0x0000	R/W	Synchronize FW with GAS blue Alpha change	
REG_SF_USER_DbgIdx	0x03F4	0x0000	R/W	Reserved	
REG_SF_USER_DbgVal	0x03F6	0x0000	R/W	Reserved	
REG_SF_USER_DbgChanged	0x03F8	0x0000	R/W	Reserved	
REG_SF_USER_aGain	0x03FA	0x0000	R/W	Set analog gain value	
REG_SF_USER_aGainChanged	0x03FC	0x0000	R/W	Synchronize FW with analog gain change	
REG_SF_USER_dGain	0x03FE	0x0000	R/W	Set digital gain value	

Extended Image Property Controls	Address	Default	Attr	Description
REG_SF_USER_dGainChange	0x0400	0x0000	R/W	Synchronize FW with digital gain change

Output Interface Controls	Address	Default	Attr	Description
REG_TC_OIF_EnMipiLanes	0x0402	0x0000	R/W	Number of MIPI lanes (0: PVI, 1: 1 lane MIPI, 2: 2 lane MIPI)
REG_TC_OIF_EnPackets	0x0404	0x0000	R/W	MIPI configuration bit mask
REG_TC_OIF_CfgChanged	0x0406	0x0000	R/W	Synchronize FW with output interface configuration change

Debug Controls	Address	Default	Attr	Description
REG_TC_DBG_AutoAlgEnBits	0x0408	0x007F	R/W	Auto-algorithms enable/disable: SF_AA_ALL = 0, SF_AA_AE_ACTIVE = 1, SF_AA_DIV_LEI = 2, SF_AA_WB_ACTIVE = 3, SF_AA_USE_WB_FOR_ISP = 4, SF_AA_FLICKER = 5, SF_AA_FIT = 6, SF_AA_WR_HW = 7
REG_TC_DBG_IspBypass	0x040A	0x0000	R/W	Bypass FW operation
REG_TC_DBG_ReInitCmd	0x040C	0x0000	R/W	Invoke FW "soft reset"

Version Information	Address	Default	Attr	Description
REG_FWdate	0x0134	0xC71E	R	FW Date
REG_FWapiVer	0x0136	0x0001	R	FW API version
REG_FWrevision	0x0138	0x0107	R	FW revision
REG_FWpid	0x013A	0x0000	R	FW project ID
REG_FWprjName	0x013C	0x734F	R	FW project Name (Null termination string)

Version Information	Address	Default	Attr	Description	
REG_FWcompDate	0x0148	0x6544	R	FW compilation date (Null termination string)	
REG_FWSFC_VER	0x0154	0x0416	R	FW SDK Version	
REG_FWTC_VER	0x0156	0x0200	R	FW TC Version	
REG_FWrealImageLine	0x0158	0x0500	R	FW supported image line	
REG_FWsenId	0x015A	0x06AA	R	FW sensor ID support	
REG_FWusDevIdQaVersion	0x015C	0x0320	R	FW Developer ID + QA Version	
REG_FWusFwCompilationBits	0x015E	0x4020	R	FW Compilation bits (the features it supports)	
REG_ulSVNrevision	0x0160	0x71D6	R	FW version control revision (If zero, it is not aligned)	
REG_SVNpathRomAddress	0x0164		R	FW version control path ROM pointer	
REG_TRAP_N_PATCH_START_ADD	0x1B00			Trap & Patch start address	

IMPORTANT NOTICE

The information furnished by Samsung Electronics in this document is believed to be accurate and reliable. However, no responsibility is assumed by Samsung Electronics for its use, nor for any infringements of patents or other rights of third parties resulting from its use. No license is granted under any patents or patent rights of Samsung Electronics. Samsung Electronics reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current and complete.

For More Information

E-mail: yoel.yaffe@samsung.com

<http://www.samsung.com/Products/Semiconductor/index.htm>

Copyright © 2006-2009 Samsung Electronics, Inc. All Rights Reserved