

datasheet

PRELIMINARY SPECIFICATION

1/3.2" CMOS QSXGA (5 Megapixel) CameraChip™ sensor
with OmniPixel3-HS™ technology

OV5630

Copyright © 2008 OmniVision Technologies, Inc. All rights reserved.

This document is provided "as is" with no warranties whatsoever, including any warranty of merchantability, non-infringement, fitness for any particular purpose, or any warranty otherwise arising out of any proposal, specification, or sample.

OmniVision Technologies, Inc. and all its affiliates disclaim all liability, including liability for infringement of any proprietary rights, relating to the use of information in this document. No license, expressed or implied, by estoppel or otherwise, to any intellectual property rights is granted herein.

The information contained in this document is considered proprietary to OmniVision Technologies, Inc. and all its affiliates. This information may be distributed to individuals or organizations authorized by OmniVision Technologies, Inc. to receive said information. Individuals and/or organizations are not allowed to re-distribute said information.

Trademark Information

OmniVision and the OmniVision logo are registered trademarks of OmniVision Technologies, Inc. OmniPixel3-HS and CameraChip are trademarks of OmniVision Technologies, Inc.

All other trademarks used herein are the property of their respective owners.

color CMOS QSXGA (5 Megapixel) CameraChip™ sensor with OmniPixel3-HS™ technology

datasheet (CSP2)
PRELIMINARY SPECIFICATION

version 1.0
may 2008

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

Confidential
(For Truly Only)

applications

- cellular phones
- toys
- PC multimedia
- digital still camera

ordering information

- **OV05630-VL9A** (color, lead-free)
58-pin CSP2

features

- optical size of 1/3.2"
- automatic image control functions: automatic exposure control (AEC), automatic white balance (AWB), automatic band filter (ABF), automatic 50/60 Hz luminance detection, and automatic black level calibration (ABLC)
- programmable controls for frame rate, AEC/AGC, mirror and flip, cropping, windowing, and panning
- image quality controls: lens correction, defective pixel canceling
- support for output formats: 10 bit RGB RAW output, I/O tri-state configurability
- support for video or snapshot operations
- support for internal and external frame synchronization
- support for LED and flash strobe mode
- support for horizontal and vertical sub-sampling
- standard serial SCCB interface
- digital video port (DVP) parallel output interface
- MIPI interface (two lanes), MIPI hub/secondary camera interface
- embedded one-time programmable (OTP) memory
- on-chip phase lock loop (PLL)
- embedded 1.5V regulator for core power
- programmable I/O drive capability
- support for black sun cancellation
- high dynamic range (HDR) ready for sub-sampling resolution providing a dynamic range of ~ 80dB
- suitable for module size of 6.4 x 6.3 x 8.9mm
- 1.75 μ m x 1.75 μ m pixel size with Omnipixel3-HS™ structure

key specifications

- **active array size:** 2592 x 1944
- **power supply:**
core: 1.5V \pm 5% (with embedded 1.5V regulator)
analog: 2.6 ~ 3.1V (2.8V typical)
I/O: 1.7 ~ 3.1V
- **power requirements:**
active: TBD
standby: TBD
- **temperature range:**
operating: -30°C to 70°C
stable image: 0°C to 50°C
- **output formats (10-bit):** 10-bit RGB RAW output, I/O tri-state configurability
- **lens size:** 1/3.2"
- **lens chief ray angle:** 25° non-linear (see **figure 10-2**)
- **input clock frequency:** 6~27 Mhz
- **S/N ratio:** TBD
- **dynamic range:** TBD
- **maximum image transfer rate:**
QSXGA (2592x1944): 15 fps
1080p: 30 fps
720p: 60 fps
VGA (640x480): 60 fps
QVGA (320x240): 120 fps
1280x960: 60 fps
- **sensitivity:** TBD
- **shutter:** rolling shutter
- **maximum exposure interval:** TBD
- **pixel size:** 1.75 μ m x 1.75 μ m
- **well capacity:** TBD
- **dark current:** TBD
- **fixed pattern noise (FPN):** TBD
- **image area:** TBD
- **package dimensions:** 6385 μ m x 6285 μ m

Confidential
(For Truly Only)

table of contents

1	signal descriptions	1-1
2	system level description	2-1
2.1	overview	2-1
2.2	architecture	2-1
2.3	format and frame rate	2-2
2.4	SCCB interface	2-3
2.5	RESET_B	2-3
2.6	power down mode	2-3
3	block level description	3-1
3.1	pixel array structure	3-1
3.2	analog amplifier	3-2
3.3	10-bit A/D converters	3-2
4	image sensor core digital functions	4-1
4.1	mirror and flip	4-1
4.2	image cropping	4-2
4.3	test pattern	4-3
4.4	50/60hz detection	4-3
4.5	AEC and AGC algorithms	4-4
4.5.1	average-based algorithm	4-4
4.5.2	outside control zone	4-5
4.5.3	inside control zone	4-5
4.5.4	AEC	4-6
4.5.5	AGC	4-7
4.6	black level calibration (BLC)	4-10
4.7	digital gain	4-11
4.8	strobe flash control	4-11
4.8.1	strobe pulse	4-11
4.8.2	strobe pulse	4-12
4.8.3	LED1 & 2 mode	4-13
4.8.4	LED 3 mode	4-15
4.9	one-time programmable (OTP) memory	4-15
5	image sensor processor digital functions	5-1
5.1	ISP_TOP	5-1

5.2	ISP DCW, border cutting	5-1
5.3	auto white balance (AWB)	5-1
5.4	black level correction (BLC)	5-1
6	image sensor output interface digital functions	6-1
6.1	digital video port (DVP)	6-1
6.1.1	overview	6-1
6.1.2	HREF mode	6-1
6.1.3	HSYNC mode	6-5
6.1.4	three mode VSYNC output	6-5
6.1.5	DVP control registers	6-6
6.2	mobile industry processor interface (MIPI)	6-10
6.2.1	normal high speed mode	6-10
6.2.2	MIPI control registers	6-10
7	register tables	7-1
8	electrical specifications	8-1
9	mechanical specifications	9-1
9.1	physical specifications	9-1
9.2	IR reflow specifications	9-3
10	optical specifications	10-1
10.1	sensor array center	10-1
10.2	lens chief ray angle (CRA)	10-2

list of figures

figure 1-1	pin diagram	1-3
figure 2-1	OV5630 block diagram	2-2
figure 3-1	sensor array region color filter layout	3-1
figure 4-1	mirror and flip samples	4-1
figure 4-2	image cropping	4-2
figure 4-3	test pattern	4-3
figure 4-4	desired convergence	4-5
figure 4-5	histogram-based AEC/AGC reference areas	4-9
figure 4-6	xenon flash mode	4-13
figure 4-7	LED 1 & 2 mode - one pulse output	4-14
figure 4-8	LED 1 & 2 mode - multiple pulse output	4-14
figure 4-9	LED 3 mode	4-15
figure 6-1	DVP HREF timing diagram	6-1
figure 6-2	5 Megapixel timing diagram	6-2
figure 6-3	1080p timing diagram	6-3
figure 6-4	720p timing diagram	6-3
figure 6-5	VGA timing diagram	6-4
figure 6-6	960p timing diagram	6-4
figure 6-7	VSYNC output timing	6-5
figure 9-1	package specifications	9-1
figure 9-2	IR reflow ramp rate requirements	9-3
figure 10-1	sensor array center	10-1
figure 10-2	chief ray angle (CRA)	10-2

Confidential
(For Truly Only)

list of tables

table 1-1	signal descriptions	1-1
table 2-1	format and frame rate	2-2
table 4-1	mirror and flip function control	4-1
table 4-2	image cropping control registers	4-2
table 4-3	test pattern control registers	4-3
table 4-4	AEC/AGC control registers	4-4
table 4-5	AEC control functions	4-6
table 4-6	AGC control functions	4-8
table 4-7	histogram-based AEC/AGC reference area option	4-9
table 4-8	histogram-based AEC/AGC reference area option	4-10
table 4-9	digital gain control functions	4-11
table 4-10	strobe control functions	4-11
table 4-11	flashlight modes	4-12
table 4-12	OTP memory control functions	4-15
table 6-1	DVP timing	6-1
table 6-2	DVP VSYNC settings	6-5
table 6-3	DVP control registers	6-6
table 6-4	MIPI control registers	6-10
table 7-1	system control registers	7-1
table 7-2	ISP control registers	7-15
table 7-3	CIF control registers	7-18
table 7-4	clipping control registers	7-19
table 7-5	DVP control registers	7-20
table 7-6	MIPI control registers	7-24
table 8-1	absolute maximum ratings	8-1
table 8-2	DC characteristics (-30°C < TA < 70°C)	8-2
table 8-3	AC characteristics (TA = 25°C, VDD-A = 2.8V)	8-3
table 8-4	timing characteristics	8-3
table 9-1	package dimensions	9-1
table 9-2	reflow conditions	9-3
table 10-1	CRA versus image height plot	10-2

Confidential
(For Truly Only)

1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV5630 image sensor. The package information is shown in **section 9**.

table 1-1 signal descriptions (sheet 1 of 3)

pin number	signal name	pin type	description	default I/O status
A1	AVDD	power	analog power (2.6~3.1V)	power
A2	FREX	I/O	frame exposure control	input
A3	VREFN	reference	internal reference 0~2V (connect to ground using 0.1 μ F capacitor)	
A4	SVDD	power	pixel array power (2.6~3.1V)	
A5	SDA	I/O	SCCB data	
A6	VSYNC	I/O	vertical synchronization (VSYNC) output	I/O
A7	PWDN	input	power down (hardware standby)	
A8	DOGND	ground	I/O circuit ground	ground
A9	NC	–	no connect	
B1	NC	–	no connect	
B2	AGND	ground	Ground for analog circuit	ground
B3	VREFH	reference	internal reference 0~4V (connect to ground using 0.1 μ F capacitor)	
B4	SGND	ground	pixel array ground	ground
B5	SCL	input	SCCB clock	
B6	STROBE	I/O	LED output control	input
B7	RESET_B	input	hardware reset, active low	
B8	DOVDD	power	I/O circuit power (1.7~3.1V)	power
B9	DATA8	I/O	bit[8] of parallel output port / input	I/O
C1	NC	–	no connect	
C2	NC	–	no connect	
C7	DATA9	I/O	bit[9] of parallel port output / input	I/O
C8	DATA7	I/O	bit[7] of parallel output port / input	I/O
C9	DATA6	I/O	bit[6] of parallel output port / input	I/O
D1	NC	–	no connect	

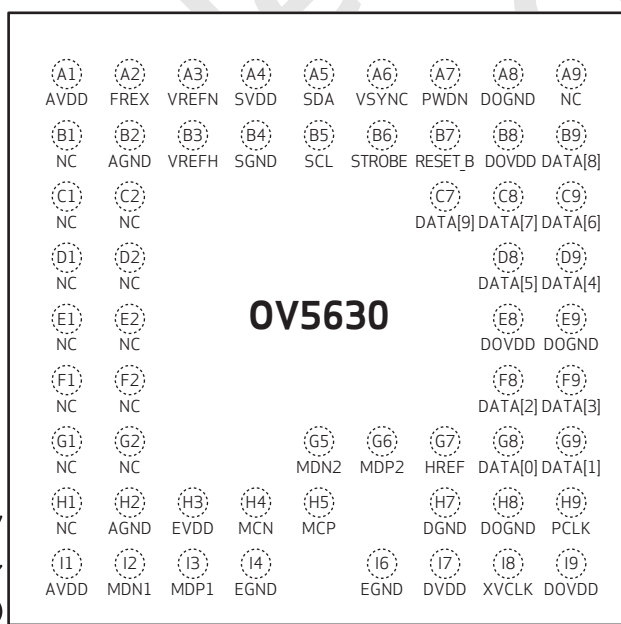
table 1-1 signal descriptions (sheet 2 of 3)

pin number	signal name	pin type	description	default I/O status
D2	NC	–	no connect	
D8	DATA5	I/O	bit[5] of parallel output port / input	I/O
D9	DATA4	I/O	bit[4] of parallel output port / input	I/O
E1	NC	–	no connect	
E2	NC	–	no connect	
E8	DOVDD	power	I/O circuit power (1.7~3.1V)	power
E9	DOGND	ground	I/O circuit ground	ground
F1	NC	–	no connect	
F2	NC	–	no connect	
F8	DATA2	I/O	bit[2] of parallel output port / input	I/O
F9	DATA3	I/O	bit[3] of parallel output port / input	I/O
G1	NC	–	no connect	
G2	NC	–	no connect	
G5	MDN2	I/O	MIPI data lane 2 negative output	
G6	MDP2	I/O	MIPI data lane 2 positive output	
G7	HREF	I/O	horizontal reference (data valid) output	
G8	DATA0	I/O	bit[0] of parallel output port / input	
G9	DATA1	I/O	bit[1] of parallel output port / input	
H1	NC	–	no connect	
H2	AGND	ground	analog ground	ground
H3	EVDD	power	MIPI power (1.5V, short to DVDD) (connect to ground using a 0.1 μ F capacitor)	
H4	MCN	I/O	MIPI clock negative output	
H5	MCP	I/O	MIPI clock positive output	
H7	DGND	ground	digital core logic ground	ground
H8	DOGND	ground	I/O circuit ground	
H9	PCLK	I/O	pixel clock output input	
I1	AVDD	power	analog power (2.6~3.1V)	power
I2	MDN1	I/O	MIPI data lane 1 negative output	
I3	MDP1	I/O	MIPI data lane 1 positive output	

table 1-1 signal descriptions (sheet 3 of 3)

pin number	signal name	pin type	description	default I/O status
14	EGND	ground	MIPI ground	ground
16	EGND	ground	MIPI ground	
17	DVDD	power	digital core logic power reference (connect to ground using a 0.1 μ F capacitor) (external supply: 1.35~1.65V, 1.5V typical)	
18	XVCLK	input	system clock input	
19	DOVDD	power	I/O circuit power (1.7~3.1V)	

figure 1-1 pin diagram



top view

5630_CSP_DS_1_1

OV5630

color CMOS QSXGA (5 Megapixel) CameraChip™ sensor with OmniPixel3-HS™ technology

Confidential
(For Truly Only)

2 system level description

2.1 overview

The OV5630 (color) CameraChip™ sensor is a low-voltage, high-performance 1/3.2-inch 5 megapixel CMOS image sensor that provides the full functionality of a single chip 5 Megapixel (2592x1944) camera using OmniPixel3-HS™ technology in a small footprint package. It provides full-frame, sub-sampled, windowed 8-bit/10-bit images in various formats via the control of the Serial Camera Control Bus (SCCB) interface or MIPI interface.

The OV5630 has an image array capable of operating at up to 15 frames per second (fps) in full resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, white balance and defective pixel canceling, etc., are programmable through the SCCB interface. In addition, Omnivision CameraChip sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

For storage purposes, the OV5630 includes a one-time programmable (OTP) memory.

The OV5630 has a two-lane MIPI interface and a traditional parallel digital video port. The sensor can also be used to communicate to an external secondary camera (digital video port) while providing continued output through the MIPI interface.

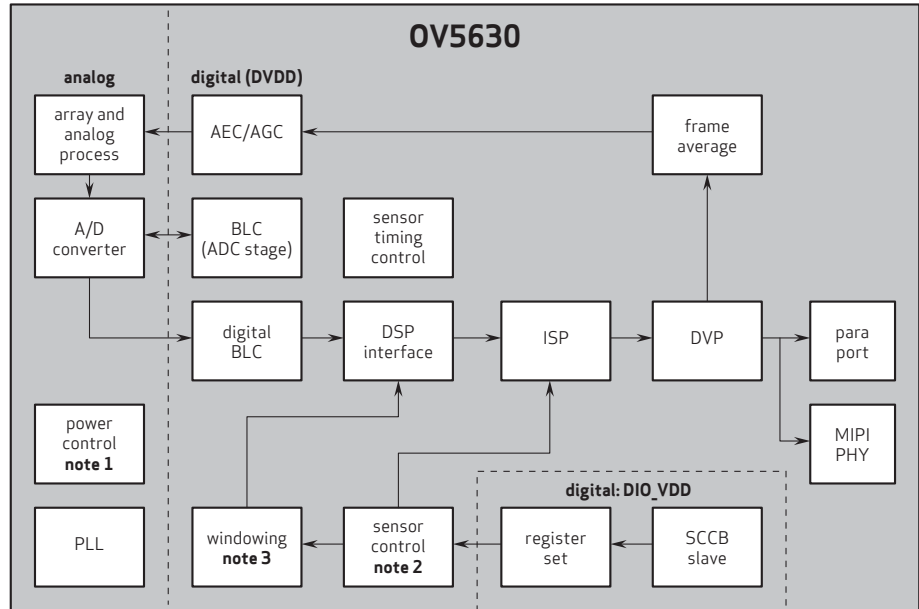
2.2 architecture

The OV5630 by HREF and VSYNC. The maximum pixel rate is 96 Megapixels per second. **figure 2-1** shows the functional block diagram of the OV5630 image sensor.

The timing generator outputs signals to access the rows of the image array, precharging and sampling the rows of array in series. In the time between pre-charging and sampling a row, the charge in the pixels decreases with the time exposed to the incident light. This is known as exposure time.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the pixel data in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. The ADC then outputs 10-bit data for each pixel in the array.

figure 2-1 OV5630 block diagram



- note 1** power control (positive and negative pump, regulator)
- note 2** sensor control (group hold, mask corrupted frame, etc.)
- note 3** windowing (crop, mirror, vflip, etc.)

5630_DS_2_3

2.3 format and frame rate

table 2-1 format and frame rate

format	resolution	frame rate	scaling method	pixel clock
5 Mpixel	2592x1944	15 fps	–	96 Mhz
1080p	1920x1080	30 fps	cropping	96 Mhz
720p	1280x720	60 fps	cropping and subsampling	96 Mhz
VGA	640x480	60 fps	subsampling	48 Mhz
QVGA	320x240	120 fps	subsampling	48 Mhz
1280x960	1280x960	30 fps	subsampling	96 Mhz

2.4 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the CameraChip sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

2.5 RESET_B

The OV5630 includes a RESET_B (pin B7) that forces a complete hardware reset when it is pulled low (ground). The OV5630 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface.

2.6 power down mode

Two methods are available to place the OV5630 into power-down mode.

- Hardware power-down may be selected by pulling the PWDN (pin A7) high (DOVDD). When this occurs, the OV5630 internal device clock is halted and all internal counters are reset. The current draw is less than 250 μ A in this standby mode.
- Software power-down through the SCCB interface suspends internal circuit activity but does not halt the device clock. The current requirements drop to less than 1 mA in this mode. All register content is maintained in standby mode.

OV5630

color CMOS QSXGA (5 Megapixel) CameraChip™ sensor with OmniPixel3-HS™ technology

Confidential
(For Truly Only)

3 block level description

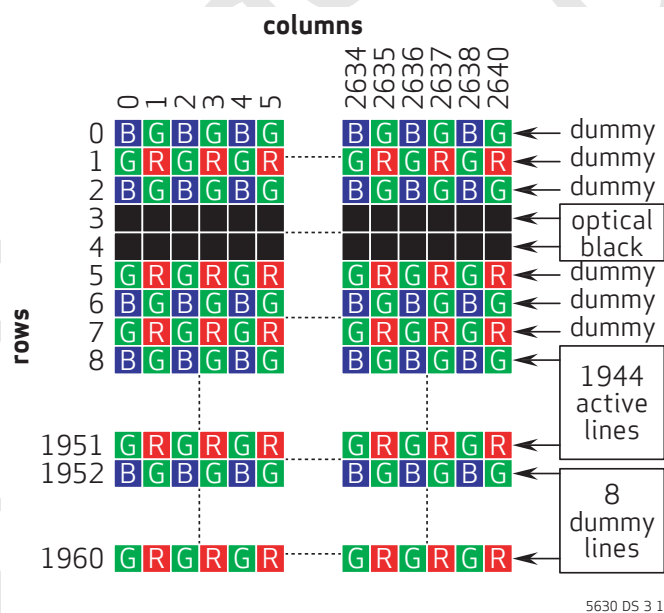
3.1 pixel array structure

The OV5630 sensor has an image array of 2640 columns by 1960 rows (5,174,400 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 5,174,400 pixels, 5,080,384 (2592x1944) are active pixels and can be output. The other pixels are used for black level calibration and interpolation. The center 2592x1944 is suggested to be output from the whole active pixel array. The backend processor can use the boundary pixels for additional processing.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1 sensor array region color filter layout



3.2 analog amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

3.3 10-bit A/D converters

The balanced signal is then digitized by the on-chip 10-bit ADC. It can operate at up to 27 MHz and is fully synchronous to the pixel clock. The actual conversion rate is determined by the frame rate.

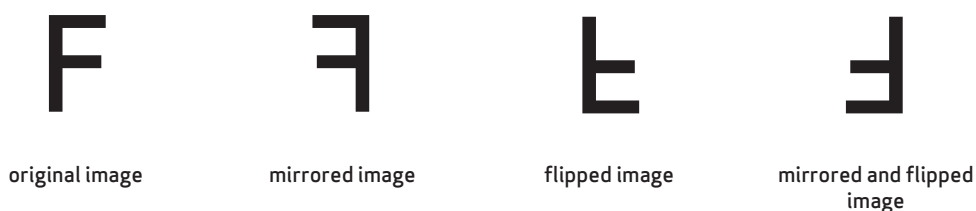
Confidential
(For Truly Only)

4 image sensor core digital functions

4.1 mirror and flip

The OV5630 provides two independent options for alternating the read-out (see [section 3.1](#)) order of the image data, horizontally mirrored and vertically flipped read-out modes, which respectively reverse the sensor data read-out order horizontally and vertically. In mirror mode, since the Bayer order changes BGBG to GBGB, we usually delay the read-out sequence by one pixel. In vertical flip mode, the ISP block will detect whether the pixel is in a red line or in a blue line and make the necessary adjustment. Thus, the OV5630 supports four pixel read-out modes (see [section 3.1](#)), standard, horizontally mirrored, vertically flipped, and both horizontally mirrored and vertically flipped, which is shown in [figure 4-1](#).

figure 4-1 mirror and flip samples



5630_DS_4.1

table 4-1 mirror and flip function control

function	register	description
mirror	0x30F8[6]	mirror ON/OFF select 0: mirror OFF 1: mirror ON
flip	0x30F8[7]	flip ON/OFF select 0: flip OFF 1: flip ON

4.2 image cropping

The image cropping area is defined by four parameters, HSTART (horizontal address start), HEND (horizontal address end), VSTART (vertical address start), and VEND (vertical address end). By properly setting these parameters, any portion within the sensor array can be cropped as a visible area. Cropping is achieved by simply masking the pixels outside the cropped window. It is independent of flip and mirror.

figure 4-2 image cropping

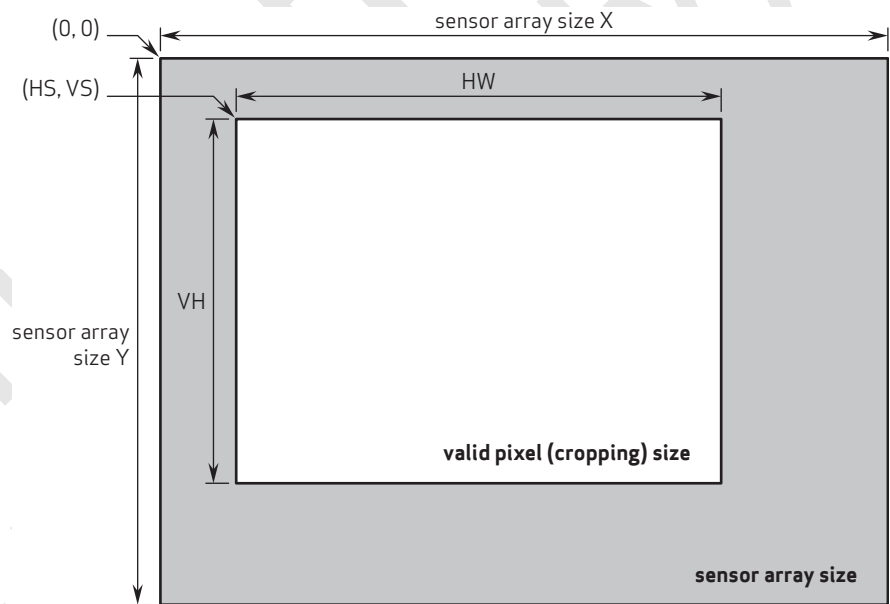


table 4-2 image cropping control registers

function	register	description
horizontal address start	{0x3024, 0x3025}	HSTART[15:8] = 0x3024 HSTART[7:0] = 0x3025
vertical address start ^a	{0x3026, 0x3027}	VSTART[15:8] = 0x3026 VSTART[7:0] = 0x3027
horizontal address end	{0x3028, 0x3029}	HEND[15:8] = 0x3028 HEND[7:0] = 0x3029
vertical address end	{0x302A, 0x302B}	VEND[15:8] = 0x302A VEND[7:0] = 0x302B

a. VS can only be an even num

4.3 test pattern

For testing purposes, the OV5630 offers one type of test pattern, color bar.

figure 4-3 test pattern

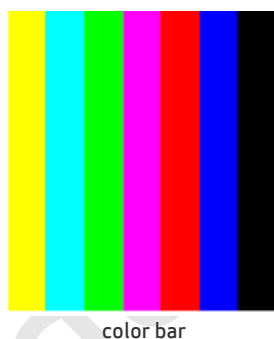


table 4-3 test pattern control registers

function	register	description
test pattern ON/OFF	0x3508[7]	test pattern ON/OFF select 0: OFF 1: ON
color bar	TBD	color bar pattern select 10: color bar pattern color bar enable 0: color bar OFF 1: color bar enable 0: color bar 1: normal image

4.4 50/60hz detection

When the integration time is not an integer multiple of the period of light intensity, the image will flicker. The function of the detector is to detect whether the sensor is under a 50Hz or 60Hz light source so that the basic step of integration time can be determined.

4.5 AEC and AGC algorithms

Auto Exposure Control (AEC) and Auto Gain Control (AGC) allow the OV5630 to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Besides automatic adjustment, exposure time and gain can also be manually controlled externally. The related registers are listed in [table 4-4](#)

table 4-4 AEC/AGC control registers

function	register	description
AEC enable	0x3013[0]	auto/manual exposure control select 0: manual 1: auto
AEC exposure time	{0x3002, 0x3003}	AEC[15:8] = 0x3002[15:8] AEC[7:0] = 0x3003[7:0]
AEC short exposure time	{0x3008, 0x3009}	AECs[15:8] = 0x3008[15:8] AECs[7:0] = 0x3009[7:0] (Only valid in HDR mode.)
AGC gain	0x3000	AGC[7:0] = 0x3000[7:0]
AGC short exposure line gain	0x3001	AGCs[7:0] = 0x3001[7:0] (only valid in HDR mode.)

4.5.1 average-based algorithm

The average-based AEC controls image luminance using registers **WPT** (0x3018) and **BPT** (0x3019). The value of register **WPT** (0x3018) indicates the high threshold value and the value of register **BPT** (0x3019) indicates the low threshold value. When the target image luminance average value **YAVG** (0x301B) is within the range specified by registers **WPT** (0x3018) and **BPT** (0x3019), the AEC keeps the current exposure time unchanged. When **YAVG** (0x301B) is greater than the value in register **WPT** (0x3018), meaning it is too bright, the AEC will decrease the exposure time. When **YAVG** (0x301B) is less than the value in register **BPT** (0x3019), meaning it is too dark, the AEC will increase the exposure time. Accordingly, the value in register **WPT** (0x3018) should be greater than the value in register **BPT** (0x3019). The gap between the values of registers **WPT** (0x3018) and **BPT** (0x3019) controls the image stability.

The AEC function supports both standard and fast adjustment when updating the exposure time so that the consequent image luminance falls into the range between **WPT** and **BPT**. AEC in standard mode allows single-step increment or decrement in the adjustment. AEC in fast mode updates the increment or decrement ten times faster.

Register **VPT** (0x301A) controls the fast AEC range. If the target image **YAVG** (0x301B) is greater than $0x301A[7:4] \times 16$, AEC will decrease by 2. If **YAVG** (0x301B) is less than $0x301A[3:0] \times 16$, AEC will increase by 2.

As shown in **figure 4-4**, the AEC/AGC convergence uses two regions, the inner stable operating region and the outer control zone, which defines the convergence step size change as follows:

4.5.2 outside control zone

step size: $2 \times (\text{AEC}[15:0])$

$t_{\text{STEP}}: t_{\text{ROW}} \times (2 \times \text{AEC}[15:0])$

4.5.3 inside control zone

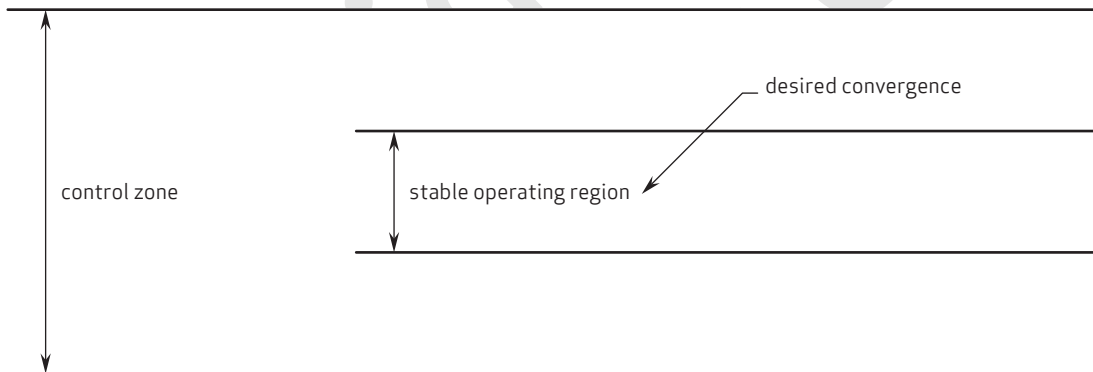
step size: $2 \times (\text{AEC}[15:0]) \div 16$

$t_{\text{STEP}}: t_{\text{ROW}} \times (2 \times \text{AEC}[15:0] \div 16)$

Once the current value is inside the stable operating region, the AEC/AGC value has converged.

The Step Limit register acts to create a "middle ground" by limiting the maximum step size to 32 rows (delay time = $t_{\text{ROW}} \times 32$).

figure 4-4 desired convergence



5630_DS_4_4

control zone upper limit: **VPT**[7:4] (0x301A[7:4]), 4'b0000}

control zone lower limit: **VPT**[3:0] (0x301A[3:0]), 4'b0000}

stable operating region upper limit: **WPT**[7:0] (0x3018)

stable operating region lower limit: **BPT**[7:0] (0x3019)

table 4-5 AEC control functions

function	register	description
WPT	0x3018	luminance signal / histogram high range for AEC/AGC operation AEC/AGC value decreases in auto mode when average luminance histogram is greater than WPT [7:0].
BPT	0x3019	luminance signal / histogram low range for AEC/AGC operation AEC/AGC value increases in auto mode when average luminance histogram is less than BPT [7:0].
VPT	0x301A	fast mode large step range thresholds - effective only in AEC/AGC fast mode Bit[7:4]: high threshold Bit[3:0]: low threshold AEC/AGC may change in larger steps when luminance average is greater than VPT[7:4] or less than VPT[3:0].
YAVG	0x301B	luminance average - this register will auto update. Average luminance is calculated from the B/Gb/Gr/R channel average as follows: B/Gb/Gr/R channel average = (BAVG[7:0] + GbAVG[7:0] + GrAVG[7:0] + RAVG[7:0]) × 0.25
fast AEC enable	0x3013[7]	AEC speed select 0: normal 1: faster AEC adjustment

4.5.4 AEC

The function of the AEC is to calculate the integration time of the next frame and send the information to the timing control block. Based on the statistics of previous frames, the AEC is able to determine whether the integration time should increase, decrease, fast increase, fast decrease, or remain unchanged.

In extremely bright situations, the LAEC activates, allowing less than one row integration time. In extremely dark situations, the VAEC activates, allowing larger than one frame integration time.

4.5.4.1 LAEC

If the integration time is only one row but the image is still too bright, the AEC enters LAEC mode. Within LAEC, the integration time can be further decreased to a minimum of 1/16 row or so. The LAEC ON/OFF can be set in register 0x3013.

4.5.4.2 banding ON mode in AEC

In Banding ON mode, the AEC step, which is also called 'band', increments by an integer multiple of the period of light intensity. The purpose of this design is to reject image flickering when the light source is not steady but periodical.

For a given operating frequency, we can express the band step in terms of row timing:

Band Step = 'period of light intensity' × 'frame rate' × 'rows per frame'

The band steps for 50 Hz and 60 Hz light sources can be set in registers 0x3070 ~ 0x3071 and 0x3072 ~ 0x3073, respectively.

When auto banding is ON and if the next integration time is less than the minimum band step, banding will automatically turn OFF. It will turn ON again when the next integration time becomes larger than the minimum band. If auto banding is disabled, the minimum integration time is one band minimum. Auto banding can be set in register 0x3013[4].

4.5.4.3 banding OFF mode in AEC

When banding is OFF, integration time increases/decreases by 1/16 of the previous step in slow mode or becomes twice/half of the previous step in fast mode.

4.5.4.4 VAEC

In extremely dark situations, the integration time needs to be longer than one frame.

The OV5630 supports long integration times such as 2 frames, 3 frames, 4 frames and 8 frames. This is achieved by slowing down the original frame rate and waiting for exposure. The VAEC ceiling can be set in register 0x3015. The VAEC can be disabled by setting register 0x3014 to 0.

4.5.5 AGC

Unlike prolonging the integration time, increasing the gain will amplify both signal and noise. Thus, the AGC usually starts after the AEC is full. However, in some cases where the adjacent AEC step changes are too large ($> 1/16$), the AGC step should be inserted between these two AEC steps. Otherwise, the integration time will keep switching from two adjacent steps and the image will flicker.

4.5.5.1 integration time between 1 ~ 16 rows

When integration time is less than 16 rows, the changes between adjacent AEC steps is larger than 1/16, which can possibly make the image oscillate between two AEC levels. Thus, some AGC steps are added in between. For example, from AEC = 2 rows to AEC = 3 rows, there are 7 more AGC steps ($1 + x/16$, $x = 1\sim7$) inserted, which ensures every step change is less than 1/16.

4.5.5.2 gain insertion between AEC banding steps

In banding ON mode, the minimum integration time change is the period of light intensity (10ms for 50 Hz or 16.67ms for 60 Hz). For the first 16 band steps, since the change between adjacent steps is larger than 1/16, AGC steps are inserted to ensure image stability.

4.5.5.3 gain insertion between VAEC steps

Between VAEC steps (e.g., integration time = 1 frame and 2 frames, AGC steps are inserted to ensure no adjacent step change is larger than 1/16.

4.5.5.4 when AEC reaches maximum

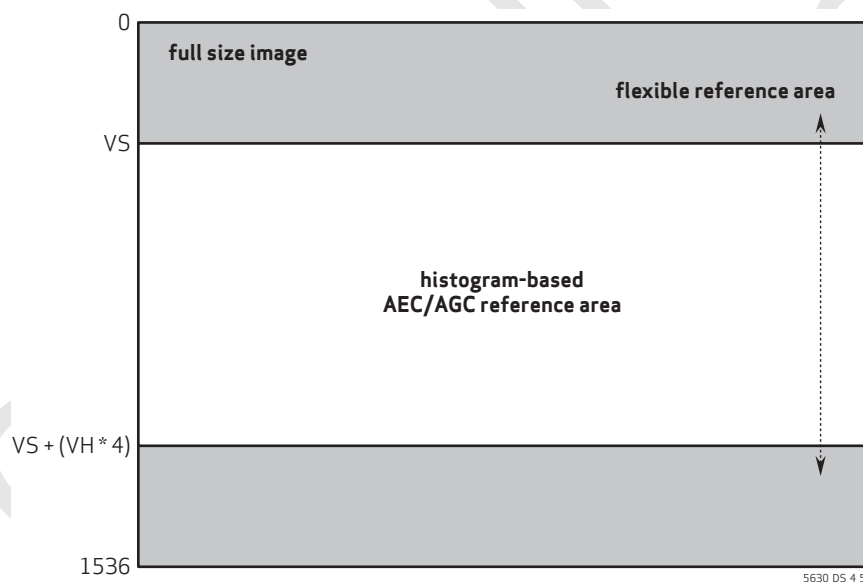
When the AEC reaches the maximum exposure time while the image is still too dark (this usually happens under super low light conditions), the AGC starts to increase until the image luminance of the frame falls into the no-adjustment region or when the AGC reaches its maximum. The AGC maximum can be set in register 0x3015.

table 4-6 AGC control functions (sheet 1 of 2)

function	register	description
LAEC ON/OFF	0x3013[3]	LAEC ON/OFF 0: ON 1: OFF
banding ON/OFF	0x3013[5]	banding ON/OFF 0: ON 1: OFF
VAEC ON/OFF	0x3014[3]	VAEC ON/OFF 0: ON 1: OFF
auto banding	0x3014[6]	auto banding ON/OFF 0: ON 1: OFF
VAEC ceiling (maximum integration time)	0x3015[6:4]	VAEC ceiling 000: 1 frame 001: 1.5 frames 010: 2 frames 011: 3 frames 100: 4 frames 101: 6 frames 110: 8 frames 111: 12 frames
AGC ceiling (maximum gain)	0x3015[2:0]	maximum gain 001: 4x 010: 8x 011: 16x 100: 32x 101: 64x 110: 128x
maximum band for 50 Hz	0x301C[5:0]	maximum band for 50 Hz in terms of row exposure

table 4-6 AGC control functions (sheet 2 of 2)

function	register	description
maximum band for 60 Hz	0x301D[5:0]	maximum band for 60 Hz in terms of row exposure
band step for 50 Hz	{0x305C,0x305D}	BD50st[15:8] = 0x305C[7:0] BD50st[7:0] = 0x305D[7:0]
band step for 60 Hz	{0x305E,0x305F}	BD60st[15:8] = 0x305E[7:0] BD60st[7:0] = 0x305F[7:0]

figure 4-5 histogram-based AEC/AGC reference areas**table 4-7** histogram-based AEC/AGC reference area option (sheet 1 of 2)

function	register	description
LAEC ON/OFF	0x3013[3]	LAEC ON/OFF select 0: OFF 1: ON
banding ON/OFF	0x3013[5]	banding ON/OFF select 0: OFF 1: ON

table 4-7 histogram-based AEC/AGC reference area option (sheet 2 of 2)

function	register	description
VAEC ON/OFF	0x3014[3]	VAEC ON/OFF select 0: OFF 1: ON
auto banding	0x3013[4]	auto banding ON/OFF select 0: OFF 1: ON
max integration time	0x3015[6:4]	VAEC ceiling 000: 1 frame 001: 1.5 frames 010: 2 frames 011: 3 frames 100: 4 frames 101: 6 frames 110: 8 frames 111: 12 frames
max_band_50hz	0x301C[5:0]	number of max banding steps for 50Hz in terms of row exposure
max_band_60hz	0x301D[5:0]	number of max banding steps for 60Hz in terms of row exposure
banding step for 50Hz	{0x305C, 0x305D}	BD50st[9:8] = 0x305C[1:0] BD50st[7:0] = 0x305D[7:0]
banding step for 60Hz	{0x305E, 0x305F}	BD60st[9:8] = 0x305E[1:0] BD60st[7:0] = 0x305F[7:0]

4.6 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used to provide the data for black level calibration.

table 4-8 histogram-based AEC/AGC reference area option

function	register	description
target	0x3069[3:0]	target black level value that is used in the algorithm
MBLC	0x306E[1]	when set, triggers BLC manually for 32 frames
BLCX2	0x307C[2]	when set, BLC will be triggered when the gain is changing (high gain)

4.7 digital gain

After black level subtraction, multiplication may apply to all pixel values based on an optional digital gain. By default, the sensor will use analog gain up to its maximum before applying digital gain to the pixel.

table 4-9 digital gain control functions

function	register	description
digital gain enable	0x307C[5]	digital gain enable 0: disable 1: enable
digital gain select	0x307E[7:6]	range of digital gain 00: apply digital gain only if gain $\geq 2x$ 01: apply digital gain only if gain $\geq 4x$ 1x: apply digital gain only if gain $\geq 8x$

4.8 strobe flash control

To achieve the best image quality possible under low light conditions, the use of strobe flash is recommended. The OV5630 provides a programmable strobe signal function.

4.8.1 strobe pulse

The OV5630 can generate a programmable strobe signal from the **STROBE** pin (table 4.9). lists the strobe pulse control registers.

table 4-10 strobe control functions (sheet 1 of 2)

function	register	description
strobe function enable	0x30E8 [7]	strobe function enable 0: strobe disable 1: start strobe enable
strobe output pulse polarity control	0x30E8 [6]	strobe output polarity control 0: positive pulse 1: negative pulse
xenon mode strobe pulse width	0x30E8 [3:2]	xenon mode pulse width 00: 1 line 01: 2 lines 10: 3 lines 11: 4 lines

table 4-10 strobe control functions (sheet 2 of 2)

function	register	description
strobe mode	0x30E8 [1:0]	strobe mode select 00: xenon mode 01: LED 1 & 2 mode 10: LED 1 & 2 mode 11: LED 3 mode

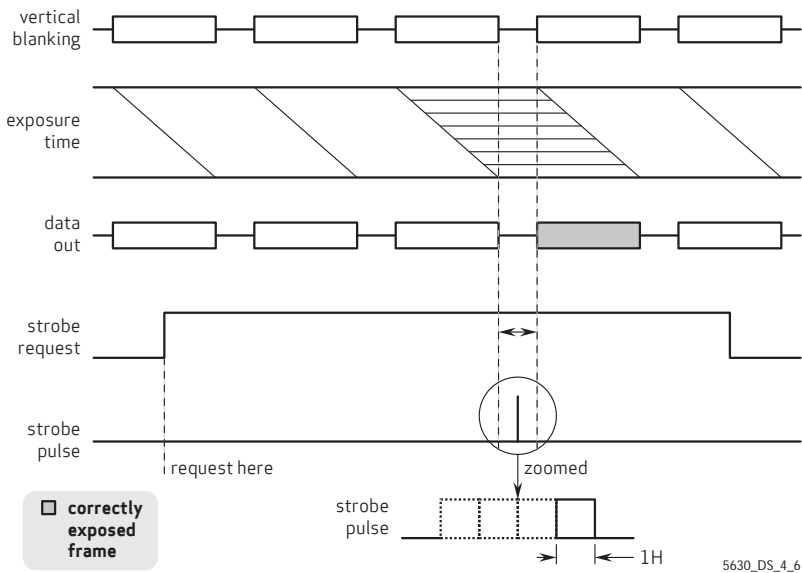
4.8.2 strobe pulse

The strobe signal is programmable and supports both LED and Xenon modes. The polarity of the pulse can be changed. The strobe signal is enabled (turned high/low depending on the pulse's polarity) by requesting the signal via the SCCB. Flash modules are typically triggered by the rising edge (falling edge if the signal polarity is changed). It supports the flash modes shown in [table 4-11](#).

table 4-11 flashlight modes

function	register	description
xenon	one pulse	no
LED 1	pulse	no
LED 2	pulse	no
LED 3	continuous	yes

figure 4-6 xenon flash mode



4.8.3 LED1 & 2 mode

Two frames after the strobe request is submitted, the third frame is correctly exposed. The strobe pulse will be activated only one time if the strobe end request is set correctly (see [figure 4-7](#)). If end request is not sent, the strobe signal is activated intermittently until the strobe end request is set (see [figure 4-8](#)). The number of skipped frames is programmable.

figure 4-7 LED 1 & 2 mode - one pulse output

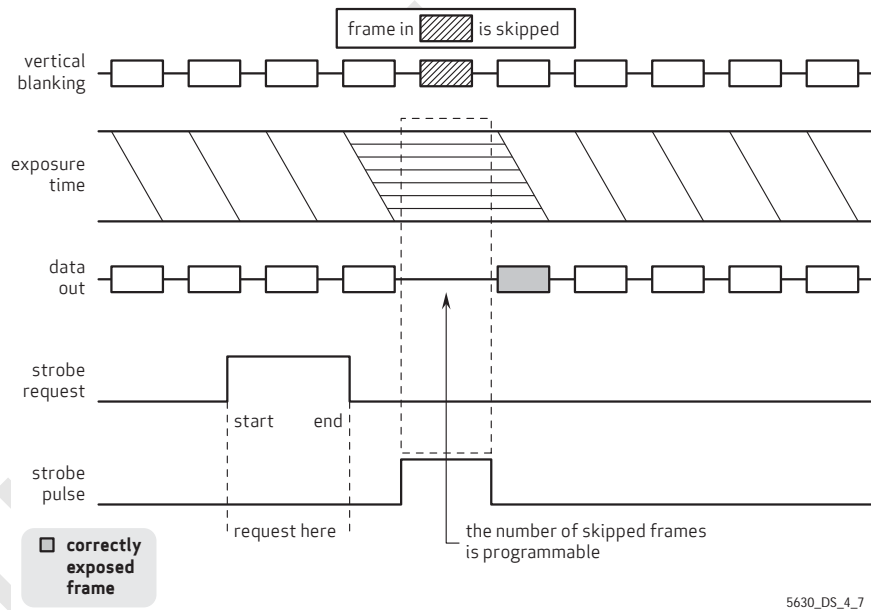
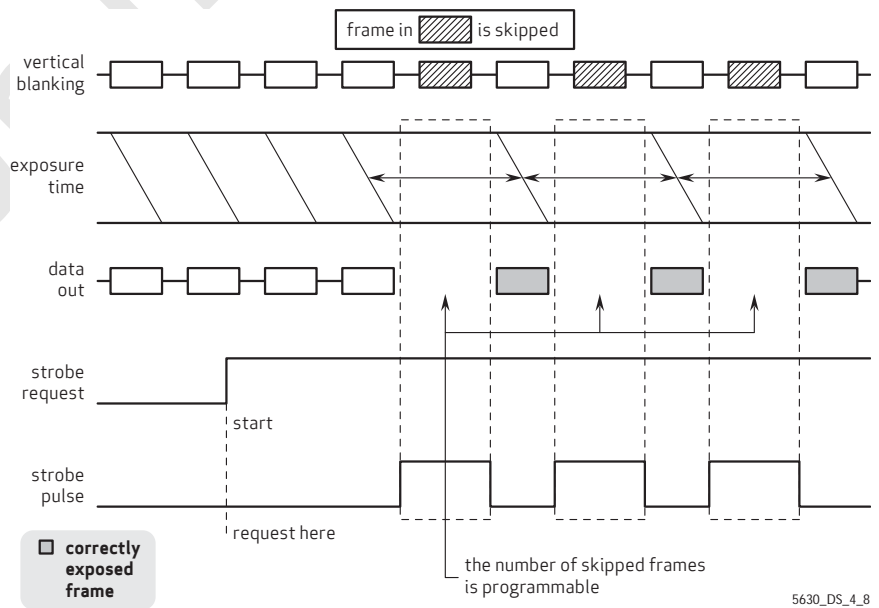


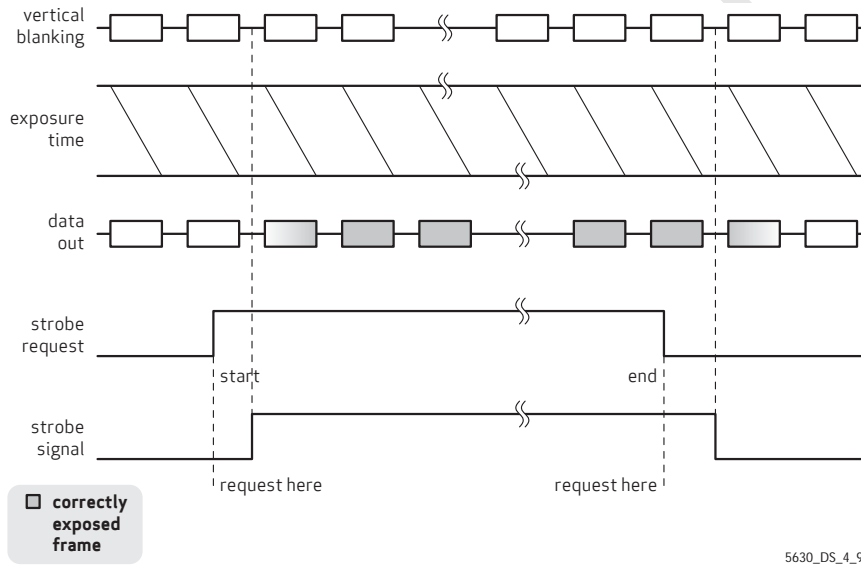
figure 4-8 LED 1 & 2 mode - multiple pulse output



4.8.4 LED 3 mode

In LED 3 mode, the strobe signal stays active until the strobe end request is sent (see [figure 4-9](#)).

figure 4-9 LED 3 mode



4.9 one-time programmable (OTP) memory

The high-density one-time programmable (OTP) memory of the OV5630 is organized as 128-bit by 1 electrical fuse with a random access interface. The main function is to store chip identification and manufacturing information.

The OTP memory has three operation modes, program, read, and inactive. It is in inactive mode by default. When register 0x303E is set to 0xAA, the OTP memory enters program mode and data in the OTP registers (0x30D0~0x30DF) are sequentially burned into the OTP memory. When register 0x303E is set to 0x55, the OTP memory enters read mode and data in the OTP memory are read out and loaded into the OTP registers (0x30D0~0x30DF). [table 4-12](#) summarizes the corresponding registers.

table 4-12 OTP memory control functions

function	register	description
OTP program data	0x30D0~0x30DF	data to be programmed/read into/from OTP for customer
OTP program/read enable	0x303E	OTP read/write control 0x55: read from OTP memory 0xAA: write to OTP memory

OV5630

color CMOS QSXGA (5 Megapixel) CameraChip™ sensor with OmniPixel3-HS™ technology

Confidential
(For Truly Only)

5 image sensor processor digital functions

5.1 ISP_TOP

The ISP_TOP includes all module enable signals, buffer power down control, top level control signals as well as ISP modules that require control bytes (WBC).

- White Black pixel Canceling (WBC) is used to detect and remove defect pixels.

5.2 ISP DCW, border cutting

This part includes the size registers for ISP input windowing, ISP output windowing, and scaling input windowing. The ISP input windowing is designed to support digital zoom. The ISP output windowing and scaling input windowing are both for cutting some border pixels or border lines which are not good enough due to algorithm limitation.

5.3 auto white balance (AWB)

The main purpose of the Auto White Balance (AWB) function is to automatically correct the white balance of the image. There are two main functions AWB: AWB_Stat and AWB_Gain.

- AWB_Stat is used to automatically generate digital gains for different light sources
- AWB_Gain is used to apply the AWB_Stat gains on RAW data to remove unrealistic color

The main purpose of the Lens Correction (LENC) function is to compensate for lens imperfection. According to the radius of each pixel to the lens, the module calculates a gain for the pixel, correcting each pixel with its gain calculated to compensate for the light distribution due to lens curvature.

5.4 black level correction (BLC)

Black Level Correction (BLC) is used to adjust black level situations.

OV5630

color CMOS QSXGA (5 Megapixel) CameraChip™ sensor with OmniPixel3-HS™ technology

Confidential
(For Truly Only)

6 image sensor output interface digital functions

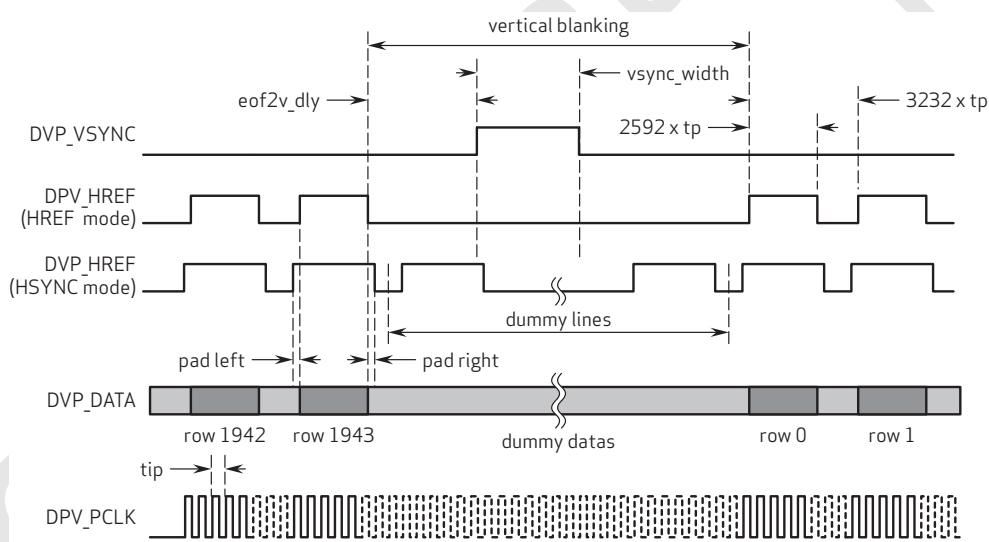
6.1 digital video port (DVP)

6.1.1 overview

The Digital Video Port (DVP) provides 10-bit and 8-bit parallel data output in all formats supported and extended features including HREF, CCIR656 format, HSYNC mode and test pattern output.

6.1.2 HREF mode

figure 6-1 DVP HREF timing diagram



note: 1. DVP_PCLK can be optional gated when DVP_HREF is low.
2. Polarity of DVP_VSYNC, DVP_HREF, DVP_PCLK can be switched separately.

5630_D5_6_1

table 6-1 DVP timing (sheet 1 of 2)

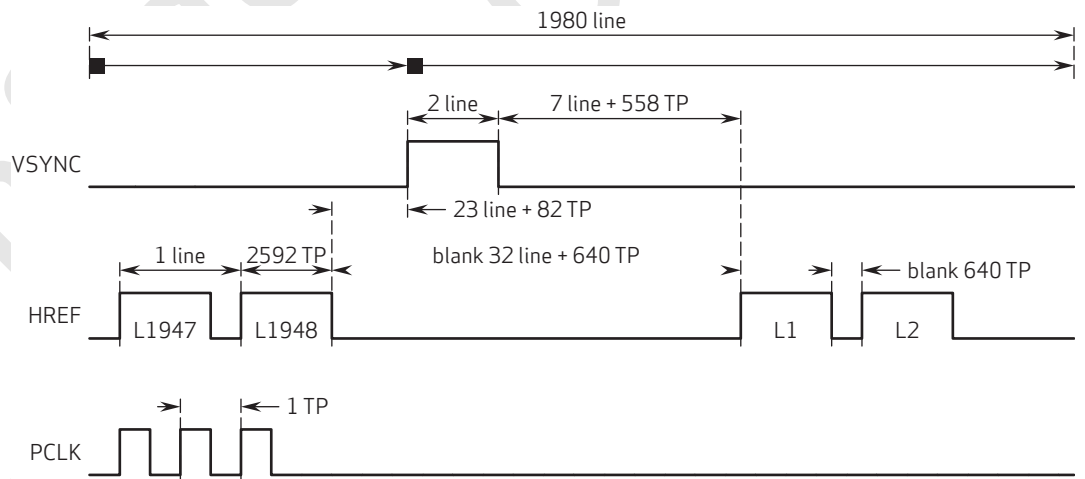
symbol	parameter	registers	typ	unit
Tp	PCLK period	–	10.4	ns
eof2v_dly ^a	PCLK numbers from end of the frame to rising edge VSYNC of the next frame	{0x3509,0x350A, 0x350B}	256	tp
v2h_dly	PCLK numbers from VSYNC falling edge to the first HREF rising edge	0x3515	0	tp
h2v_dly	PCLK numbers from the last HREF falling edge to next frame VSYNC rising edge	0x3514	0	tp

table 6-1 DVP timing (sheet 2 of 2)

symbol	parameter	registers	typ	unit
pad_right	dummy pixel numbers at the end of a line	0x350C	0	tp
pad_left	dummy pixel numbers at the beginning of a line	0x350D	0	tp
vsync_width	PCLK numbers of VSYNC	{0x350E[5:4], 0x3507[7:1],5'h0}	2048	tp

a. eof2v_dly, vsync_width and h2v_dly, v2h_dly are variable for different VSYNC mode.

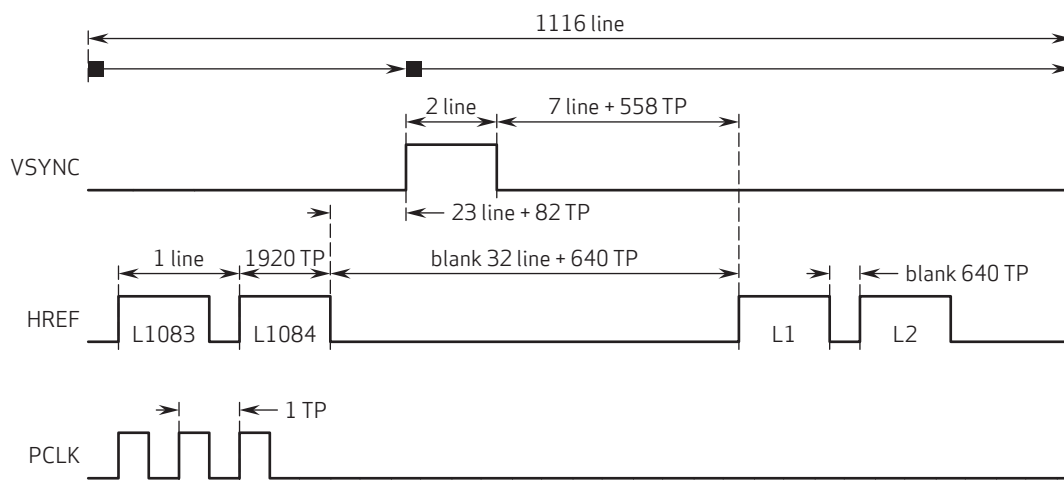
figure 6-2 5 Megapixel timing diagram



note 1 TP = 1/96M
 1 line = 3232 TP
 Sys CLK = 96MHz
 four more lines are added in each resolution for BLC

5630_DS_6_2

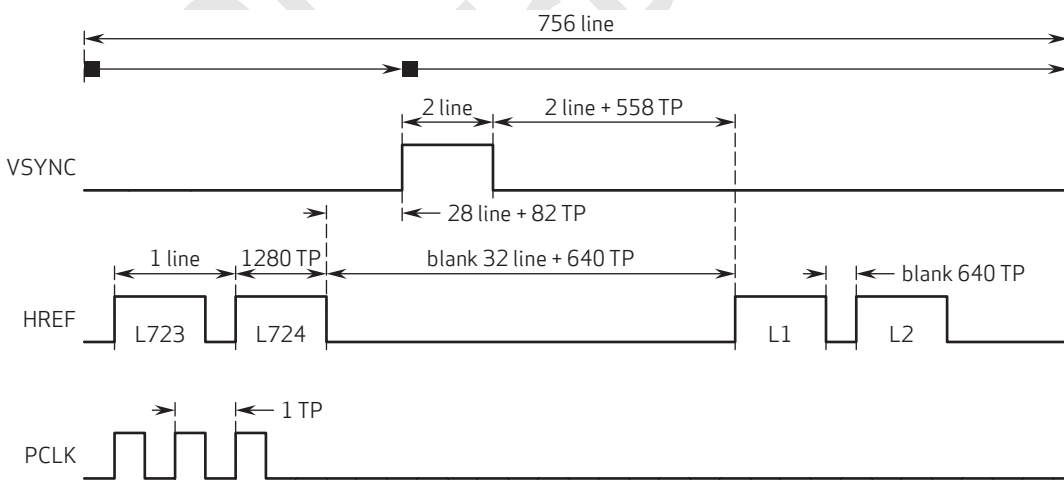
figure 6-3 1080p timing diagram



note 1 TP = 1/96M
 1 line = 2560 TP
 Sys CLK = 96MHz
 four more lines are added in each resolution for BLC

5630_DS_6.3

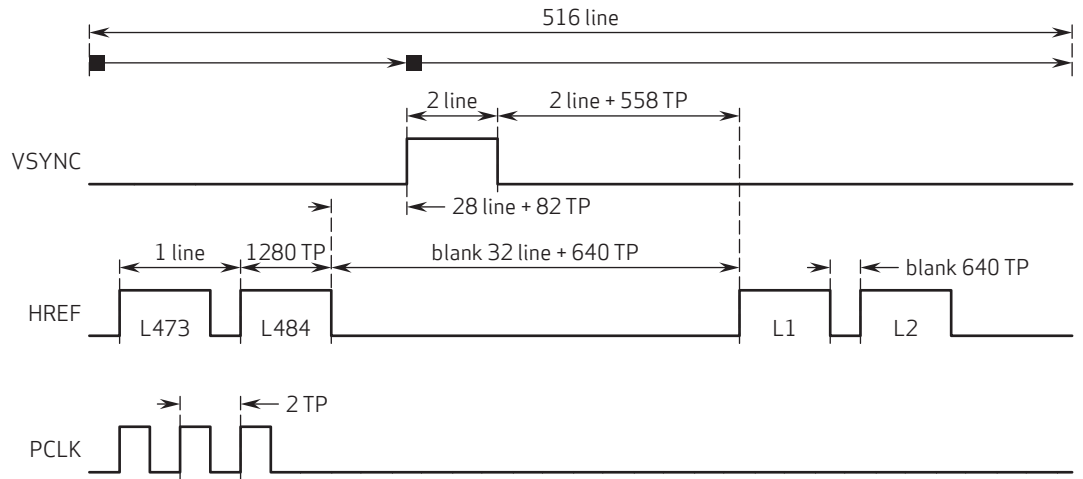
figure 6-4 720p timing diagram



note 1 TP = 1/96M
 1 line = 1920 TP
 Sys CLK = 96MHz
 four more lines are added in each resolution for BLC

5630_DS_6.4

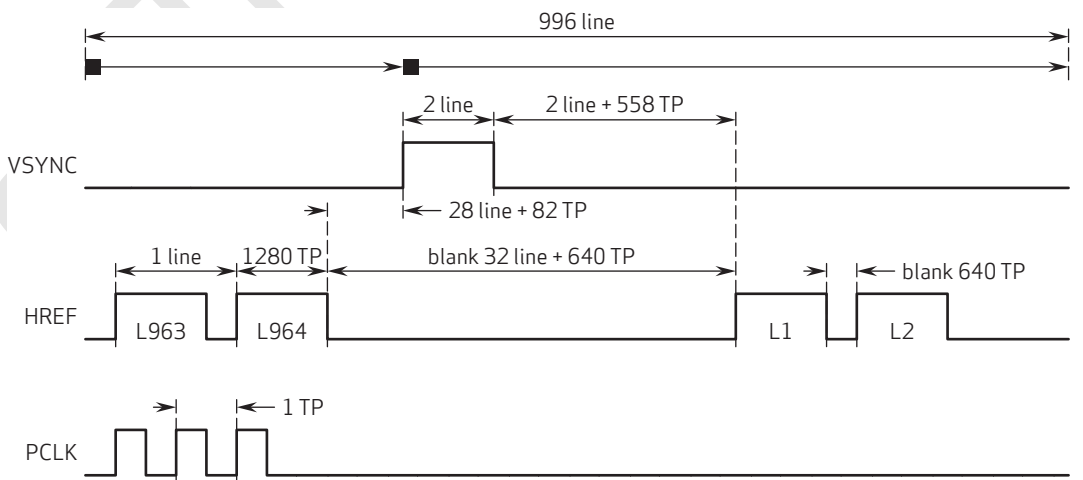
figure 6-5 VGA timing diagram



note 1 TP = 1/96M
 1 line = 1920 TP
 Sys CLK = 96MHz
 four more lines are added in each resolution for BLC

5630_DS_6_5

figure 6-6 960p timing diagram



note 1 TP = 1/96M
 1 line = 1920 TP
 Sys CLK = 96MHz
 four more lines are added in each resolution for BLC

5630_DS_6_6

6.1.3 HSYNC mode

In this mode, the line blanking time and VSYNC to the first image line are fixed. Also, there are dummy lines when vertical blanking. Only need to write register 0x3506 to 0x30 to enable HSYNC mode.

6.1.4 three mode VSYNC output

The OV5630 supports three different VSYNC output timing modes, vsync_old, vsync_new, and vsync_three.

vsync_three is the default output mode. **figure 6-7** describes the three VSYNC timing modes and **table 6-2** are the relative registers of VSYNC.

figure 6-7 VSYNC output timing

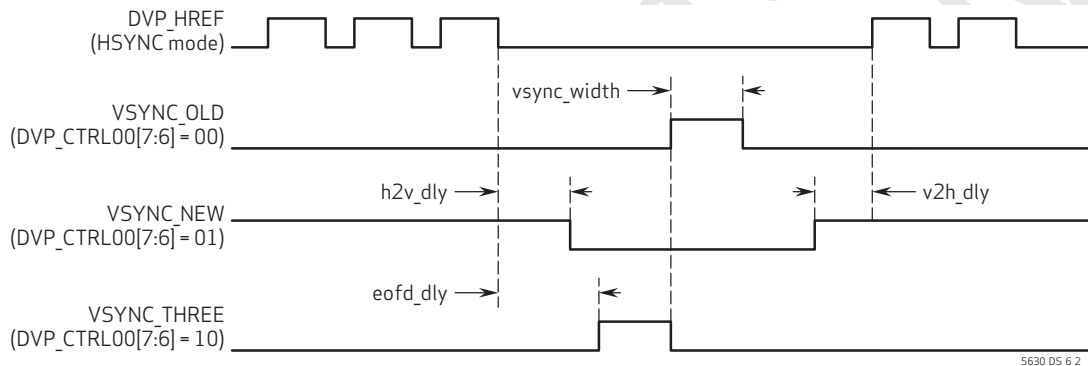


table 6-2 DVP VSYNC settings

mode	control mode	timing control	registers	default value
vsync_old	0x3500[7:6] = 2'h0	vsync_width	{0x350E[5:4], 0x3507[7:1], 5'h0}	2048
vsync_new	0x3500[7:6] = 2'h1	h2v_dly	0x3514	0
		v2h_dly	0x3515	0
vsync_three	0x3500[7:6] = 2'h2	eof2v_dly	{0x3509, 0x350A, 0x350B}	256
		vsync_width	{0x350E[5:4], 0x3507[7:1], 5'h0}	2048

6.1.5 DVP control registers

table 6-3 DVP control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3500	DVP_CTRL00	0x80	RW	<p>DVP Control 00</p> <p>Bit[7:6]: VSYNC select</p> <p>00: Select vsync_old</p> <p>01: Select vsync_new</p> <p>10: Select vsync_three</p> <p>11: Reserved</p> <p>Bit[5]: pclk_gate_en</p> <p>1: Gate dvp_pclk when HREF is low</p> <p>Bit[4]: vsync_gate</p> <p>0: Gate dvp_pclk when VSYNC and pclk_gate_en is high</p> <p>1: Do not gate dvp_pclk when VSYNC is high</p> <p>Bit[3]: dmy_line_sel</p> <p>0: Auto generate dummy lines</p> <p>1: Use first lines as dummy lines</p> <p>Bit[2]: Change polarity of PCLK</p> <p>Bit[1]: Change polarity of HREF</p> <p>Bit[0]: vsync_pol</p> <p>0: VSYNC = 1 is frame blanking time</p>

table 6-3 DVP control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3501	DVP_CTRL01	0x00	RW	DVP Control 01 Bit[7]: ccir656_en Bit[6]: sync_code_sel 0: Auto generate sync_code 1: Use FS, FE, LS and LE as ccir656 sync_code Bit[5]: vhref_tst (reserved) 1: Use dvp_data_o to output vhref_i Bit[4]: data_order 0: DVP output dvp_data[11:0] 1: DVP output dvp_data[0:11] Bit[3]: dvp_bit8 0: Swap 2 bit when dvp_h and dvp_l 1: Swap 4 bit Bit[2]: dvp_h 0: Output dvp_data[11:0] 1: Output dvp_data{n:0, 11:n-1} n: 7 or 9 Bit[1]: dvp_l 0: Select dvp_data[11:0] 1: Select dvp_data{n:0, 11:n+1} n: 3 or 1 Bit[0]: ch_flag - write 1 to it to generate flag for HSYNC mode
0x3502	DVP_CTRL02	0xAB	RW	DVP Control 02 Bit[7:0]: CCIR656 sync code for FS
0x3503	DVP_CTRL03	0xB6	RW	DVP Control 03 Bit[7:0]: CCIR656 sync code for FE
0x3504	DVP_CTRL04	0x80	RW	DVP Control 04 Bit[7:0]: CCIR656 sync code for LS
0x3505	DVP_CTRL05	0x9D	RW	DVP Control 05 Bit[7:0]: CCIR656 sync code for LE
0x3506	DVP_CTRL06	0x20	RW	DVP Control 06 Bit[7:6]: Reserved Bit[5]: dvp_en Bit[4]: hsync_en Bit[3:0]: Reserved
0x3507	DVP_CTRL07	0x80	RW	DVP Control 07 Bit[7:1]: vsync_width[7:1] - width of VSYNC when selecting vsync_old and vsync_three Bit[0]: hskip_man_o[0]

table 6-3 DVP control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3508	DVP_CTRL08	0x00	RW	DVP Control 08 Bit[7]: tst_ptn_en Bit[6]: tst_bit8 Bit[5]: tst_bit12 Bit[4]: tst_mode 0: 00, 01, 02, ..., 80, FF 1: 00, 00, 01, 01, ..., FF, FF Bit[3:0]: dmy_line_nu
0x3509	DVP_CTRL09	0x00	RW	DVP Control 09 Bit[7:0]: eof2v_dly[23:16]
0x350A	DVP_CTRL0A	0x01	RW	DVP Control 0A Bit[7:0]: eof2v_dly[15:8]
0x350B	DVP_CTRL0B	0x00	RW	DVP Control 0B Bit[7:0]: eof2v_dly[7:0]
0x350C	DVP_CTRL0C	0x00	RW	DVP Control 0C Bit[7:0]: pad_right
0x350D	DVP_CTRL0D	0x00	RW	DVP Control 0D Bit[7:0]: pad_left
0x350E	DVP_CTRL0E	0x40	RW	DVP Control 0E Bit[7:6]: Reserved Bit[5:4]: vsync_width[9:8] Bit[3:1]: Reserved Bit[0]: skip_man_en_o

table 6-3 DVP control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x350F	DVP_CTRL0F	0x88	RW	DVP Control 0F Bit[7]: eav_first 0: sav_first 1: eav_first Bit[6]: f_sel Bit[5]: f_value Bit[4]: fix_f 0: Auto generate ccir_f 1: Use f_value as ccir_f Bit[3:2]: blk_sel 00: Select 12'h800 and 12'h100 as toggle data x1: Selet 12'h000 as toggle data 10: Select tog0 and tog1 as toggle data Bit[1]: no_sof 0: Reset state machine at SOF 1: Do not reset state machine at SOF Bit[0]: no_clip 0: Clip output data between 10'h004 and 10'h3FB 1: Do not clip output data when in CCIR656 mode
0x3510	DVP_CTRL10	0x09	RW	DVP Control 10 Bit[7:4]: Reserved Bit[3:2]: tog0[11:10] - toggle data0 when line blanking or dummy lines Bit[1:0]: tog1[11:10] - toggle data1 when line blanking or dummy lines
0x3511	DVP_CTRL11	0xAA	RW	DVP Control 11 Bit[7:0]: tog0[9:2] - toggle data0 when line blanking or dummy lines
0x3512	DVP_CTRL12	0x55	RW	DVP Control 12 Bit[7:0]: tog1[9:2] - toggle data1 when line blanking or dummy lines
0x3513	DVP_CTRL13	0x02	RW	DVP Control 13 Bit[7:0]: Reserved
0x3514	DVP_CTRL14	0x00	RW	DVP Control 14 Bit[7:0]: h2v_dly
0x3515	DVP_CTRL15	0x00	RW	DVP Control 15 Bit[7:0]: v2h_dly

6.2 mobile industry processor interface (MIPI)

The MIPI interface fully supports the MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) and the MIPI Alliance Specification for D-PHY. The MIPI interface provides a single uni-directional clock lane and two bi-directional data lane solution for communication links between components inside a mobile device. The two data lanes fully support the HS (uni-direction) and LP (bi-direction) data transfer modes.

6.2.1 normal high speed mode

The default is to use two lanes to output HS data with a free running clock lane. The user only needs to set `pclk_period` (0x3637), which is the pixel clock period of MIPI_TOP. It will affect the global timing of MIPI_DPHY_spec. The default value is 8 ns (one bit decimal).

6.2.2 MIPI control registers

table 6-4 MIPI control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3010	PLL_3	0x41	RW	PLL Control Bit[5]: LaneDiv control bit 0: Use one lane to transfer HS data 1: Use two lanes to transfer HS data Bit[3:0]: Scale_Div control bits
0x3601	MIPI_CTRL01	0x01	RW	Bit[0]: bit8 1: 8-bit mode
0x3602	MIPI_CTRL02	0x22	RW	Bit[2]: line_sync_en 1: Send line sync short packet for MIPI Bit[1]: gate_sc_en 1: Gate MIPI clock when no packet
0x3603	MIPI_CTRL03	0x49	RW	Bit[2]: ph_byte_order for ECC 0: {DI,WC_l,WC_h} 1: {DI,WC_h,WC_l} Bit[1]: ph_bit_order for ECC {DI[7:0],WC[7:0],WC[15:8]} 1: {DI[0:7],WC[0:7],WC[8:15]}
0x360C	MIPI_CTRL0C	0x12	RW	Bit[7:6]: VC, virtual channel ID
0x360E	MIPI_CTRL0E	0x23	RW	Bit[5:0]: wkup_dly 1 ms wakeup delay/4096 for MIPI ultra low power resume, sclk cycle fir MARK1)

table 6-4 MIPI control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3610	MIPI_CTRL10	0x40	RW	Bit[7:0]: Width_man[7:0]/4, when in JPEG mode user can use width_man to set the width of each image line
0x3611	MIPI_CTRL11	0x0C	RW	Bit[7:5]: width_man[10:8], Width_man_real = width_man × 4
0x361F	MIPI_CTRL1F	0x0E	RW	Bit[7:0]: PCLK_period PCLK2x period, 1-bit decimal and unit is ns PCLK_PERIOD should be set according to the PLL setting. It affects the MIPI_DPHY timing. The PCLK2x cycles when HS_ZERO_SEL=1, and the unit is ns when HS_ZERO_SEL=0
0x3622	MIPI_CTRL22	0x28	RW	Bit[7:2]: n × UI for t_hs_zero Minimum high speed zero Bit[1:0]: Min_hs_zero_high Unit is PCLK2x cycles when hs_zero_sel = 1 and unit is ns when hs_zero_sel = 0
0x3623	MIPI_CTRL23	0x96	RW	Bit[7:0]: min_hs_zero_low
0x3624	MIPI_CTRL24	0x10	RW	Bit[7:2]: n × UI for t_hs_trail Minimum high speed trail Bit[1:0]: Min_hs_trail_high Unit is PCLK2x cycles when hs_trail_sel = 1 and unit is ns when hs_trail_sel = 0
0x3625	MIPI_CTRL25	0x3C	RW	Bit[7:0]: min_hs_trail_low
0x3626	MIPI_CTRL26	0x01	RW	Bit[7:2]: n × UI for t_clk_zero Minimum clock zero Bit[1:0]: Min_clk_zero_high Unit is PCLK2x cycles when clk_zero_sel = 1 and unit is ns when clk_zero_sel = 0
0x3627	MIPI_CTRL27	0x86	RW	Bit[7:0]: Min_clk_zero_low
0x3628	MIPI_CTRL28	0x00	RW	Bit[7:2]: n × UI for min_clk_pre Minimum clock prepare time Bit[1:0]: Min_clk_pre_high Unit is PCLK2x cycles when clk_prepare_sel = 1 and unit is ns when clk_prepare_sel = 0
0x3629	MIPI_CTRL29	0x32	RW	Bit[7:0]: Min_clk_pre_low

table 6-4 MIPI control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x362A	MIPI_CTRL2A	0x00	RW	Bit[7:2]: n × UI for max_clk_pre Maximum clock prepare time Bit[1:0]: max_clk_pre_high, unit is ns
0x362B	MIPI_CTRL3B	0x8C	RW	Bit[7:0]: Max_clk_pre_low
0x362C	MIPI_CTRL3C	0xD0	RW	Bit[7:2]: n × UI for min_clk_post, minimum clk_post Bit[1:0]: Min_clk_post_high Unit is PCLK2x cycles when clk_post_sel = 1 and unit is ns when clk_post_sel = 0
0x362D	MIPI_CTRL2D	0x56	RW	Bit[7:0]: min_clk_post_low
0x362E	MIPI_CTRL2E	0x00	RW	Bit[7:2]: n × UI for min_clk_trail Bit[1:0]: Min_clk_trail_high Unit is PCLK2x cycles when clk_trail_sel = 1 and unit is ns when clk_trail_sel = 0
0x362F	MIPI_CTRL2F	0x3C	RW	Bit[7:0]: Min_clk_trail_low
0x3630	MIPI_CTRL30	0x00	RW	Bit[7:2]: n × UI for min_lpx_p Bit[1:0]: Min_lpx_p_high, unit is PCLK2x cycles when lpx_p_sel = 1 and unit is ns when lpx_p_sel = 0
0x3631	MIPI_CTRL31	0x32	RW	Bit[7:0]: Min_lpx_p_low
0x3632	MIPI_CTRL32	0x10	RW	Bit[7:2]: n × UI for min_hs_prepare Bit[1:0]: min_hs_prepare_high Unit is PCLK2x cycles when hs_prepare_sel = 1 and unit is ns when hs_prepare_sel = 0
0x3633	MIPI_CTRL33	0x2A	RW	Bit[7:0]: Min_hs_prepare_low
0x3634	MIPI_CTRL34	0x18	RW	Bit[7:2]: n × UI for max_hs_prepare Bit[1:0]: Max_hs_prepare_high Unit is ns
0x3635	MIPI_CTRL35	0x55	RW	Bit[7:0]: Max_hs_prepare_low
0x3636	MIPI_CTRL36	0x00	RW	Bit[7:2]: n × UI for min_hs_exit Bit[1:0]: min_hs_exit_high Unit is PCLK2x cycles when hs_exit_sel = 1 and unit is ns when hs_exit_sel = 0
0x3637	MIPI_CTRL37	0x64	RW	Bit[7:0]: Min_hs_exit_low

table 6-4 MIPI control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x363D	MIPI_CTRL3D	0x60	RW	Bit[6]: JPG_pad_en 1: MIPI_FIFO will pad pixels to meet width_man
0x364C	MIPI_CTRL4C	0x00	RW	Bit[2]: Ph_byte_order2 0: ph = {di,wc} for ECC 1: ph = {wc,di}

Confidential
(For Truly Only)

OV5630

color CMOS QSXGA (5 Megapixel) CameraChip™ sensor with OmniPixel3-HS™ technology

Confidential
(For Truly Only)

7 register tables

The following tables provide descriptions of the device control registers contained in the OV5630. For all registers enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x6C for write and 0x6D for read.

table 7-1 system control registers (sheet 1 of 14)

address	register name	default value	R/W	description
0x3000	AGCL	0x00	RW	Sensor Gain, or Sensor Long Exposure Gain when used in HDR mode auto or manual Byte: low
0x3001	AGCS	0x00	RW	Sensor Short Exposure Gain, only used in HDR mode auto or manual
0x3002	AECL	0x00	RW	Coarse Exposure Time Auto or Manual Byte: High Units: Lines
0x3003	AECL	0x00	RW	Coarse Exposure Time Auto or Manual Byte: High Units: Lines
0x3004	LAEC	0x00	RW	Fine Exposure Time Auto or Manual Byte: High Units: System clocks
0x3005	LAEC	0x00	RW	Fine Exposure Time Auto or Manual Byte: high Units: System clocks
0x3006	AGCH	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor gain auto or manual Byte: High
0x3007	RSVD	–	–	Reserved
0x3008	AECS	0x00	RW	Coarse Exposure Time HDR Auto Or Manual Byte: High Units: Lines
0x3009	AECS	0x00	RW	Coarse Exposure Time HDR Auto Or Manual Byte: High Units: Lines
0x300A	PIDH	0x56	RW	ID Byte: High
0x300B	PIDL	0x32	RW	ID Byte: Low
0x300C	SCCB_ID	0x6C	RW	SCCB_ID
0x300D	RSVD	–	–	Reserved

table 7-1 system control registers (sheet 2 of 14)

address	register name	default value	R/W	description
0x300E	R_PLL1	0x38	RW	Bit[7:6]: PLL pre divider 00: 1 01: 1.5 10: 2 11: 3 Bit[5:0]: PLL divider PLLDiv=64-plldiv[5:0]
0x300F	R_PLL2	0x01	RW	Bit[7:4]: System clock divider ratio=r_divs[3:0]+1 Bit[3:0]: MIPI divider ratio=r_divm[3:0]+1
0x3010	R_PLL3	0x02	RW	Bit[7]: Bypass PLL Bit[6:4]: PLL charge pump current control Bit[3]: Reserved Bit[2]: LaneDiv control Bit[0]: LaneDiv=1 1: LaneDiv = 2 Bit[1:0]: DIV4/5 control 00: Ratio = 1 01: Ratio = 1 10: Ratio = 4 11: Ratio = 5
0x3011	R_PLL4	0x40	RW	Bit[7:6]: Digital clock input divider 00: 1 01: 2 10: 4 11: 4 Bit[5:0]: Reserved
0x3012	SYS	0x00	RW	System Control Bit[7]: Software system reset Bit[6:0]: Reserved
0x3013	AUTO_1	0x00	RW	AEC Enable
0x3014	AUTO_2	0x00	RW	Old Banding ALG
0x3015	AUTO_3	0x00	RW	High Gain Limit
0x3016	AUTO_4	0x00	RW	Bit[7]: LGOPT Bit[6]: T7_opt Bit[5:4]: HLGopt Bit[3]: AddVS_opt Bit[2]: Reserved Bit[1:0]: sub_exp_x2
0x3017	AUTO_5	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: RAECG

table 7-1 system control registers (sheet 3 of 14)

address	register name	default value	R/W	description
0x3018	WPT	0x78	RW	Luminance Signal/Histogram High Range for AEC/AGC operation
0x3019	BPT	0x68	RW	Luminance Signal/Histogram Low Range for AEC/AGC operation
0x301A	VPT	0xD4	RW	Fast Mode Large Step Range Thresholds effective only in AEC/AGC fast mode Bit[[7:4]: High threshold Bit[[3:0]: Low threshold
0x301B	YAVG	0x00	R	Luminance Average - this register will auto update. Average luminance is calculated from the B/Gb/Gr/R channel average as follows: B/Gb/Gr/R channel average = (BAVG[7:0] + GbAVG[7:0] + GrAVG[7:0] + RAVG[7:0]) x 0.25
0x301C	AECG_MAX50	0x05	RW	50 Hz Smooth Banding Maximum Steps Control Bit[[7:6]: Reserved Bit[[5:0]: 50 Hz smooth banding maximum steps
0x301D	AECG_MAX60	0x07	RW	60 Hz Smooth Banding Maximum Steps Control Bit[[7:6]: Reserved Bit[[5:0]: 60 Hz smooth banding maximum steps
0x301E	ADDVS	0x00	RW	Extra VSYNC Pulse Width Byte: High Units: Lines
0x301F	ADDVS	0x00	RW	Extra VSYNC Pulse Width Byte: Low Units: lines
0x3020	FRAME_LENGTH_LINES	0x07	RW	Frame Length Byte: High Units: Lines
0x3021	FRAME_LENGTH_LINES	0xBC	RW	Frame Length Byte: Low Units: Lines
0x3022	LINE_LENGTH_PCK	0x0C	RW	Line Length Byte: High Units: System clocks
0x3023	LINE_LENGTH_PCK	0xA0	RW	Line Length Byte: Low Units: System clocks

table 7-1 system control registers (sheet 4 of 14)

address	register name	default value	R/W	description
0x3024	X_ADDR_START	0x00	RW	X Address of the Top Left Corner of the Visible Pixel Byte: High Units: Pixels
0x3025	X_ADDR_START	0x00	RW	X Address of the Top Left Corner of the Visible Pixel Byte: High Units: Pixels
0x3026	Y_ADDR_START	0x00	RW	Y Address of the Top Left Corner of the Visible Pixel Byte: High Units: Lines
0x3027	Y_ADDR_START	0x00	RW	Y Address of the Top Left Corner of the Visible Pixel Byte: High Units: Lines
0x3028	X_ADDR_END	0x0A	RW	X Address of the Bottom Right Corner of the Visible Pixel Byte: High Units: Pixels
0x3029	X_ADDR_END	0x1F	RW	X Address of the Bottom Right Corner of the Visible Pixel Byte: High Units: Pixels
0x302A	Y_ADDR_END	0x07	RW	Y Address of the Bottom Right Corner of the Visible Pixel Byte: High Units: Lines
0x302B	Y_ADDR_END	0x97	RW	Y Address of the Bottom Right Corner of the Visible Pixel Byte: High Units: Lines
0x302C	X_OUTPUT_SIZE	0x0A	RW	Width of Image Data Output from the Sensor Byte: High Units: Pixels
0x302D	X_OUTPUT_SIZE	0x20	RW	Width of Image Data Output from the Sensor Byte: Low Units: Pixels
0x302E	Y_OUTPUT_SIZE	0x07	RW	Height of Image Data Output from the Sensor Byte: High Units: Lines

table 7-1 system control registers (sheet 5 of 14)

address	register name	default value	R/W	description
0x302F	Y_OUTPUT_SIZE	0x98	RW	Height of Image Data Output from the Sensor Byte: low Units: lines
0x3030	FRAME_CNT	0x00	R	Frame Count
0x3031~ 0x3037	RSVD	–	–	Reserved
0x3038	DATR_LMO	0x00	R	Sigma5060 LMO Bit[7:0]
0x3039	DATR_LMO	0x00	R	Sigma5060 LMO Bit[15:8]
0x303A	DATR_LMO	0x00	R	Sigma5060 LMO Bit[19:16]
0x303B~ 0x303C	RSVD	–	–	Reserved
0x303D	DATR_D56	0x00	R	Sigma5060 Register
0x303E	DATR_EF	0x00	R	OTP Register
0x303F~ 0x3047	RSVD	–	–	Reserved
0x3048	R_SIGMA	0x00	RW	R_sigma[7:0]
0x3049	R_SIGMA	0x30	RW	R_sigma[15:8]
0x304A	R_SIGMA	0x20	RW	R_sigma[23:16]
0x304B	R_SIGMA	0x30	RW	R_sigma[31:24]
0x304C	R_SIGMA	0xA7	RW	R_sigma[39:32]
0x304D	R_SIGMA	0x29	RW	R_sigma[47:40]
0x304E	D56COM	0x02	RW	Sigma5060 Clock Control Bit[7]: Clock source select 0: CLK_SCCB 1: DSPCLK Bit[6]: 5060 auto threshold enable Bit[5]: Enable 5060 detection every 4 seconds Bit[4:0]: Clock divider
0x304F	RSVD	–	–	Reserved
0x3050	5060TH	0x00	R	Read 5060 Auto Threshold Value
0x3051~ 0x3057	RSVD	–	–	Reserved

table 7-1 system control registers (sheet 6 of 14)

address	register name	default value	R/W	description
0x3058	LMO_TH1	0x00	RW	Light Meter Output Lowest Value for D5060 Auto Threshold Curve Range from 1 to 7
0x3059	LMO_TH2	0x00	RW	Light Meter Output Highest Value for D5060 Auto Threshold Curve Range from 0x16 to 0x40
0x305A	LMO_K	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Light Meter high threshold. Range from 0x16 to 0x40. Range from 5'b00000 to 5'b11111
0x305B	RSVD	–	–	Reserved
0x305C	BD50ST	0x00	RW	BD50st Byte: High
0x305D	BD50ST	0x55	RW	BD50st Byte: Low
0x305E	BD60ST	0x55	RW	BD60st Byte: High
0x305F	BD60ST	0x01	RW	BD60st Byte: Low
0x3060	BLC	0x44	RW	Sensor BLC Control
0x3061~ 0x3064	RSVD	–	–	Reserved
0x3065	BLC	0x40	RW	Bit[7:6]: Reserved Bit[5:4]: DLY_BR 00: AD_G latch by ADCLK_B 01: AD_G latch by PCLK_B 1x: AD_G latch by PCLK Bit[3:0]: Reserved
0x3066~ 0x3067	RSVD	–	–	Reserved
0x3068	BLC	0x00	RW	Bit[7:5]: Reserved Bit[4:3]: DLY_G 00: AD_G latch by ADCLK_B 01: AD_G latch by PCLK_B 1x: AD_G latch by PCLK Bit[2:0]: Reserved
0x3069	BLC	0x44	RW	Bit[7]: RAD128_inv Bit[6:0]: Reserved
0x306A~ 0x306C	RSVD	–	–	Reserved

table 7-1 system control registers (sheet 7 of 14)

address	register name	default value	R/W	description
0x306D	HSYNST	0x08	RW	HSYNC Start Bit[7:0]: HSYNST[7:0] Units: System clocks
0x306E	HSYNED	0x20	RW	HSYNC End Bit[7:0]: HSYNED[7:0] Units: System clocks
0x306F	HSYNED/HSYNST	0x00	RW	Bit[7:4]: HSYNED[11:8] Bit[3:0]: HSYNST[11:8] Units: System clocks
0x3070	TMC	0x24	RW	RWIN0[7:0]: System Timing and Window Control Bit[7]: RSA1_sel – fixed SA1 end point Bit[6]: Reserved Bit[5]: VREF_opt2 – same number of lines as from array Bit[4]: VREF_opt Bit[3]: Reserved Bit[2]: HREF_opt – same number of pixels as from array Bit[1]: Rcsft_opt Bit[0]: Reserved
0x3071~ 0x30AF	RSVD	–	–	Reserved
0x30B0	IO_CTRL	0xFF	RW	IO_Ctrl0 Enable of Second Camera Interface CY[7:0]
0x30B1	IO_CTRL	0xFF	RW	IO_Ctrl1 Enable of Second Camera Interface Bit[7:6]: Reserved Bit[5]: C_VSYNC Bit[4]: C_STROBE Bit[3]: C_PCLK Bit[2]: C_HREF Bit[1:0]: CY[9:8]
0x30B2	IO_CTRL	0x00	RW	IO_Ctrl2 Enable of Second Camera Interface Bit[7:5]: Reserved Bit[4]: C_FREX Bit[3:0]: R_PAD[3:0]

table 7-1 system control registers (sheet 8 of 14)

address	register name	default value	R/W	description
0x30B3	DSIO	0x00	RW	DSIO[7:0] Bit[7]: Reserved Bit[6]: Rpckinv – invert OP_PCLK Bit[5:4]: Rpcksw – switch PCLK & OP_PCLK Bit[3]: RPCKman 0: Division from ISP subsample 1: Manual control use RPCLKdiv Bit[2]: Reserved Bit[1:0]: RPCLKdiv – PCLK divisor 00: 1 01: 2 10: 4 11: 8
0x30B4	DSIO	0x00	RW	DSIO[15:8] Bit[7:6]: Rtest 00: IMG to PAD 01: Mix signals to PAD 10: Array addr and timing to PAD 11: Array timing to PAD Bit[5:4]: Reserved Bit[3]: RdspblueLat Bit[2]: OTP_TST Bit[1:0]: OTP_SCK_OPT
0x30B5	DSIO	0x10	RW	DSIO[23:16] Bit[7]: RmirrCKINV Bit[6]: Rnewt Bit[5:4]: long_exp_opt[1:0] Bit[3]: VSLatopt Bit[2]: VSLatdly Bit[1]: HDR_en Bit[0]: RHDR_fix gain
0x30B6	TMC	0x00	RW	TMC10 Bit[7:6]: Reserved Bit[5]: Rposispck Bit[4]: RframeENhi Bit[3]: Tri_B Bit[2]: RselNewslp Bit[1:0]: Reserved

table 7-1 system control registers (sheet 9 of 14)

address	register name	default value	R/W	description
0x30B7	TMC	0x80	RW	TMC12 Bit[7]: dis_ISP_rw – disable r/w of regs from ISP/MIPI Bit[6:4]: Reserved Bit[3]: Rgrp_wr_en – enable group write Bit[2]: grp_i2c2uc_wr Bit[1]: Reserved Bit[0]: Ri2c_isp_wrB
0x30B8	RSVD	–	–	Reserved
0x30B9	TMC	0x00	RW	TMC14 Bit[7]: T_RWopt_buf Bit[6:4]: Reserved Bit[3]: RuclatchB Bit[2]: Reserved Bit[1]: RmipiRegrst – enable the mipi sys reset to clear REG Bit[0]: RmipirstEn – enable the reset control from mipi
0x30BA	TMC	0x01	RW	COM4 Bit[7]: RANAdsB Bit[6]: RPLLdsb Bit[5]: RCCP2dsb Bit[4]: RADCsdb Bit[3]: RDSPBLUE_opt1 Bit[2]: RDSPBLUE_opt0 Bit[1]: RDSPdsb Bit[0]: Ri2cPLLrsen
0x30BB	TMC	0x00	RW	REG6C - Drop Frame Type Control Bit[7]: ARBLUE_inv Bit[6]: VFLIP_DropF_EN Bit[5]: QVGA_DropF_EN Bit[4]: fl_DropF_EN Bit[3]: fl_DropF_WR_EN Bit[2:1]: Reserved Bit[0]: y_addr_DropF_dis
0x30BC	TMC	0x00	RW	REG6E Bit[7:6]: Reserved Bit[5:4]: Fmaxopt Bit[3]: Lminopt Bit[2]: RHDRLaec Bit[1]: Reserved Bit[0]: Glatch_opt

table 7-1 system control registers (sheet 10 of 14)

address	register name	default value	R/W	description
0x30BD	R_CLK	0x07	RW	RSCLK[7:0] - System Clock Control Bit[7]: REQ50ph2 – switch sync PH1 and PH2 for analog clock Bit[6]: RPCK delay Bit[5:4]: RPCK – switch source of PCLK 00: CLK_IN 01: CLK_IN inverted 10: PH2 11: PH1 Bit[3:2]: isp_i2c_clk option Bit[1:0]: RPHGAP – gap between PH1 and PH2 00: 1ns + transfer delay 01: 2ns 10: 3ns 11: 0ns
0x30BE	R_CLK	0x00	RW	RACLK[7:0]: Analog Clock Control Bit[7:6]: CLKNrate – PUMP N derating 00: 1:1 01: 1:2 10: 1:4 11: 1:8 Bit[5:4]: CLKPrate – PUMP P derating 00: 1:1 01 1:2 10 1:4 11 1:8 Bit[3]: PUMPxclk – switch between PCLK and CLK_SCCB Bit[2]: RADCFree – ADC clock digital free running Bit[1]: RADCFree – ADC clock free running Bit[0]: RADRFree – array clock free running

table 7-1 system control registers (sheet 11 of 14)

address	register name	default value	R/W	description
0x30BF	R_CLK	0x80	RW	RACLK1[7:0]: Analog Clock Control 1 Bit[7]: RADRinv – invert array clock Bit[6:4]: RADRdly – array clock delay 000: 0ns 001: 2ns 010: 4ns 011: 6ns 100: 8ns 101: 10ns 110: 12ns 111: 14ns Bit[3]: RADAINV – invert analog clock Bit[2:0]: RADADly – analog clock delay 000: 0ns 001: 2ns 010: 4ns 011: 6ns 100: 8ns 101: 10ns 110: 12ns 111: 14ns
0x30C0~ 0x30DF	RSVD	–	–	Reserved
0x30E0	FRS	0x06	RW	Frame / Flash Exposure Control RFRES0 Bit[7]: RflwFX Bit[6]: FRSdly Bit[5]: Fdly10 Bit[4]: FLRS Bit[3]: FnoSA1 Bit[2]: FTXsep Bit[1]: FRSTsep Bit[0]: FTXdly
0x30E1	FRS	0x80	RW	RFRES1 Bit[7:5]: AFTX_D Bit[4]: Reserved Bit[3]: TXHEN Bit[2]: MFRMCLR Bit[1]: Reserved Bit[0]: FRMCLREN
0x30E2	FRS	0x88	RW	RFRES2 Bit[7]: FE1PIN Bit[6]: sel_ADD_all Bit[5:4]: Reserved Bit[3:2]: RFRSlag Bit[1:0]: Fpul

table 7-1 system control registers (sheet 12 of 14)

address	register name	default value	R/W	description
0x30E3	FRS	0x0C	RW	RFRES3 Bit[7:2]: Reserved Bit[1]: Rpre2df Bit[0]: REQopt
0x30E4	FRS	0x07	RW	FECNT
0x30E5	FRS	0x00	RW	FFCNT[7:0]
0x30E6	FRS	0x20	RW	FFCNT[15:0]
0x30E7	FRS	0x80	RW	RFRM Bit[7]: RSTR_FREX_Sync Bit[6]: RSTR_FREX Bit[5]: RSTR_EDGE Bit[4]: RSTR_INV Bit[3:1]: Reserved Bit[0]: STR_EN
0x30E8	FRS	0x00	RW	RSTRB Bit[7]: Start Bit[6]: Invert STROBE Bit[5:4]: Reserved Bit[3:2]: XENON out Bit[1:0]: Strobe out
0x30E9	SA1TMC	0x00	RW	Bit[7]: SWB fix Bit[6]: TX inverse Bit[5]: PCBAR_ALL Bit[4]: Rbsun_fix Bit[3]: Rshift_hi Bit[2]: Rbit1 Bit[1]: RSA1EN_low Bit[0]: Rbsun_dis
0x30EA	TMC	0x00	RW	Bit[7]: Reserved Bit[6]: Rjump_man Bit[5]: Ryoffs_man Bit[4]: Rxoffs_man Bit[3:0]: Reserved
0x30EB	TMC	0x00	RW	Bit[7:4]: isp_h_offset_man[11:8], [7:0] is at 0x307B Bit[3]: Reserved Bit[2:0]: isp_v_offset_man[10:8], [7:0] is at 0x307B
0x30EC~0x30EF	RSVD	–	–	Reserved
0x30F0	FLEX	0x10	RW	REG_TXP: Transmit Precharge Time
0x30F1	FLEX	0x08	RW	REG_FLT: charge floating Point Time

table 7-1 system control registers (sheet 13 of 14)

address	register name	default value	R/W	description
0x30F2	FLEX	0x10	RW	REG_TXT: Transmit Transfer Time
0x30F3	FLEX	0x20	RW	REG_HBK: Hold Black Time
0x30F4	FLEX	0x20	RW	REG_HSG: Hold Signal Time
0x30F5	FLEX	0x40	RW	SA1sft: Shift of SA1 Ending Point
0x30F6	RVSOPT	0xB0	RW	RVSopt Bit[7]: Reserved Bit[6]: Width of VS pulse 0: 1-3 lines 1: Dozens of system clocks Bit[5]: VS start point 0: Frame start 1: Frame end Bit[4]: VS end point 0: frame start 1: frame end Bit[3:2]: VS end line Bit[1:0]: VS start line
0x30F7	AUTO	0x00	RW	Auto Control for AEC/AGC Bit[7]: Rvario Bit[6]: RfixR Bit[5]: Reserved Bit[4]: DropF_EN Bit[3]: EXPNG Bit[2:0]: Ratio[2:0]
0x30F8	IMAGE_TRANSFORM	0x00	RW	Bit[7]: VFLIP Bit[6]: HMIRROR Bit[5]: RISPsubV – enable V subsample in ISP Bit[4]: RISPsub – enable H subsample in ISP Bit[3:2]: VSUB 00: Full 01: 1:2 10: 1:4 11: Reserved Bit[1:0]: HSUB 00: Full 01: 1:2 10: 1:4 11: Reserved Note: H subsample can be implemented in ARRAY and ISP depending on the value of RISPsub Note: V subsample is performed in schematic and ARRAY only

table 7-1 system control registers (sheet 14 of 14)

address	register name	default value	R/W	description
0x30F9	IMAGE_LUM	0x00	RW	Bit[7]: Ravglatch – latch average 0: Use latch sig from ISP 1: Use latch sig from timing in blanking lines Bit[6]: Reserved Bit[5]: SLEEP_opt Bit[4]: SLEEP_NoLatch Bit[3:2]: RSVD Bit[1]: Vertical skip Bit[0]: analog_gain_NODELAY
0x30FA	IMAGE_SYSTEM	0x01	RW	Bit[7]: software_reset 0: Normal open 1: All including I2C is reset to default, then go to stand by Bit[6:3]: Reserved Bit[2]: mask_corrupted_frames 0: Frames are dropped due to change of timing, size etc. 1: No frame drop Bit[1]: grouped_parameter_hold for gain, integration and video timing sig 0: Timing critical signals are written immediately 1: Timing critical signals are written in blanking lines Bit[0]: mode_select 0: Software sleep/standby 1: Streaming
0x30FB~0x30FE	RSVD	–	–	Reserved
0x30FF	GROUP_WR	0x00	RW	Group_write Flag Register

table 7-2 ISP control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3300		0xFF	RW	ISP enable control, 0 - disable, 1- enable (corresponding clock will be stopped if one module is disabled) Bit[7]: wc_en (remove black pixel) Bit[6]: bc_en (remove white pixel) Bit[5]: awb_en Bit[4]: awb_gain_en Bit[3]: dig_gain_en Bit[2]: lenc_en Bit[1]: even_en (disabled if blc_en = 0) Bit[0]: blc_en
0x3301		0xC0	RW	Bit[7]: flip_on Bit[6]: mirror_on Bit[5:4]: bar_sel Bit[1:0]: (0/3 - standard color bar, 1- bar values changed vertically, 2 - bar values changed horizontally) Bit[3]: bar_bl Bit[2]: win_bl Bit[1]: bar_en Bit[0]: vap_en
0x3302		0x00	RW	Bit[7]: awb-man Bit[6]: dig_gain_man_en Bit[5]: awb_bias_en Bit[4]: bias_man_en Bit[3]: sof_sel Bit[2]: g_first Bit[1]: neg_edge Bit[0]: ext_sensor (get data from external sensor)
0x3303		0x00	RW	Bit[7:5]: Reserved Bit[2]: awb_long 0: AWB can get long and short exposure data 1: AWB can only get long exposure data Bit[1:0]: rblue_ctrl Bit[1]: rblue_change_en: enable rblue change at vsync fall edge Bit[0]: rblue_change
0x3304		0x40	RW	Bit[7:0]: digital_gain_manual
0x3305		0x40	RW	Bit[7:0]: bias_manual
0x3306		0x42	RW	Bit[7]: awb_freeze_en Bit[6]: fast_awb Bit[5:0]: awb step size

table 7-2 ISP control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3307		0x04	RW	Range from Unstable to Stable Bit[7:0]: stable_rangeBit[7:0]
0x3308		0x04	RW	Bit[3:0]: r_gain_manBit[11:8]
0x3309		0x00	RW	Bit[7:0]: r_gain_manBit[7:0]
0x330A		0x04	RW	Bit[3:0]: g_gain_manBit[11:8]
0x330B		0x00	RW	Bit[7:0]: g_gain_manBit[7:0]
0x330C		0x04	RW	Bit[3:0]: b_gain_manBit[11:8]
0x330D		0x00	RW	Bit[7:0]: b_gain_manBit[7:0]
0x330E		0x08	RW	Bit[7:0]: stable_rangewBit[7:0] range from stable to unstable stable_tangew > stable_range
0x330F		0x00	RW	Bit[7:0]: AWB_frame_cntBit[7:0] awb gain will change one step every frames until it is stable
0x3310	RSVD	–	–	Reserved
0x3311		0xH00	RW	Bit[7]: wbc_opt_limit 0: Use second big 1: Use neighbor average Bit[6:5]: Border value sel 00: 0x00 01: 0xFF 10: 0x80 11: dup Bit[4]: th_opt (white_pixel only) Bit[3:0]: th_value (white pixel only)
0x3312		0x00	RW	Bit[4]: vap_addopt Bit[3:0]: wbc_th
0x3313		0xF0	RW	Bit[7:4]: vap_avg_enBit[3:0] Bit[3:2]: vap_vskipBit[1:0] 00: Reserved 01: 1:1 10: 1:2 11: 1:4 Bit[1:0]: vap_hskip 00: Reserved 01: 1:1 10: 1:2 11: 1:4
0x3314		0x0A	RW	Horizontal Input Size High Bits Bit[7:5]: Reserved Bit[3:0]: dsp_hsize_inBit[11:8]

table 7-2 ISP control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3315		0x20	RW	Horizontal Input Size Low Bits Bit[7:0]: dsp_hsize_inBit[7:0]
0x3316		0x07	RW	Vertical Input Size Low Bits Bit[7:5]: Reserved Bit[2:0]: dsp_vsize_inBit[10:8]
0x3317		0x98	RW	Vertical Input Size Low Bits Bit[7:0]: dsp_vsize_inBit[7:0]
0x3318		0x00	RW	Bit[7:4]: dsp_vpad_out Bit[3:0]: dsp_hpad_out
0x3319		0x01	RW	Bit[6:4]: start_line Bit[3]: even_man_en: Bit[2]: even_man1_en: evenodd man enable Bit[1]: Evenodd from black line Bit[0]: even_avg: average current blc with previous frame blc
0x331A		0x00	RW	Bit[7:0]: even_man0
0x331B		0x00	RW	Bit[7:0]: even_man1
0x331C		0x00	RW	Bit[7:0]: even_man2
0x331D		0x00	RW	Bit[7:0]: even_man3
0x331E		0x07	RW	Bit[7]: blc_man_en Bit[6]: blc_man1_en: blc man enable Bit[5:4]: bypass_modeBit[1:0]: data bypass mode Bit[3]: Reserved Bit[2]: blc_cut_bline: cut black line enable Bit[1]: average current BLC with previous frame BLC Bit[0]: blc_agc_on: frame agcchange
0x331F		0x02	RW	Bit[7:4]: black_num Bit[3:0]: blc_minnum
0x3320		0xFF	RW	Bit[7:0]: blc_lmt_option, blc threshold
0x3321		0x10	RW	Bit[7]: Reserved Bit[6:0]: blc_thre, evenodd threshold
0x3322		0x10	RW	Bit[7:0]: blc_target_b0, black target level 0
0x3323		0x10	RW	Bit[7:0]: blc_target_b1, black target level 1
0x3324		0x00	RW	blc_man0Bit[9:8]
0x3325		0x00	RW	blc_man0Bit[7:0]

table 7-2 ISP control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x3326		0x00	RW	blc_man1Bit[9:8]
0x3327		0x00	RW	blc_man1Bit[7:0]
0x3328		0x00	RW	blc_man2Bit[9:8]
0x3329		0x00	RW	blc_man2Bit[7:0]
0x332a		0x00	RW	blc_man3Bit[9:8]
0x332b		0x00	RW	blc_man3Bit[7:0]
0x332c		0x00	RW	blc_man4Bit[9:8]
0x332d		0x00	RW	blc_man4Bit[7:0]
0x332e		0x00	RW	blc_man5Bit[9:8]
0x332f		0x00	RW	blc_man5Bit[7:0]
0x3330		0x00	RW	blc_man6Bit[9:8]
0x3331		0x00	RW	blc_man6Bit[7:0]
0x3332		0x00	RW	blc_man7Bit[9:8]
0x3333		0x00	RW	blc_man7Bit[7:0]
0x3334~ 0x33CE	RSVD	–	–	Reserved

table 7-3 CIF control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3200~ 0x3201	RSVD	–	–	Reserved

table 7-3 CIF control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3202	CIF_CTRL2	0x00	R/W	Bit[7]: Reserved Bit[6]: rev_rblue 0: Use ptn_rblue as CIF rblue input 1: Use reverse d ptn_rblue as CIF rblue input Bit[5]: rev_pclk 0: Use ext_snr PCLK as CIF PCLK input 1: Use reversed ext_snr PCLK as CIF pclk input Bit[4]: rev_href 0: Use ext_snr HREF as CIF HREF input 1: Use reversed ext_snr HREF as CIF HREF input Bit[3]: rev_vsync 0: Use ext_snr VSYNC as CIF VSYNC input 1: Use reversed ext_snr VSYNC as CIF VSYNC input Bit[2]: rev_cif_rblue 0: Use CIF output rblue as ISP rblue input 1: Use reversed CIF output rblue as ISP rblue input Bit[1]: rev_ptn_rblue, generate ptn rblue 0: First line of ext_snr is BG line 1: First line of ext_snr is GR line Bit[0]: Reserved

table 7-4 clipping control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3400	CLIP_CTRL0	0xFF	R/W	Bit[7:0]: b_max
0x3401	CLIP_CTRL1	0x00	R/W	Bit[7:0]: b_min
0x3402	CLIP_CTRL2	0xFF	R/W	Bit[7:0]: g_max
0x3403	CLIP_CTRL3	0x00	R/W	Bit[7:0]: g_min
0x3404	CLIP_CTRL4	0xFF	R/W	Bit[7:0]: r_max
0x3405	CLIP_CTRL5	0x00	R/W	Bit[7:0]: r_min

table 7-4 clipping control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3406	CLIP_CTRL6	0x33	R/W	Bit[7:6]: g_minBit[9:8] Bit[5:4]: g_maxBit[9:8] Bit[3:2]: b_minBit[9:8] Bit[1:0]: b_maxBit[9:8]
0x3407	CLIP_CTRL7	0x03	R/W	Bit[7]: Reserved Bit[6]: Bypass clipping 1: Bypass Bit[5]: r_flip Bit[4]: r_mirror Bit[3:2]: r_minBit[9:8] Bit[1:0]: r_maxBit[9:8]

table 7-5 DVP control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3500	DVP_CTRL00	0x80	RW	DVP Control 00 Bit[7:6]: VSYNC select 00: Select vsync_old 01: Select vsync_new 10: Select vsync_three 11: Reserved Bit[5]: pclk_gate_en 1: Gate dvp_pclk when HREF is low Bit[4]: vsync_gate 0: Gate dvp_pclk when VSYNC and pclk_gate_en is high 1: Do not gate dvp_pclk when VSYNC is high Bit[3]: dmy_line_sel 0: Auto generate dummy lines 1: Use first lines as dummy lines Bit[2]: Change polarity of PCLK Bit[1]: Change polarity of HREF Bit[0]: vsync_pol 0: VSYNC = 1 is frame blanking time

table 7-5 DVP control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3501	DVP_CTRL01	0x00	RW	DVP Control 01 Bit[7]: ccir656_en Bit[6]: sync_code_sel 0: Auto generate sync_code 1: Use FS, FE, LS and LE as ccir656 sync_code Bit[5]: Reserved Bit[4]: data_order 0: DVP output dvp_data[11:0] 1: DVP output dvp_data[0:11] Bit[3]: dvp_bit8 0: Swap 2 bit when dvp_h and dvp_l 1: Swap 4 bit Bit[2]: dvp_h 0: Output dvp_data[11:0] 1: Output dvp_data{n:0, 11:n-1} n: 7 or 9 Bit[1]: dvp_l 0: Select dvp_data[11:0] 1: Select dvp_data{n:0, 11:n+1} n: 3 or 1 Bit[0]: ch_flag - write 1 to it to generate flag for HSYNC mode
0x3502	DVP_CTRL02	0xAB	RW	DVP Control 02 Bit[7:0]: CCIR656 sync code for FS
0x3503	DVP_CTRL03	0xB6	RW	DVP Control 03 Bit[7:0]: CCIR656 sync code for FE
0x3504	DVP_CTRL04	0x80	RW	DVP Control 04 Bit[7:0]: CCIR656 sync code for LS
0x3505	DVP_CTRL05	0x9D	RW	DVP Control 05 Bit[7:0]: CCIR656 sync code for LE
0x3506	DVP_CTRL06	0x20	RW	DVP Control 06 Bit[7:6]: Reserved Bit[5]: dvp_en Bit[4]: hsync_en Bit[3:0]: Reserved
0x3507	DVP_CTRL07	0x80	RW	DVP Control 07 Bit[7:1]: vsync_width[7:1] - width of VSYNC when selecting vsync_old and vsync_three Bit[0]: hskip_man_o[0]

table 7-5 DVP control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3508	DVP_CTRL08	0x00	RW	DVP Control 08 Bit[7]: tst_ptn_en Bit[6]: tst_bit8 Bit[5]: tst_bit12 Bit[4]: tst_mode 0: 00, 01, 02, ..., 80, FF 1: 00, 00, 01, 01, ..., FF, FF Bit[3:0]: dmy_line_nu
0x3509	DVP_CTRL09	0x00	RW	DVP Control 09 Bit[7:0]: eof2v_dly[23:16]
0x350A	DVP_CTRL0A	0x01	RW	DVP Control 0A Bit[7:0]: eof2v_dly[15:8]
0x350B	DVP_CTRL0B	0x00	RW	DVP Control 0B Bit[7:0]: eof2v_dly[7:0]
0x350C	DVP_CTRL0C	0x00	RW	DVP Control 0C Bit[7:0]: pad_right
0x350D	DVP_CTRL0D	0x00	RW	DVP Control 0D Bit[7:0]: pad_left
0x350E	DVP_CTRL0E	0x40	RW	DVP Control 0E Bit[7:6]: Reserved Bit[5:4]: vsync_width[9:8] Bit[3:1]: Reserved Bit[0]: skip_man_en_o

table 7-5 DVP control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x350F	DVP_CTRL0F	0x88	RW	DVP Control 0F Bit[7]: eav_first 0: sav_first 1: eav_first Bit[6]: f_sel Bit[5]: f_value Bit[4]: fix_f 0: Auto generate ccir_f 1: Use f_value as ccir_f Bit[3:2]: blk_sel 00: Select 12'h800 and 12'h100 as toggle data x1: Selet 12'h000 as toggle data 10: Select tog0 and tog1 as toggle data Bit[1]: no_sof 0: Reset state machine at SOF 1: Do not reset state machine at SOF Bit[0]: no_clip 0: Clip output data between 10'h004 and 10'h3FB 1: Do not clip output data when in CCIR656 mode
0x3510	DVP_CTRL10	0x09	RW	DVP Control 10 Bit[7:4]: Reserved Bit[3:2]: tog0[11:10] - toggle data0 when line blanking or dummy lines Bit[1:0]: tog1[11:10] - toggle data1 when line blanking or dummy lines
0x3511	DVP_CTRL11	0xAA	RW	DVP Control 11 Bit[7:0]: tog0[9:2] - toggle data0 when line blanking or dummy lines
0x3512	DVP_CTRL12	0x55	RW	DVP Control 12 Bit[7:0]: tog1[9:2] - toggle data1 when line blanking or dummy lines
0x3513	DVP_CTRL13	0x02	RW	DVP Control 13 Bit[7:0]: Reserved
0x3514	DVP_CTRL14	0x00	RW	DVP Control 14 Bit[7:0]: h2v_dly
0x3515	DVP_CTRL15	0x00	RW	DVP Control 15 Bit[7:0]: v2h_dly

table 7-6 MIPI control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3010	PLL_3	0x41	RW	PLL Control Bit[7:6]: Reserved Bit[5]: LaneDiv control bit 0: Use one lane to transfer HS data 1: Use two lanes to transfer HS data Bit[3:0]: Scale_Div control bits
0x3601	MIPI_CTRL01	0x01	RW	Bit[7:1]: Reserved Bit[0]: bit8 1: 8-bit mode
0x3602	MIPI_CTRL02	0x22	RW	Bit[7:3]: Reserved Bit[2]: line_sync_en 1: Send line sync short packet for MIPI Bit[1]: gate_sc_en 1: Gate MIPI clock when no packet Bit[0]: Reserved
0x3603	MIPI_CTRL03	0x49	RW	Bit[7:3]: Reserved Bit[2]: ph_Byte_order for ECC 0: {DI,WC_l,WC_h} 1: {DI,WC_h,WC_l} Bit[1]: ph_bit_order for ECC {DI[7:0],WC[7:0],WC[15:8]} 1: {DI[0:7],WC[0:7],WC[8:15]} Bit[0]: Reserved
0x360C	MIPI_CTRL0C	0x12	RW	Bit[7:6]: VC, virtual channel ID Bit[5:0]: Reserved
0x360E	MIPI_CTRL0E	0x23	RW	Bit[7:6]: Reserved Bit[5:0]: wkup_dly 1 ms wakeup delay/4096 for MIPI ultra low power resume, (SCLK cycle for MARK1)
0x3610	MIPI_CTRL10	0x40	RW	Bit[7:0]: Width_man[7:0]/4, when in JPEG mode user can use width_man to set the width of each image line
0x3611	MIPI_CTRL11	0x0C	RW	Bit[7:5]: width_man[10:8], Width_man_real = width_man × 4 Bit[4:0]: Reserved

table 7-6 MIPI control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x361F	MIPI_CTRL1F	0x0E	RW	Bit[7:0]: PCLK_period PCLK2x period, 1-bit decimal and unit is ns PCLK_PERIOD should be set according to the PLL setting. It affects the MIPI_DPHY timing. The PCLK2x cycles when HS_ZERO_SEL=1, and the unit is ns when HS_ZERO_SEL=0
0x3622	MIPI_CTRL22	0x28	RW	Bit[7:2]: n x UI for t_hs_zero Minimum high speed zero Bit[1:0]: Min_hs_zero_high Unit is PCLK2x cycles when hs_zero_sel = 1 and unit is ns when hs_zero_sel = 0
0x3623	MIPI_CTRL23	0x96	RW	Bit[7:0]: min_hs_zero_low
0x3624	MIPI_CTRL24	0x10	RW	Bit[7:2]: n x UI for t_hs_trail Minimum high speed trail Bit[1:0]: Min_hs_trail_high Unit is PCLK2x cycles when hs_trail_sel = 1 and unit is ns when hs_trail_sel = 0
0x3625	MIPI_CTRL25	0x3C	RW	Bit[7:0]: min_hs_trail_low
0x3626	MIPI_CTRL26	0x01	RW	Bit[7:2]: n x UI for t_clk_zero Minimum clock zero Bit[1:0]: Min_clk_zero_high Unit is PCLK2x cycles when clk_zero_sel = 1 and unit is ns when clk_zero_sel = 0
0x3627	MIPI_CTRL27	0x86	RW	Bit[7:0]: Min_clk_zero_low
0x3628	MIPI_CTRL28	0x00	RW	Bit[7:2]: n x UI for min_clk_pre Minimum clock prepare time Bit[1:0]: Min_clk_pre_high Unit is PCLK2x cycles when clk_prepare_sel = 1 and unit is ns when clk_prepare_sel = 0
0x3629	MIPI_CTRL29	0x32	RW	Bit[7:0]: Min_clk_pre_low
0x362A	MIPI_CTRL2A	0x00	RW	Bit[7:2]: n x UI for max_clk_pre Maximum clock prepare time Bit[1:0]: max_clk_pre_high, unit is ns
0x362B	MIPI_CTRL3B	0x8C	RW	Bit[7:0]: Max_clk_pre_low

table 7-6 MIPI control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x362C	MIPI_CTRL3C	0xD0	RW	Bit[7:2]: n × UI for min_clk_post, minimum clk_post Bit[1:0]: Min_clk_post_high Unit is PCLK2x cycles when clk_post_sel = 1 and unit is ns when clk_post_sel = 0
0x362D	MIPI_CTRL2D	0x56	RW	Bit[7:0]: min_clk_post_low
0x362E	MIPI_CTRL2E	0x00	RW	Bit[7:2]: n × UI for min_clk_trail Bit[1:0]: Min_clk_trail_high Unit is PCLK2x cycles when clk_trail_sel = 1 and unit is ns when clk_trail_sel = 0
0x362F	MIPI_CTRL2F	0x3C	RW	Bit[7:0]: Min_clk_trail_low
0x3630	MIPI_CTRL30	0x00	RW	Bit[7:2]: n × UI for min_lpx_p Bit[1:0]: Min_lpx_p_high, unit is PCLK2x cycles when lpx_p_sel = 1 and unit is ns when lpx_p_sel = 0
0x3631	MIPI_CTRL31	0x32	RW	Bit[7:0]: Min_lpx_p_low
0x3632	MIPI_CTRL32	0x10	RW	Bit[7:2]: n × UI for min_hs_prepare Bit[1:0]: min_hs_prepare_high Unit is PCLK2x cycles when hs_prepare_sel = 1 and unit is ns when hs_prepare_sel = 0
0x3633	MIPI_CTRL33	0x2A	RW	Bit[7:0]: Min_hs_prepare_low
0x3634	MIPI_CTRL34	0x18	RW	Bit[7:2]: n × UI for max_hs_prepare Bit[1:0]: Max_hs_prepare_high Unit is ns
0x3635	MIPI_CTRL35	0x55	RW	Bit[7:0]: Max_hs_prepare_low
0x3636	MIPI_CTRL36	0x00	RW	Bit[7:2]: n × UI for min_hs_exit Bit[1:0]: min_hs_exit_high Unit is PCLK2x cycles when hs_exit_sel = 1 and unit is ns when hs_exit_sel = 0
0x3637	MIPI_CTRL37	0x64	RW	Bit[7:0]: Min_hs_exit_low
0x363D	MIPI_CTRL3D	0x60	RW	Bit[7]: Reserved Bit[6]: JPG_pad_en 1: MIPI_FIFO will pad pixels to meet width_man Bit[5:0]: Reserved

table 7-6 MIPI control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x364C	MIPI_CTRL4C	0x00	RW	Bit[7:3]: Reserved Bit[2]: Ph_ByteUnits_order2 0: ph = {di,wc} for ECC 1: ph = {wc,di} Bit[1:0]: Reserved

Confidential
(For Truly Only)

OV5630

color CMOS QSXGA (5 Megapixel) CameraChip™ sensor with OmniPixel3-HS™ technology

Confidential
(For Truly Only)

8 electrical specifications

table 8-1 absolute maximum ratings

parameter	absolute maximum rating ^a	
stable operating temperature	0°C to +50°C	
operating temperature	-30°C to +70°C	
ambient storage temperature	-40°C to +125°C	
ambient humidity	TBD	
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-C}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)	-0.3V to $V_{DD-IO} + 1V$	
lead-free temperature, surface-mount process	245°C	

- a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device.

table 8-2 DC characteristics ($-30^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$)

symbol	parameter	min	typ	max	unit
supply					
V _{DD-A}	supply voltage (analog)	2.6	2.8	3.1	V
V _{DD-S}	supply voltage (pixel)	2.6	2.8	3.1	V
V _{DD-D}	supply voltage (digital I/O)	1.7 2.6	1.8 2.8	3.1 3.1	V
V _{DD-DO}	supply voltage (digital core) ^a	1.425	1.5	1.575	V
V _{DD-E}	supply voltage (MIPI)	1.425	1.5	1.575	V
I _{DD-A}	active (operating) current 2592 x 1944 @ 10 fps ^b	TBD	60	TBD	mA
I _{DD-S}		TBD	10	TBD	mA
I _{DD-DO}		TBD	90	TBD	mA
I _{DD-A}	active (operating) current 1280 x 720 @ 60 fps ^b	TBD	60	TBD	mA
I _{DD-S}		TBD	10	TBD	mA
I _{DD-DO}		TBD	60	TBD	mA
I _{DDS-SCCB}	standby current	TBD	TBD	TBD	mA
I _{DDS-PWDN}		TBD	TBD	TBD	μA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.5V, DOVDD = 1.8V)					
V _{IL}	input voltage LOW			0.54	V
V _{IH}	input voltage HIGH	1.26			V
C _{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V _{OH}	output voltage HIGH	1.62			V
V _{OL}	output voltage LOW			0.18	V
serial interface inputs					
V _{IL} ^c	SCL and SDA	-0.5	0	0.54	V
V _{IH} ^c	SCL and SDA	1.26	1.8	2.3	V

a. when internal regulator is bypassed

b. using internal regulator for DVDD and short DVDD with EVDD; DOVDD = 2.8V

c. based on DOVDD = 1.8V

table 8-3 AC characteristics ($T_A = 25^\circ\text{C}$, $V_{DD-A} = 2.8\text{V}$)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		30		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	setting time for hardware reset			<1	ms
	setting time for software reset			<1	ms
	setting time for resolution mode change			<1	ms
	setting time for register setting			<300	ms

table 8-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{osc}	frequency (XVCLK)	6	24	27	MHz
t_r , t_f	clock input rise/fall time			5 (10 ^a)	ns

a. if using the internal PLL

OV5630

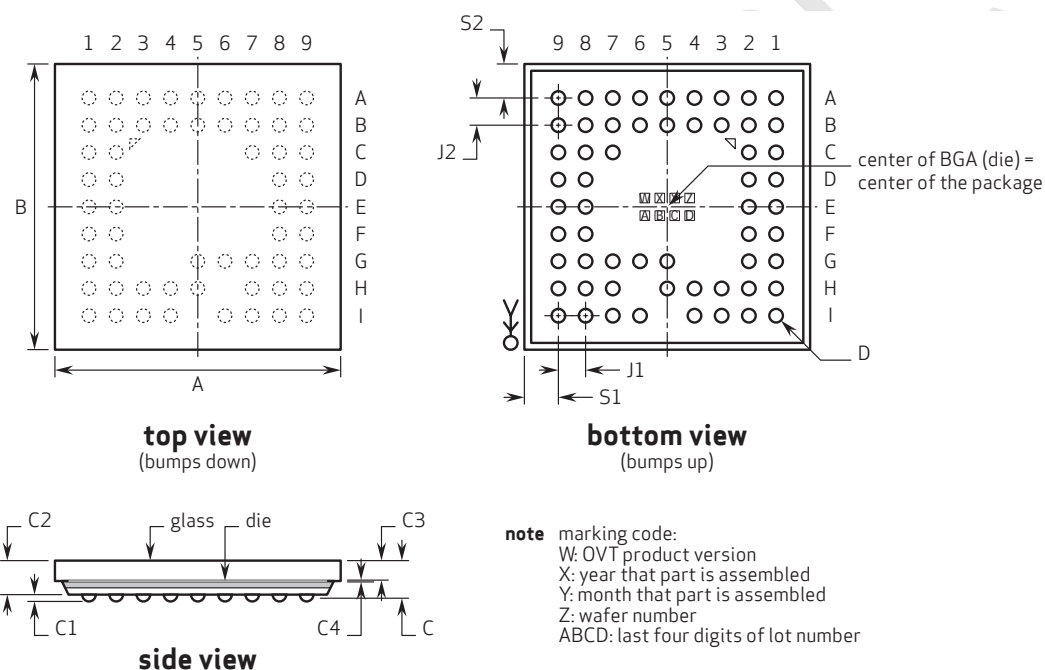
color CMOS QSXGA (5 Megapixel) CameraChip™ sensor with OmniPixel3-HS™ technology

Confidential
(For Truly Only)

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications



5630_CSP_DS_9_1

table 9-1 package dimensions (sheet 1 of 2)

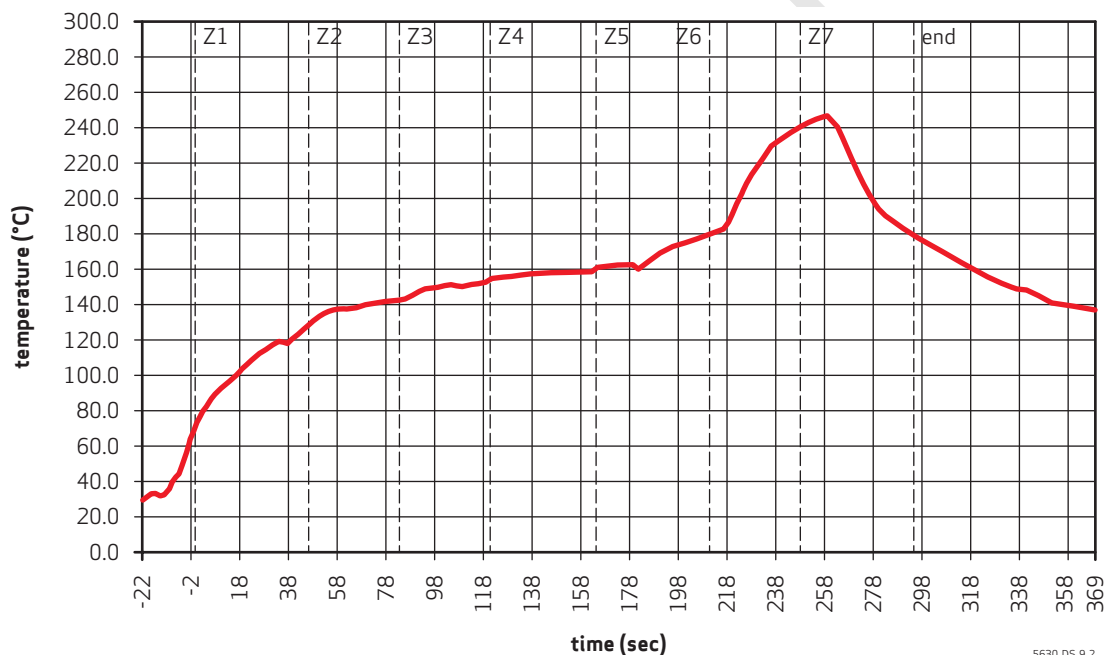
parameter	symbol	min	typ	max	unit
package body dimension x	A	6360	6385	6410	μm
package body dimension y	B	6260	6285	6310	μm
package height	C	825	885	945	μm
ball height	C1	130	160	190	μm
package body thickness	C2	680	725	770	μm
cover glass thickness	C3	390	400	410	μm
airgap between cover glass and sensor	C4	37	41	45	μm
ball diameter	D	270	300	330	μm

table 9-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
total pin count	N		58 (10NC)		
pin count x-axis	N1		9		
pin count y-axis	N2		9		
pins pitch x-axis	J1		650		μm
pins pitch y-axis	J2		630		μm
edge-to-pin center distance analog x	S1	563	593	623	μm
edge-to-pin center distance analog y	S2	593	623	653	μm

9.2 IR reflow specifications

figure 9-2 IR reflow ramp rate requirements



note

The OV5630 uses a lead-free package.

table 9-2 reflow conditions

condition	exposure
average ramp-up rate (30°C to 217°C)	less than 3°C per second
> 100°C	between 330 - 600 seconds
> 150°C	at least 210 seconds
> 217°C	at least 30 seconds (30 ~ 120 seconds)
peak temperature	245°C
cool-down rate (peak to 50°C)	less than 6°C per second
time from 30°C to 245°C	no greater than 390 seconds

OV5630

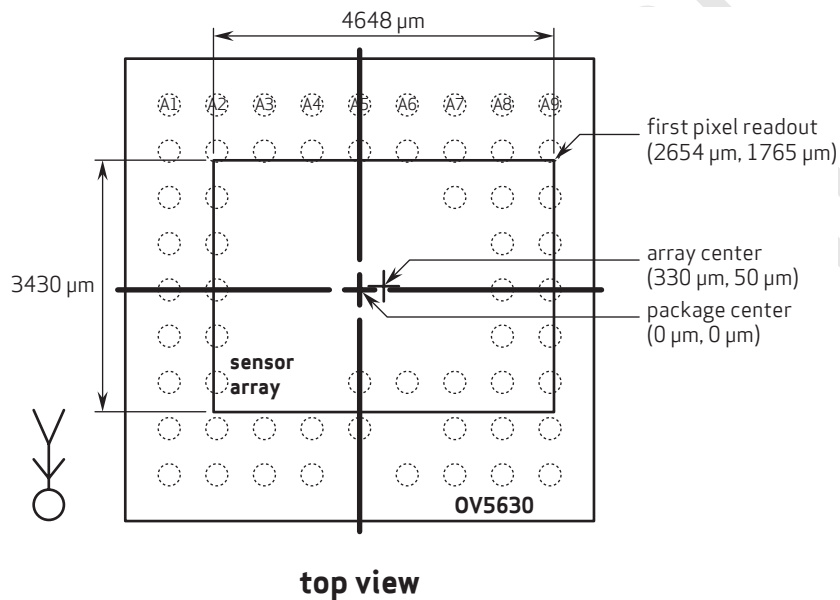
color CMOS QSXGA (5 Megapixel) CameraChip™ sensor with OmniPixel3-HS™ technology

Confidential
(For Truly Only)

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

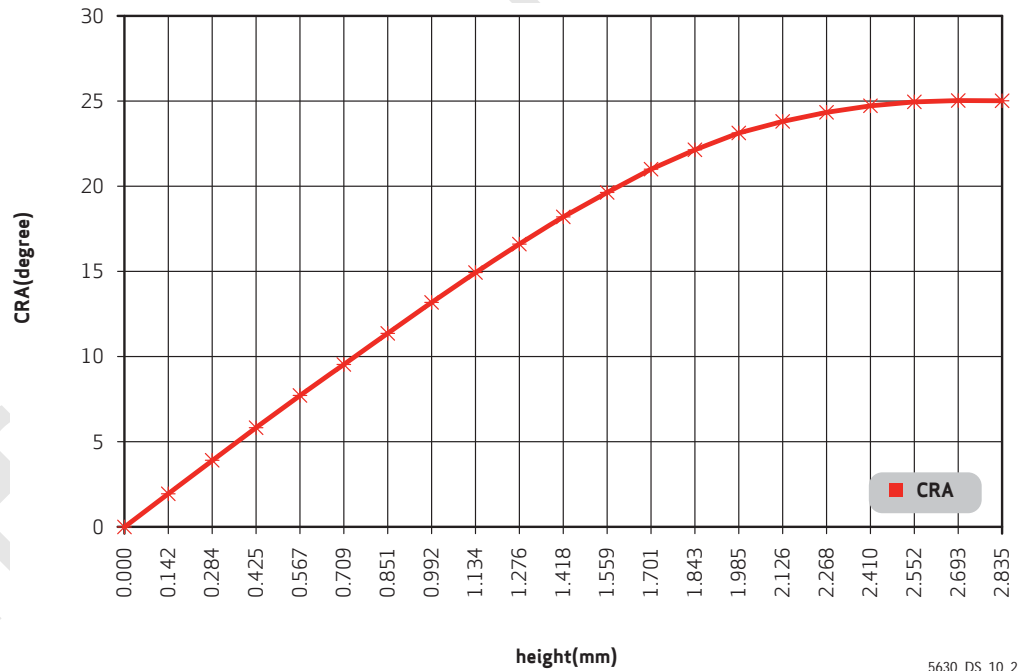
note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A9 oriented down on the PCB.

5630_CSP_DS_10_1

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)



5630_DS_10_2

table 10-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0.00	0.000	0.0
0.05	0.142	1.9
0.10	0.284	3.9
0.15	0.425	5.8
0.20	0.567	7.7
0.25	0.709	9.5
0.30	0.851	11.4
0.35	0.992	13.2
0.40	1.134	14.9
0.45	1.276	16.6

table 10-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.50	1.418	18.2
0.55	1.559	19.7
0.60	1.701	21.0
0.65	1.843	22.2
0.70	1.985	23.1
0.75	2.126	23.9
0.80	2.268	24.4
0.85	2.410	24.8
0.90	2.552	25.0
0.95	2.693	25.1
1.00	2.835	25.0

OV5630

color CMOS QSXGA (5 Megapixel) CameraChip™ sensor with OmniPixel3-HS™ technology

Confidential
(For Truly Only)

revision history

version 1.0 05.09.2008

- initial release

Confidential
(For Truly Only)

OV5630

color CMOS QSXGA (5 Megapixel) CameraChip™ sensor with OmniPixel3-HS™ technology

Confidential
(For Truly Only)

the clear advantage™

OmniVision Technologies, Inc.

UNITED STATES

1341 Orleans Drive
Sunnyvale, CA 94089

tel: +1 408 542 3000

fax: +1 408 542 3001

email: salesamerican@ovt.com

Indianapolis +1 317 297 7240

Philadelphia +1 610 688 3436

UNITED KINGDOM

Hampshire +44 1256 744 610

FINLAND

Nokia +358 3 341 1898

GERMANY

Munich +49 89 63 81 99 88

CHINA

Beijing +86 10 6580 1690

Shanghai +86 21 6105 5100

Shenzhen +86 755 8384 9733

Hong Kong +852 2403 4011

JAPAN

Tokyo +81 3 5765 6321

KOREA

Seoul +82 2 3478 2812

SINGAPORE +65 6562 8250

TAIWAN

Taipei +886 2 2657 9800 -
ext.#100