Data Sheet

S6B33BL

132 RGB Segment & 162 Common Driver For 65,536 Color STN LCD

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Ver. 1.20

System LSI Division
Semiconductor Business
SAMSUNG ELECTRONICS CO., LTD.

(http://www.samsung.com/Products/Semiconductor/DisplayDriverIC)

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INTRODUCTION

S6B33BL is a mid-display-size-compatible driver for liquid crystal dot matrix gray-scale graphic systems. With on-chip CR oscillator circuit, the display-timing signal is generated without being sent from MPU. Also, it is capable of using 8bit/16bit data bus alternatively and operating with 68/80-series MPU in asynchronous. Due to the LCD driving signal (132 RGB X 162 output) corresponding to the display data and the internal bit-map display RAM of 132 ×162 ×16-bit, S6B33BL is capable of operating maximum 132 RGB x 162 dot LCD panels in low-power consumption. Being the segment RGB 3-output, one pixel is 16-bit data and S6B33BL can display max 65,536 colors.

FEATURES

Driver Output

– 132 RGB x 162 COM

Gray Scale Function

– 65,536 color display of R: 32 gray scale, G: 64 gray scale, B: 32 gray scale
– 4,096 color display of R: 16 gray scale, G: 16 gray scale, B: 16 gray scale
– 256 color display of R: 8 gray scale, G: 8 gray scale, B: 4 gray scale

On-chip Display Data RAM

– Capacity: 132 x 16 x 162 = 342.144 kbits

Display Mode

– Normal display mode: Entire duty displaying, Partial display mode: Partial duty displaying
– Area scroll mode: Particular area scrolling, Standby mode: Internal display clocks off

Microprocessor Interface

– 8-bit/16 bit parallel bi-directional interface with 6800-series or 8080-series
– 3/4 Pin SPI (only write operation)

On-chip Low Power Analog Circuit

– On-chip CR oscillator (Internal cap. & external resistor), external clock available
– Voltage converter / Voltage regulator / Voltage follower
– On-chip electronic contrast control (256 steps)

Operating Voltage Range

– VDD = 1.45 to 1.55 [V] (Typical 1.5 [V])
– VDD3 = 1.65 to 3.3[V]
– VIN1 = 2.4 ~ 3.6 [V], VIN1R = 2.4 ~ 3.6 [V]
– Display operating voltage (V1): 2.0 to 4.0 V
– LCD Operating Voltage Range: Max. 20 V

Low Power Consumption

– 600μA Typ. (Refer to DC CHARACTERISTICS (2))

Package Type

COG (Output Pad Pitch Min. 20 μm)

Special Features

– Non-Volatile Memory (MTP) for V1 Calibration

BLOCK DIAGRAM

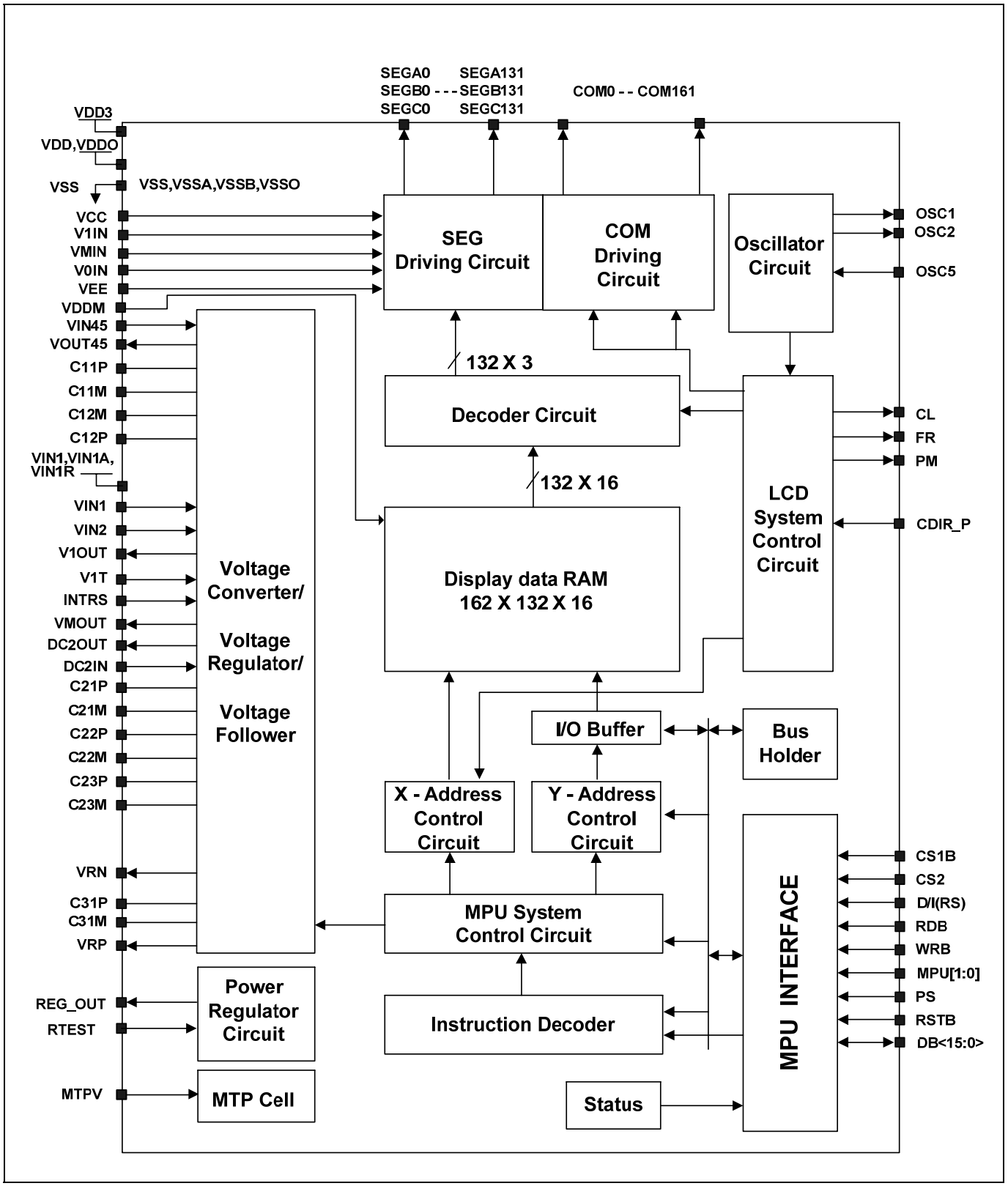


Figure 1. Block Diagram

PAD CONFIGURATION

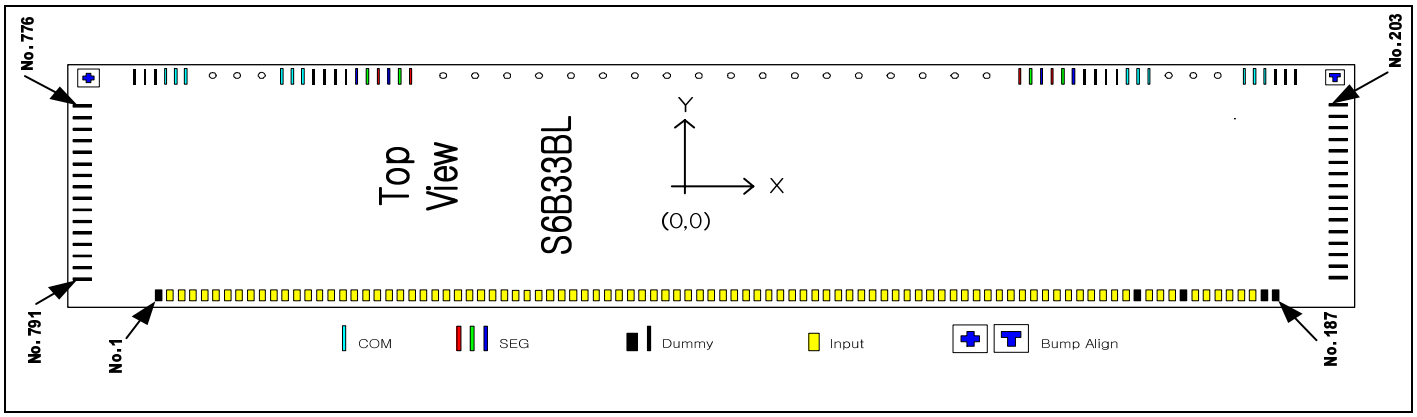


Figure 2. S6B33BL Chip Pad Configuration

Table 1. S6B33BL Pad Dimensions

ITEM	PAD NO.	SIZE		UNIT
		X	Y	
CHIP SIZE (with S/L 80 ㎛)	-	12000	720	㎛
PAD PITCH	1 to 56, 60 to 64, 81 to 186	60		
	187	90		
	57 to 59, 65 to 80	85		
	188 to 791	20		
BUMPED PAD TOP SIZE	1 to 187	40±2	56±2	
	188 to 203, 776 to 791	110±2	11±2	
	204 to 775	11±2	110±2	
BUMPED PAD HEIGHT	In wafer	15(typ)±3		
	In Chip	Under 2		

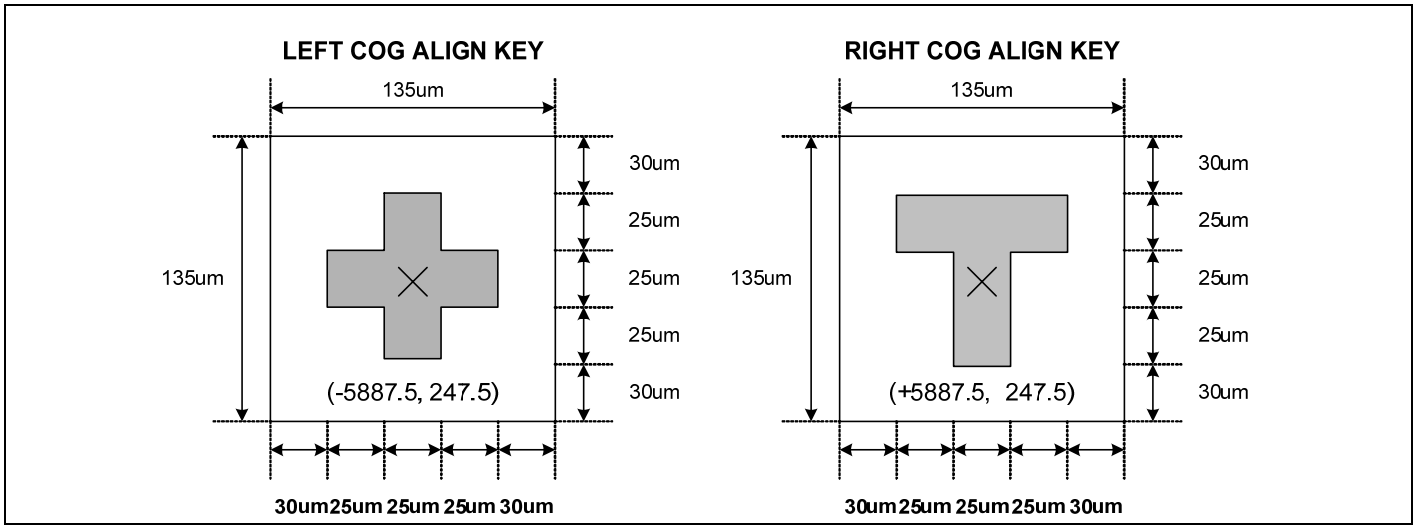


Figure 3. BUMP & COG Align Key Coordinate

PIN CONFIGURATION

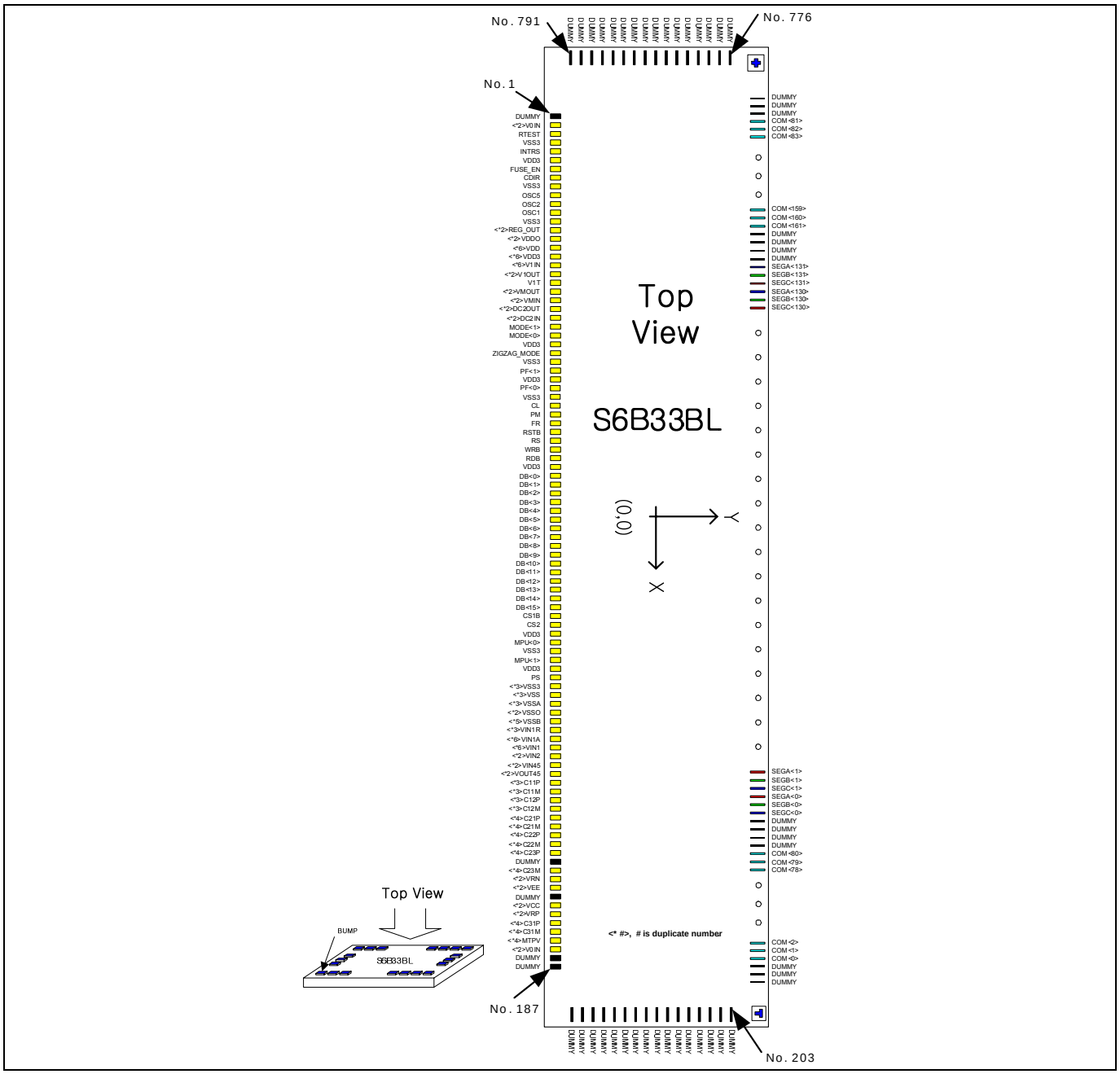


Figure 4. S6B33BL Chip Pin Configuration

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
1	DUMMY	-5832.5	-285	51	ZIGZAG_MODE	-2832.5	-285	101	VSSB	642.5	-285
2	V0IN	-5772.5	-285	52	VSS3	-2772.5	-285	102	VSSB	702.5	-285
3	V0IN	-5712.5	-285	53	PF<1>	-2712.5	-285	103	VSSB	762.5	-285
4	RTEST	-5652.5	-285	54	VDD3	-2652.5	-285	104	VSSB	822.5	-285
5	VSS3	-5592.5	-285	55	PF<0>	-2592.5	-285	105	VIN1R	882.5	-285
6	INTRS	-5532.5	-285	56	VSS3	-2532.5	-285	106	VIN1R	942.5	-285
7	VDD3	-5472.5	-285	57	CL	-2472.5	-285	107	VIN1R	1002.5	-285
8	FUSE_EN	-5412.5	-285	58	PM	-2387.5	-285	108	VIN1A	1062.5	-285
9	CDIR	-5352.5	-285	59	FR	-2302.5	-285	109	VIN1A	1122.5	-285
10	VSS3	-5292.5	-285	60	RSTB	-2217.5	-285	110	VIN1A	1182.5	-285
11	OSC5	-5232.5	-285	61	RS	-2157.5	-285	111	VIN1A	1242.5	-285
12	OSC2	-5172.5	-285	62	WRB	-2097.5	-285	112	VIN1A	1302.5	-285
13	OSC1	-5112.5	-285	63	RDB	-2037.5	-285	113	VIN1A	1362.5	-285
14	VSS3	-5052.5	-285	64	VDD3	-1977.5	-285	114	VIN1	1422.5	-285
15	REG_OUT	-4992.5	-285	65	DB<0>	-1917.5	-285	115	VIN1	1482.5	-285
16	REG_OUT	-4932.5	-285	66	DB<1>	-1832.5	-285	116	VIN1	1542.5	-285
17	VDDO	-4872.5	-285	67	DB<2>	-1747.5	-285	117	VIN1	1602.5	-285
18	VDDO	-4812.5	-285	68	DB<3>	-1662.5	-285	118	VIN1	1662.5	-285
19	VDD	-4752.5	-285	69	DB<4>	-1577.5	-285	119	VIN1	1722.5	-285
20	VDD	-4692.5	-285	70	DB<5>	-1492.5	-285	120	VIN2	1782.5	-285
21	VDD	-4632.5	-285	71	DB<6>	-1407.5	-285	121	VIN2	1842.5	-285
22	VDD	-4572.5	-285	72	DB<7>	-1322.5	-285	122	VIN45	1902.5	-285
23	VDD	-4512.5	-285	73	DB<8>	-1237.5	-285	123	VIN45	1962.5	-285
24	VDD	-4452.5	-285	74	DB<9>	-1152.5	-285	124	VOUT45	2022.5	-285
25	VDD3	-4392.5	-285	75	DB<10>	-1067.5	-285	125	VOUT45	2082.5	-285
26	VDD3	-4332.5	-285	76	DB<11>	-982.5	-285	126	C11P	2142.5	-285
27	VDD3	-4272.5	-285	77	DB<12>	-897.5	-285	127	C11P	2202.5	-285
28	VDD3	-4212.5	-285	78	DB<13>	-812.5	-285	128	C11P	2262.5	-285
29	VDD3	-4152.5	-285	79	DB<14>	-727.5	-285	129	C11M	2322.5	-285
30	VDD3	-4092.5	-285	80	DB<15>	-642.5	-285	130	C11M	2382.5	-285
31	V1IN	-4032.5	-285	81	CS1B	-557.5	-285	131	C11M	2442.5	-285
32	V1IN	-3972.5	-285	82	CS2	-497.5	-285	132	C12P	2502.5	-285
33	V1IN	-3912.5	-285	83	VDD3	-437.5	-285	133	C12P	2562.5	-285
34	V1IN	-3852.5	-285	84	MPU<0>	-377.5	-285	134	C12P	2622.5	-285
35	V1IN	-3792.5	-285	85	VSS3	-317.5	-285	135	C12M	2682.5	-285
36	V1IN	-3732.5	-285	86	MPU<1>	-257.5	-285	136	C12M	2742.5	-285
37	V1OUT	-3672.5	-285	87	VDD3	-197.5	-285	137	C12M	2802.5	-285
38	V1OUT	-3612.5	-285	88	PS	-137.5	-285	138	C21P	2862.5	-285
39	V1T	-3552.5	-285	89	VSS3	-77.5	-285	139	C21P	2922.5	-285
40	VMOUT	-3492.5	-285	90	VSS3	-17.5	-285	140	C21P	2982.5	-285
41	VMOUT	-3432.5	-285	91	VSS3	42.5	-285	141	C21P	3042.5	-285
42	VMIN	-3372.5	-285	92	VSS	102.5	-285	142	C21M	3102.5	-285
43	VMIN	-3312.5	-285	93	VSS	162.5	-285	143	C21M	3162.5	-285
44	DC2OUT	-3252.5	-285	94	VSS	222.5	-285	144	C21M	3222.5	-285
45	DC2OUT	-3192.5	-285	95	VSSA	282.5	-285	145	C21M	3282.5	-285
46	DC2IN	-3132.5	-285	96	VSSA	342.5	-285	146	C22P	3342.5	-285
47	DC2IN	-3072.5	-285	97	VSSA	402.5	-285	147	C22P	3402.5	-285
48	MODE<1>	-3012.5	-285	98	VSSO	462.5	-285	148	C22P	3462.5	-285
49	MODE<0>	-2952.5	-285	99	VSSO	522.5	-285	149	C22P	3522.5	-285
50	VDD3	-2892.5	-285	100	VSSB	582.5	-285	150	C22M	3582.5	-285

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
151	C22M	3642.5	-285	201	DUMMY	5898	83	251	COM<44>	4770	258
152	C22M	3702.5	-285	202	DUMMY	5898	103	252	COM<45>	4750	258
153	C22M	3762.5	-285	203	DUMMY	5898	123	253	COM<46>	4730	258
154	C23P	3822.5	-285	204	DUMMY	5710	258	254	COM<47>	4710	258
155	C23P	3882.5	-285	205	DUMMY	5690	258	255	COM<48>	4690	258
156	C23P	3942.5	-285	206	DUMMY	5670	258	256	COM<49>	4670	258
157	C23P	4002.5	-285	207	COM<0>	5650	258	257	COM<50>	4650	258
158	DUMMY	4062.5	-285	208	COM<1>	5630	258	258	COM<51>	4630	258
159	C23M	4122.5	-285	209	COM<2>	5610	258	259	COM<52>	4610	258
160	C23M	4182.5	-285	210	COM<3>	5590	258	260	COM<53>	4590	258
161	C23M	4242.5	-285	211	COM<4>	5570	258	261	COM<54>	4570	258
162	C23M	4302.5	-285	212	COM<5>	5550	258	262	COM<55>	4550	258
163	VRN	4362.5	-285	213	COM<6>	5530	258	263	COM<56>	4530	258
164	VRN	4422.5	-285	214	COM<7>	5510	258	264	COM<57>	4510	258
165	VEE	4482.5	-285	215	COM<8>	5490	258	265	COM<58>	4490	258
166	VEE	4542.5	-285	216	COM<9>	5470	258	266	COM<59>	4470	258
167	DUMMY	4602.5	-285	217	COM<10>	5450	258	267	COM<60>	4450	258
168	VCC	4662.5	-285	218	COM<11>	5430	258	268	COM<61>	4430	258
169	VCC	4722.5	-285	219	COM<12>	5410	258	269	COM<62>	4410	258
170	VRP	4782.5	-285	220	COM<13>	5390	258	270	COM<63>	4390	258
171	VRP	4842.5	-285	221	COM<14>	5370	258	271	COM<64>	4370	258
172	C31P	4902.5	-285	222	COM<15>	5350	258	272	COM<65>	4350	258
173	C31P	4962.5	-285	223	COM<16>	5330	258	273	COM<66>	4330	258
174	C31P	5022.5	-285	224	COM<17>	5310	258	274	COM<67>	4310	258
175	C31P	5082.5	-285	225	COM<18>	5290	258	275	COM<68>	4290	258
176	C31M	5142.5	-285	226	COM<19>	5270	258	276	COM<69>	4270	258
177	C31M	5202.5	-285	227	COM<20>	5250	258	277	COM<70>	4250	258
178	C31M	5262.5	-285	228	COM<21>	5230	258	278	COM<71>	4230	258
179	C31M	5322.5	-285	229	COM<22>	5210	258	279	COM<72>	4210	258
180	MTPV	5382.5	-285	230	COM<23>	5190	258	280	COM<73>	4190	258
181	MTPV	5442.5	-285	231	COM<24>	5170	258	281	COM<74>	4170	258
182	MTPV	5502.5	-285	232	COM<25>	5150	258	282	COM<75>	4150	258
183	MTPV	5562.5	-285	233	COM<26>	5130	258	283	COM<76>	4130	258
184	V0IN	5622.5	-285	234	COM<27>	5110	258	284	COM<77>	4110	258
185	V0IN	5682.5	-285	235	COM<28>	5090	258	285	COM<78>	4090	258
186	DUMMY	5742.5	-285	236	COM<29>	5070	258	286	COM<79>	4070	258
187	DUMMY	5832.5	-285	237	COM<30>	5050	258	287	COM<80>	4050	258
188	DUMMY	5898	-177	238	COM<31>	5030	258	288	DUMMY	4030	258
189	DUMMY	5898	-157	239	COM<32>	5010	258	289	DUMMY	4010	258
190	DUMMY	5898	-137	240	COM<33>	4990	258	290	DUMMY	3990	258
191	DUMMY	5898	-117	241	COM<34>	4970	258	291	DUMMY	3970	258
192	DUMMY	5898	-97	242	COM<35>	4950	258	292	SEGC<0>	3950	258
193	DUMMY	5898	-77	243	COM<36>	4930	258	293	SEGB<0>	3930	258
194	DUMMY	5898	-57	244	COM<37>	4910	258	294	SEGA<0>	3910	258
195	DUMMY	5898	-37	245	COM<38>	4890	258	295	SEGC<1>	3890	258
196	DUMMY	5898	-17	246	COM<39>	4870	258	296	SEGB<1>	3870	258
197	DUMMY	5898	3	247	COM<40>	4850	258	297	SEGA<1>	3850	258
198	DUMMY	5898	23	248	COM<41>	4830	258	298	SEGC<2>	3830	258
199	DUMMY	5898	43	249	COM<42>	4810	258	299	SEGB<2>	3810	258
200	DUMMY	5898	63	250	COM<43>	4790	258	300	SEGA<2>	3790	258

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
301	SEGC<3>	3770	258	351	SEGA<19>	2770	258	401	SEGB<36>	1770	258
302	SEGB<3>	3750	258	352	SEGC<20>	2750	258	402	SEGA<36>	1750	258
303	SEGA<3>	3730	258	353	SEGB<20>	2730	258	403	SEGC<37>	1730	258
304	SEGC<4>	3710	258	354	SEGA<20>	2710	258	404	SEGB<37>	1710	258
305	SEGB<4>	3690	258	355	SEGC<21>	2690	258	405	SEGA<37>	1690	258
306	SEGA<4>	3670	258	356	SEGB<21>	2670	258	406	SEGC<38>	1670	258
307	SEGC<5>	3650	258	357	SEGA<21>	2650	258	407	SEGB<38>	1650	258
308	SEGB<5>	3630	258	358	SEGC<22>	2630	258	408	SEGA<38>	1630	258
309	SEGA<5>	3610	258	359	SEGB<22>	2610	258	409	SEGC<39>	1610	258
310	SEGC<6>	3590	258	360	SEGA<22>	2590	258	410	SEGB<39>	1590	258
311	SEGB<6>	3570	258	361	SEGC<23>	2570	258	411	SEGA<39>	1570	258
312	SEGA<6>	3550	258	362	SEGB<23>	2550	258	412	SEGC<40>	1550	258
313	SEGC<7>	3530	258	363	SEGA<23>	2530	258	413	SEGB<40>	1530	258
314	SEGB<7>	3510	258	364	SEGC<24>	2510	258	414	SEGA<40>	1510	258
315	SEGA<7>	3490	258	365	SEGB<24>	2490	258	415	SEGC<41>	1490	258
316	SEGC<8>	3470	258	366	SEGA<24>	2470	258	416	SEGB<41>	1470	258
317	SEGB<8>	3450	258	367	SEGC<25>	2450	258	417	SEGA<41>	1450	258
318	SEGA<8>	3430	258	368	SEGB<25>	2430	258	418	SEGC<42>	1430	258
319	SEGC<9>	3410	258	369	SEGA<25>	2410	258	419	SEGB<42>	1410	258
320	SEGB<9>	3390	258	370	SEGC<26>	2390	258	420	SEGA<42>	1390	258
321	SEGA<9>	3370	258	371	SEGB<26>	2370	258	421	SEGC<43>	1370	258
322	SEGC<10>	3350	258	372	SEGA<26>	2350	258	422	SEGB<43>	1350	258
323	SEGB<10>	3330	258	373	SEGC<27>	2330	258	423	SEGA<43>	1330	258
324	SEGA<10>	3310	258	374	SEGB<27>	2310	258	424	SEGC<44>	1310	258
325	SEGC<11>	3290	258	375	SEGA<27>	2290	258	425	SEGB<44>	1290	258
326	SEGB<11>	3270	258	376	SEGC<28>	2270	258	426	SEGA<44>	1270	258
327	SEGA<11>	3250	258	377	SEGB<28>	2250	258	427	SEGC<45>	1250	258
328	SEGC<12>	3230	258	378	SEGA<28>	2230	258	428	SEGB<45>	1230	258
329	SEGB<12>	3210	258	379	SEGC<29>	2210	258	429	SEGA<45>	1210	258
330	SEGA<12>	3190	258	380	SEGB<29>	2190	258	430	SEGC<46>	1190	258
331	SEGC<13>	3170	258	381	SEGA<29>	2170	258	431	SEGB<46>	1170	258
332	SEGB<13>	3150	258	382	SEGC<30>	2150	258	432	SEGA<46>	1150	258
333	SEGA<13>	3130	258	383	SEGB<30>	2130	258	433	SEGC<47>	1130	258
334	SEGC<14>	3110	258	384	SEGA<30>	2110	258	434	SEGB<47>	1110	258
335	SEGB<14>	3090	258	385	SEGC<31>	2090	258	435	SEGA<47>	1090	258
336	SEGA<14>	3070	258	386	SEGB<31>	2070	258	436	SEGC<48>	1070	258
337	SEGC<15>	3050	258	387	SEGA<31>	2050	258	437	SEGB<48>	1050	258
338	SEGB<15>	3030	258	388	SEGC<32>	2030	258	438	SEGA<48>	1030	258
339	SEGA<15>	3010	258	389	SEGB<32>	2010	258	439	SEGC<49>	1010	258
340	SEGC<16>	2990	258	390	SEGA<32>	1990	258	440	SEGB<49>	990	258
341	SEGB<16>	2970	258	391	SEGC<33>	1970	258	441	SEGA<49>	970	258
342	SEGA<16>	2950	258	392	SEGB<33>	1950	258	442	SEGC<50>	950	258
343	SEGC<17>	2930	258	393	SEGA<33>	1930	258	443	SEGB<50>	930	258
344	SEGB<17>	2910	258	394	SEGC<34>	1910	258	444	SEGA<50>	910	258
345	SEGA<17>	2890	258	395	SEGB<34>	1890	258	445	SEGC<51>	890	258
346	SEGC<18>	2870	258	396	SEGA<34>	1870	258	446	SEGB<51>	870	258
347	SEGB<18>	2850	258	397	SEGC<35>	1850	258	447	SEGA<51>	850	258
348	SEGA<18>	2830	258	398	SEGB<35>	1830	258	448	SEGC<52>	830	258
349	SEGC<19>	2810	258	399	SEGA<35>	1810	258	449	SEGB<52>	810	258
350	SEGB<19>	2790	258	400	SEGC<36>	1790	258	450	SEGA<52>	790	258

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
451	SEGC<53>	770	258	501	SEGA<69>	-230	258	551	SEGB<86>	-1230	258
452	SEGB<53>	750	258	502	SEGC<70>	-250	258	552	SEGA<86>	-1250	258
453	SEGA<53>	730	258	503	SEGB<70>	-270	258	553	SEGC<87>	-1270	258
454	SEGC<54>	710	258	504	SEGA<70>	-290	258	554	SEGB<87>	-1290	258
455	SEGB<54>	690	258	505	SEGC<71>	-310	258	555	SEGA<87>	-1310	258
456	SEGA<54>	670	258	506	SEGB<71>	-330	258	556	SEGC<88>	-1330	258
457	SEGC<55>	650	258	507	SEGA<71>	-350	258	557	SEGB<88>	-1350	258
458	SEGB<55>	630	258	508	SEGC<72>	-370	258	558	SEGA<88>	-1370	258
459	SEGA<55>	610	258	509	SEGB<72>	-390	258	559	SEGC<89>	-1390	258
460	SEGC<56>	590	258	510	SEGA<72>	-410	258	560	SEGB<89>	-1410	258
461	SEGB<56>	570	258	511	SEGC<73>	-430	258	561	SEGA<89>	-1430	258
462	SEGA<56>	550	258	512	SEGB<73>	-450	258	562	SEGC<90>	-1450	258
463	SEGC<57>	530	258	513	SEGA<73>	-470	258	563	SEGB<90>	-1470	258
464	SEGB<57>	510	258	514	SEGC<74>	-490	258	564	SEGA<90>	-1490	258
465	SEGA<57>	490	258	515	SEGB<74>	-510	258	565	SEGC<91>	-1510	258
466	SEGC<58>	470	258	516	SEGA<74>	-530	258	566	SEGB<91>	-1530	258
467	SEGB<58>	450	258	517	SEGC<75>	-550	258	567	SEGA<91>	-1550	258
468	SEGA<58>	430	258	518	SEGB<75>	-570	258	568	SEGC<92>	-1570	258
469	SEGC<59>	410	258	519	SEGA<75>	-590	258	569	SEGB<92>	-1590	258
470	SEGB<59>	390	258	520	SEGC<76>	-610	258	570	SEGA<92>	-1610	258
471	SEGA<59>	370	258	521	SEGB<76>	-630	258	571	SEGC<93>	-1630	258
472	SEGC<60>	350	258	522	SEGA<76>	-650	258	572	SEGB<93>	-1650	258
473	SEGB<60>	330	258	523	SEGC<77>	-670	258	573	SEGA<93>	-1670	258
474	SEGA<60>	310	258	524	SEGB<77>	-690	258	574	SEGC<94>	-1690	258
475	SEGC<61>	290	258	525	SEGA<77>	-710	258	575	SEGB<94>	-1710	258
476	SEGB<61>	270	258	526	SEGC<78>	-730	258	576	SEGA<94>	-1730	258
477	SEGA<61>	250	258	527	SEGB<78>	-750	258	577	SEGC<95>	-1750	258
478	SEGC<62>	230	258	528	SEGA<78>	-770	258	578	SEGB<95>	-1770	258
479	SEGB<62>	210	258	529	SEGC<79>	-790	258	579	SEGA<95>	-1790	258
480	SEGA<62>	190	258	530	SEGB<79>	-810	258	580	SEGC<96>	-1810	258
481	SEGC<63>	170	258	531	SEGA<79>	-830	258	581	SEGB<96>	-1830	258
482	SEGB<63>	150	258	532	SEGC<80>	-850	258	582	SEGA<96>	-1850	258
483	SEGA<63>	130	258	533	SEGB<80>	-870	258	583	SEGC<97>	-1870	258
484	SEGC<64>	110	258	534	SEGA<80>	-890	258	584	SEGB<97>	-1890	258
485	SEGB<64>	90	258	535	SEGC<81>	-910	258	585	SEGA<97>	-1910	258
486	SEGA<64>	70	258	536	SEGB<81>	-930	258	586	SEGC<98>	-1930	258
487	SEGC<65>	50	258	537	SEGA<81>	-950	258	587	SEGB<98>	-1950	258
488	SEGB<65>	30	258	538	SEGC<82>	-970	258	588	SEGA<98>	-1970	258
489	SEGA<65>	10	258	539	SEGB<82>	-990	258	589	SEGC<99>	-1990	258
490	SEGC<66>	-10	258	540	SEGA<82>	-1010	258	590	SEGB<99>	-2010	258
491	SEGB<66>	-30	258	541	SEGC<83>	-1030	258	591	SEGA<99>	-2030	258
492	SEGA<66>	-50	258	542	SEGB<83>	-1050	258	592	SEGC<100>	-2050	258
493	SEGC<67>	-70	258	543	SEGA<83>	-1070	258	593	SEGB<100>	-2070	258
494	SEGB<67>	-90	258	544	SEGC<84>	-1090	258	594	SEGA<100>	-2090	258
495	SEGA<67>	-110	258	545	SEGB<84>	-1110	258	595	SEGC<101>	-2110	258
496	SEGC<68>	-130	258	546	SEGA<84>	-1130	258	596	SEGB<101>	-2130	258
497	SEGB<68>	-150	258	547	SEGC<85>	-1150	258	597	SEGA<101>	-2150	258
498	SEGA<68>	-170	258	548	SEGB<85>	-1170	258	598	SEGC<102>	-2170	258
499	SEGC<69>	-190	258	549	SEGA<85>	-1190	258	599	SEGB<102>	-2190	258
500	SEGB<69>	-210	258	550	SEGC<86>	-1210	258	600	SEGA<102>	-2210	258

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
601	SEGC<103>	-2230	258	651	SEGA<119>	-3230	258	701	COM<152>	-4230	258
602	SEGB<103>	-2250	258	652	SEGC<120>	-3250	258	702	COM<151>	-4250	258
603	SEGA<103>	-2270	258	653	SEGB<120>	-3270	258	703	COM<150>	-4270	258
604	SEGC<104>	-2290	258	654	SEGA<120>	-3290	258	704	COM<149>	-4290	258
605	SEGB<104>	-2310	258	655	SEGC<121>	-3310	258	705	COM<148>	-4310	258
606	SEGA<104>	-2330	258	656	SEGB<121>	-3330	258	706	COM<147>	-4330	258
607	SEGC<105>	-2350	258	657	SEGA<121>	-3350	258	707	COM<146>	-4350	258
608	SEGB<105>	-2370	258	658	SEGC<122>	-3370	258	708	COM<145>	-4370	258
609	SEGA<105>	-2390	258	659	SEGB<122>	-3390	258	709	COM<144>	-4390	258
610	SEGC<106>	-2410	258	660	SEGA<122>	-3410	258	710	COM<143>	-4410	258
611	SEGB<106>	-2430	258	661	SEGC<123>	-3430	258	711	COM<142>	-4430	258
612	SEGA<106>	-2450	258	662	SEGB<123>	-3450	258	712	COM<141>	-4450	258
613	SEGC<107>	-2470	258	663	SEGA<123>	-3470	258	713	COM<140>	-4470	258
614	SEGB<107>	-2490	258	664	SEGC<124>	-3490	258	714	COM<139>	-4490	258
615	SEGA<107>	-2510	258	665	SEGB<124>	-3510	258	715	COM<138>	-4510	258
616	SEGC<108>	-2530	258	666	SEGA<124>	-3530	258	716	COM<137>	-4530	258
617	SEGB<108>	-2550	258	667	SEGC<125>	-3550	258	717	COM<136>	-4550	258
618	SEGA<108>	-2570	258	668	SEGB<125>	-3570	258	718	COM<135>	-4570	258
619	SEGC<109>	-2590	258	669	SEGA<125>	-3590	258	719	COM<134>	-4590	258
620	SEGB<109>	-2610	258	670	SEGC<126>	-3610	258	720	COM<133>	-4610	258
621	SEGA<109>	-2630	258	671	SEGB<126>	-3630	258	721	COM<132>	-4630	258
622	SEGC<110>	-2650	258	672	SEGA<126>	-3650	258	722	COM<131>	-4650	258
623	SEGB<110>	-2670	258	673	SEGC<127>	-3670	258	723	COM<130>	-4670	258
624	SEGA<110>	-2690	258	674	SEGB<127>	-3690	258	724	COM<129>	-4690	258
625	SEGC<111>	-2710	258	675	SEGA<127>	-3710	258	725	COM<128>	-4710	258
626	SEGB<111>	-2730	258	676	SEGC<128>	-3730	258	726	COM<127>	-4730	258
627	SEGA<111>	-2750	258	677	SEGB<128>	-3750	258	727	COM<126>	-4750	258
628	SEGC<112>	-2770	258	678	SEGA<128>	-3770	258	728	COM<125>	-4770	258
629	SEGB<112>	-2790	258	679	SEGC<129>	-3790	258	729	COM<124>	-4790	258
630	SEGA<112>	-2810	258	680	SEGB<129>	-3810	258	730	COM<123>	-4810	258
631	SEGC<113>	-2830	258	681	SEGA<129>	-3830	258	731	COM<122>	-4830	258
632	SEGB<113>	-2850	258	682	SEGC<130>	-3850	258	732	COM<121>	-4850	258
633	SEGA<113>	-2870	258	683	SEGB<130>	-3870	258	733	COM<120>	-4870	258
634	SEGC<114>	-2890	258	684	SEGA<130>	-3890	258	734	COM<119>	-4890	258
635	SEGB<114>	-2910	258	685	SEGC<131>	-3910	258	735	COM<118>	-4910	258
636	SEGA<114>	-2930	258	686	SEGB<131>	-3930	258	736	COM<117>	-4930	258
637	SEGC<115>	-2950	258	687	SEGA<131>	-3950	258	737	COM<116>	-4950	258
638	SEGB<115>	-2970	258	688	DUMMY	-3970	258	738	COM<115>	-4970	258
639	SEGA<115>	-2990	258	689	DUMMY	-3990	258	739	COM<114>	-4990	258
640	SEGC<116>	-3010	258	690	DUMMY	-4010	258	740	COM<113>	-5010	258
641	SEGB<116>	-3030	258	691	DUMMY	-4030	258	741	COM<112>	-5030	258
642	SEGA<116>	-3050	258	692	COM<161>	-4050	258	742	COM<111>	-5050	258
643	SEGC<117>	-3070	258	693	COM<160>	-4070	258	743	COM<110>	-5070	258
644	SEGB<117>	-3090	258	694	COM<159>	-4090	258	744	COM<109>	-5090	258
645	SEGA<117>	-3110	258	695	COM<158>	-4110	258	745	COM<108>	-5110	258
646	SEGC<118>	-3130	258	696	COM<157>	-4130	258	746	COM<107>	-5130	258
647	SEGB<118>	-3150	258	697	COM<156>	-4150	258	747	COM<106>	-5150	258
648	SEGA<118>	-3170	258	698	COM<155>	-4170	258	748	COM<105>	-5170	258
649	SEGC<119>	-3190	258	699	COM<154>	-4190	258	749	COM<104>	-5190	258
650	SEGB<119>	-3210	258	700	COM<153>	-4210	258	750	COM<103>	-5210	258

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	NAME	X	Y
751	COM<102>	-5230	258
752	COM<101>	-5250	258
753	COM<100>	-5270	258
754	COM<99>	-5290	258
755	COM<98>	-5310	258
756	COM<97>	-5330	258
757	COM<96>	-5350	258
758	COM<95>	-5370	258
759	COM<94>	-5390	258
760	COM<93>	-5410	258
761	COM<92>	-5430	258
762	COM<91>	-5450	258
763	COM<90>	-5470	258
764	COM<89>	-5490	258
765	COM<88>	-5510	258
766	COM<87>	-5530	258
767	COM<86>	-5550	258
768	COM<85>	-5570	258
769	COM<84>	-5590	258
770	COM<83>	-5610	258
771	COM<82>	-5630	258
772	COM<81>	-5650	258
773	DUMMY	-5670	258
774	DUMMY	-5690	258
775	DUMMY	-5710	258
776	DUMMY	-5898	123
777	DUMMY	-5898	103
778	DUMMY	-5898	83
779	DUMMY	-5898	63
780	DUMMY	-5898	43
781	DUMMY	-5898	23
782	DUMMY	-5898	3
783	DUMMY	-5898	-17
784	DUMMY	-5898	-37
785	DUMMY	-5898	-57
786	DUMMY	-5898	-77
787	DUMMY	-5898	-97
788	DUMMY	-5898	-117
789	DUMMY	-5898	-137
790	DUMMY	-5898	-157
791	DUMMY	-5898	-177

PIN DESCRIPTION

Table 3. Power Supply Pins

Name	I/O	Description
VDD3	Supply	I/O power supply. VDD3 is higher than VDD(including VDD).
VDD	Supply	Regulated power supply input pin for internal digital block & Display Data RAM. This pin is connected to REG_OUT outside the chip with stabilization capacitor.
VDDO	Supply	Internal oscillator power supply This pin is connected to VDD.
VSS VSSO VSSA VSSB	GND	Ground
VSS3	GND	I/O Ground
V1IN / V1OUT	I / O	LCD segment high selected driving voltage input / output pin
VMIN / VMOUT	I / O	LCD common non-selected driving voltage input / output pin
V0IN	I	LCD segment low selected driving voltage input pin
VCC / VRP	I / O	LCD common high selected driving voltage input / output pin
VEE / VRN	I / O	LCD common low selected driving voltage input / output pin The relationship between VCC, V1, VM, V0 and VEE: VCC > V1 > VM > V0(=VSS) > VEE (V1 – VM = VM – V0, VCC –VM = VM – VEE)
VIN1R	Supply	Internal regulator power supply. This pin is connected to VIN1.
VIN1/VIN1A	I	Power supply for 1’st booster circuit and VM Amp
VIN2	I	Power supply for DC2-Amp. Recommend to connect this pin to VOUT45.
VOUT45	O	1’st booster output pin
VIN45	I	Power supply for V1. Connect to VOUT45 or VIN1. Recommend to connect this pin to VOUT45
C11P C11M C12P C12M	O	External capacitor connection pins used for 1’st booster circuit
V1T	I	V1 voltage adjustment pin. It is valid only when the external temperature compensation circuit is used. Otherwise, the ITO pattern is recommended not to be made for this pin. Note : V1T is recommended to connect the external capacitor with GND if much noise is injected into this pin.
INTRS	I	External resistor select pin for temperature compensation circuit - INTRS = L : External resistor mode, INTRS = H : Internal resistor mode
DC2IN	I	Power supply for 2’nd booster. Connect to DC2OUT pin
DC2OUT	O	Power output pin for 2’nd booster input
C21P C21M C22P C22M C23P C23M	O	External capacitor connection pins used for 2’nd booster circuit
C31P C31M	O	External capacitor connection pins used for 3’rd booster circuit
MTPV	I	Power supply for MTP programming

Table 4. MPU Interface Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RSTB</td><td>I</td><td>Reset input pin. When RSTB is “L”, initialization is executed.</td></tr>
<tr><td rowspan="9">PS
MPU[1:0]</td><td rowspan="9">I</td><td>MPU interface select pin
<table>
<tr><th>PS</th><th>MPU[1]</th><th>MPU[0]</th><th>Description</th></tr>
<tr><td>H</td><td>L</td><td>L</td><td>8080-series 8bit interface</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>8080-series 16bit interface</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>6800-series 8bit interface</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>6800-series 16bit interface</td></tr>
<tr><td>L</td><td>L</td><td>X</td><td>3 pin SPI(Write only)</td></tr>
<tr><td>L</td><td>H</td><td>X</td><td>4 pin SPI(Write only)</td></tr>
</table></td></tr>
<tr><td>NOTE : In serial mode, WRB and RDB must be fixed to either VDD3 or VSS.</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select input pins
Data / instruction I/O is enabled only when CS1B is “L” and CS2 is “H”. When chip select is non-active, DB0 to DB15 are high impedance.</td></tr>
<tr><td>RS
(D/I)</td><td>I</td><td>Data / Instruction select input pin
– RS = “H”: DB0 to DB15 are display data
– RS = “L”: DB0 to DB7 are instruction data
NOTE : In 3 pins serial mode, RS pin doesn’t care.</td></tr>
<tr><td rowspan="3">WRB
(R/W)</td><td rowspan="3">I</td><td>Read / Write execution control pin
<table>
<tr><th>PS</th><th>MPU[1]</th><th>MPU Type</th><th>WRB</th><th>Description</th></tr>
<tr><td>H</td><td>H</td><td>6800-series</td><td>R/W</td><td>Read / Write control input pin
– R/W = “H”: read
– R/W = “L”: write</td></tr>
<tr><td>H</td><td>L</td><td>8080-series</td><td>WRB</td><td>Write enable clock input pin
The data on DB0 to DB15 are latched at the rising edge of the WRB signal.</td></tr>
</table></td></tr>
<tr><td rowspan="3">RDB
(E)</td><td rowspan="3">I</td><td>Read / Write execution control pin
<table>
<tr><th>PS</th><th>MPU[1]</th><th>MPU type</th><th>RDB</th><th>Description</th></tr>
<tr><td>H</td><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
– R/W = “H”: When E is “H”, DB0 to DB15 are in an output status.
– R/W = “L”: The data on DB0 to DB15 are latched at the falling edge of the E signal.</td></tr>
<tr><td>H</td><td>L</td><td>8080-series</td><td>RDB</td><td>Read enable clock input pin
When RDB is “L”, DB0 to DB15 are in an output status.</td></tr>
</table></td></tr>
<tr><td>DB[15:8]
DB[7]/SDI
DB[6]/SCL
DB[5:0]</td><td>I/O</td><td>-DB[15:0]: 16-bit bi-directional data bus.
-SDI: Serial data input pin. The data is latched at the rising edge of SCL.
-SCL: Serial clock input pin.
When these pins are not used according to mode, these pins must be connected to VDD3 or VSS</td></tr>
<tr><td>CDIR</td><td>I</td><td>Common direction select pin.</td></tr>
</table>

Table 5. Oscillator and Power Regulator Pins

Name	I/O	Description
OSC1 OSC2	I/O	CR oscillator output pin When the internal CR oscillator is used, connect to OSC1 through a resistor. OSC1 – OSC2: Using in normal display mode, partial display mode 0 When an external oscillator is used, OSC1 pin is connected to VSS.
OSC5	I	External clock input pin When an external input is used, it is input to this pin. But the internal oscillator is used, this pin is connected to VDD3 or VSS.
REG_OUT	O	Internal voltage regulator output pin The regulator output port from this pin is used as a power supplier for an internal digital block via VDD pins.

Table 6. Timing signal Pins for monitoring

Name	I/O	Description
CL	O	Shift clock output pin
PM	O	Field delimiter output pin
FR	O	Liquid crystal alternating current output pin

Table 7. LCD driver output pins

Name	I/O	Description
SEGA0 to 131	O	LCD driving segment output (Red or Blue)
SEGB0 to 131	O	LCD driving segment output (Green)
SEGC0 to131	O	LCD driving segment output (Blue or Red)
COM0 to 161	O	LCD common outputs

Table 8. Test pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>MODE[1:0]</td><td>I</td><td>Don’t use these pins. IC maker’s test pins
These pins must be tied to VDD3.</td></tr>
<tr><td>FUSE_EN</td><td>I</td><td>Don’t use this pin. IC maker’s test pin. This pin must be tied to VDD3.</td></tr>
<tr><td>ZIGZAG_MODE</td><td>I</td><td>COM group scan mode select pin.
- ZIGZAG_MODE = H : COM group scanning operates in zigzag.
In this mode, ZIGZAG_MODE pin is tied to VDD3.
- ZIGZAG_MODE = L : COM group scanning operates in sequence.
In this mode, ZIGZAG_MODE pin is tied to VSS3.</td></tr>
<tr><td>PF[1:0]</td><td>I</td><td>Oscillator frequency select pin in partial mode 1
<table>
<tr><th>PF[1:0]</th><th>Partial mode 1 OSC frequency</th></tr>
<tr><td>00</td><td>fOSC / 2</td></tr>
<tr><td>01</td><td>fOSC / 3 (default)</td></tr>
<tr><td>10</td><td>fOSC / 4</td></tr>
<tr><td>11</td><td>fOSC / 5</td></tr>
</table>
In default setting, PF[1] is tied to VSS3, PF[0] is tied to VDD3
Note: fOSC is a oscillation frequency generated by CR oscillator.</td></tr>
<tr><td>RTEST</td><td>I</td><td>Don’t use this pin. IC maker’s test pin
This pin must be tied to VSS3.</td></tr>
<tr><td>DUMMY</td><td>-</td><td>Dummy pins are must floating. These pins are connected to VSS internally.</td></tr>
</table>

FUNCTIONAL DESCRIPTION

MPU INTERFACE

Chip Select Input

There are CS1B and CS2 pins for chip selection. The S6B33BL can interface with an MPU only when CS1B is “L” and CS2 is “H”. When these pins are set to any other combination, RS, RDB, and WRB inputs are disabled and DB0 to DB15 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel/Serial Interface

The S6B33BL has four types of interface with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in Table9.

Table 9. Parallel / Serial Interface Mode.

PS	MPU[1]	CS1B	CS2	MPU bus type
H	L	CS1B	CS2	8080-Series MPU
	H			6800-Series MPU
L	L	CS1B	CS2	3–Pin SPI
	H			4-Pin SPI

Parallel Interface (PS=”H”)

The 8-bit/16-bit bi-directional data bus is used in parallel interface. The type of MPU is selected by MPU[1] and the mode of data-bus is controlled by MPU[0] as shown in below. In accessing internal registers (RS = “L”), only DB[7:0] are valid.

Table 10. Microprocessor Selection for Parallel Interface

MPU[1]	MPU[0]	CS1B	CS2	RDB	WRB	Data Bus	MPU bus type
L	L	CS1B	CS2	RDB	WRB	DB[7:0]	8080-series MPU
	H					DB[15:0]	
H	L	CS1B	CS2	E	R/W	DB[7:0]	6800-series MPU
	H					DB[15:0]	

Table 11. Parallel Data Transfer

RS	6800-series		8080-series		Description
	RDB	WRB	RDB	WRB	
H	H	H	L	H	Read display data
H	H	L	H	L	Write display data
L	H	H	L	H	Read out internal status register
L	H	L	H	L	Write instruction data

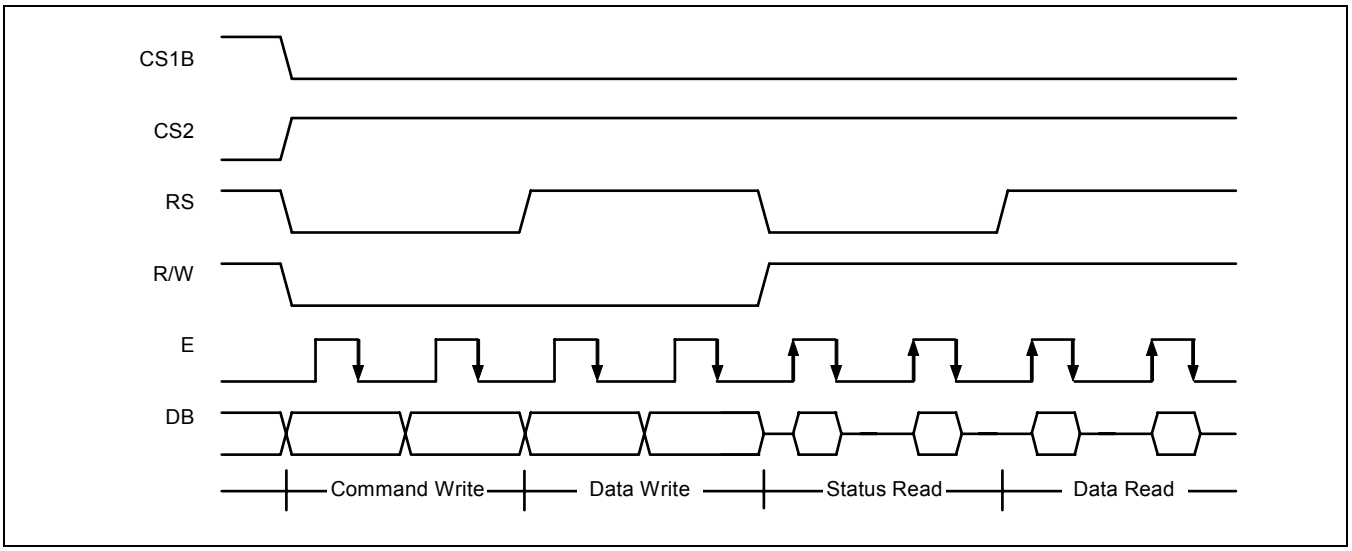


Figure 5. 6800-Series MPU Interface protocol (MPU[1]="H")

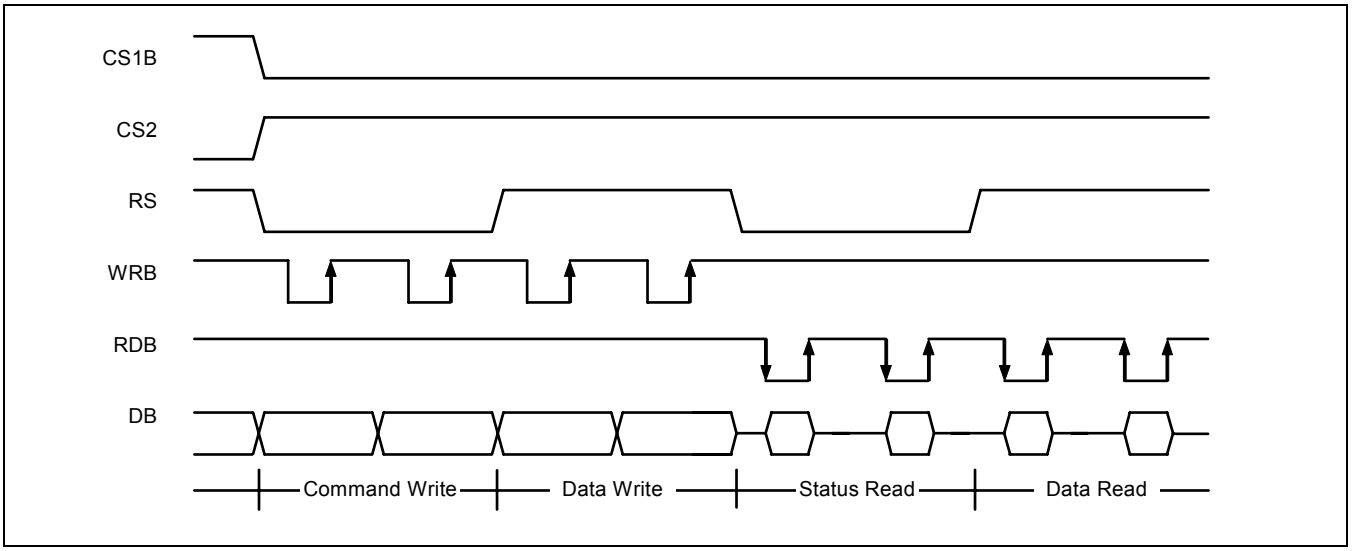


Figure 6. 8080-Series MPU Interface Protocol (MPU[1]="L")

Serial Interface (PS="L")

Communication with the microprocessor occurs via a clock-synchronized serial peripheral interface when PS is low. When using the serial interface, read operations are not allowed. When the chip select inputs are valid (CS1B = "L" & CS2 = "H"), the serial data is sent most significant bit first on the rising edge of a serial clock going into DB6 and processed as 8 bit parallel data on the eighth clock. Since the clock signal is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended. And Invalid, the internal shift register and the counter are reset.
The serial interface type is selected by setting PS as shown in Table12.

Table 12. Microprocessor Selection for Serial Interface

PS	MPU[1]	CS1B	CS2	RS	Serial Data	Serial Clock	SPI Mode
L	L	CS1B	CS2	By S/W	DB[7]	DB[6]	3-Pin
	H	CS1B	CS2	RS			4-Pin

3-Pin SPI Interface (PS = "L" & MPU[1] = "L")

In 3-Pin SPI Interface mode, the first bit of serial 9bits is used to indicate whether serial data input is display or instruction data instead of RS pin. The serial data format consists of RS (1bit) and DATA (8bits). For details, refer the Figure 7.

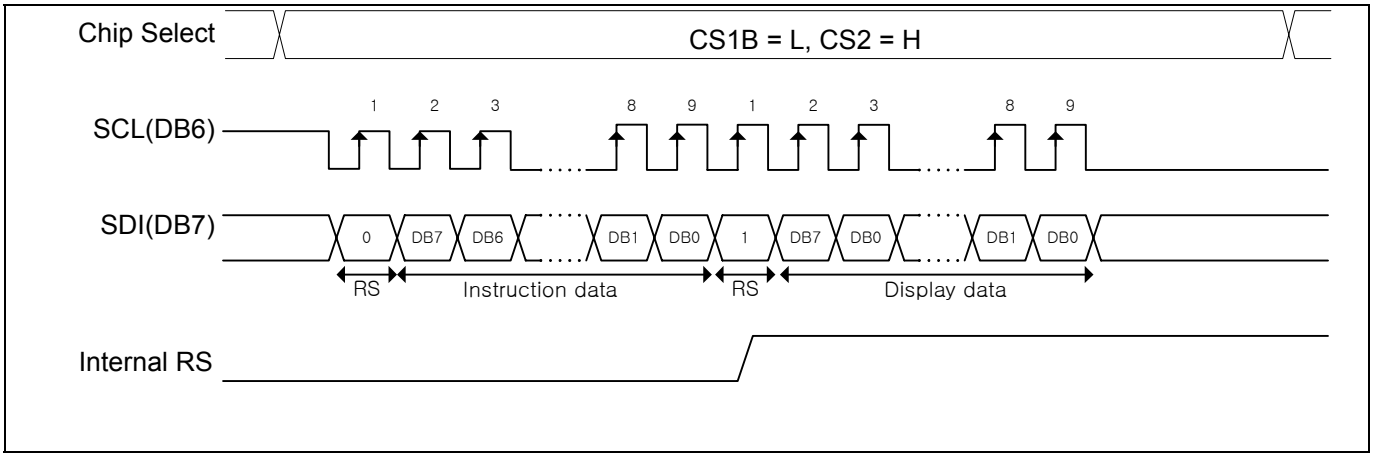


Figure 7. 3-Pin SPI Timing (RS is not used)

4-Pin Serial Interface (PS = ”L” & MPU[1] = ”H”)

In 4-pin SPI interface mode, RS pin is used for indicating whether serial data input is display or instruction data. Data is display data when RS is high and instruction data when RS is low.
Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock.

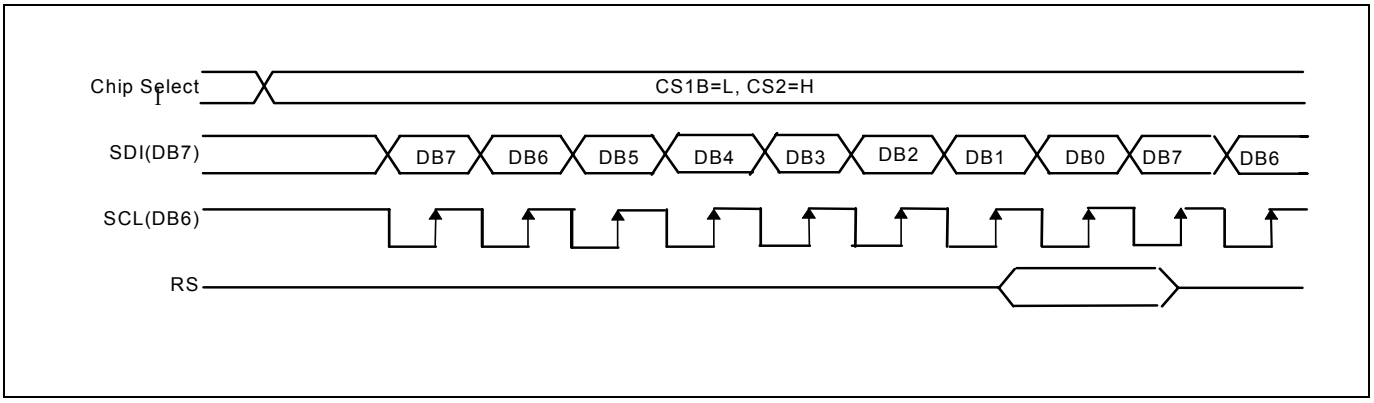


Figure 8. 4-Pin Serial Interface Timing

DISPLAY DATA RAM

The on-chip display data RAM of S6B33BL is a static RAM that is stored the data for the display. It is a 132 x 16 x 162 structure. It is controlled by 2 addresses, X and Y. And, RAM area selection and automatic address count up functions are accomplished by the internal instructions.

DDRAM Address Area Selection

A part of DDRAM address area of S6B33BL can be accessed by X and Y address area settings. After setting RAM area, the addresses become the start address.

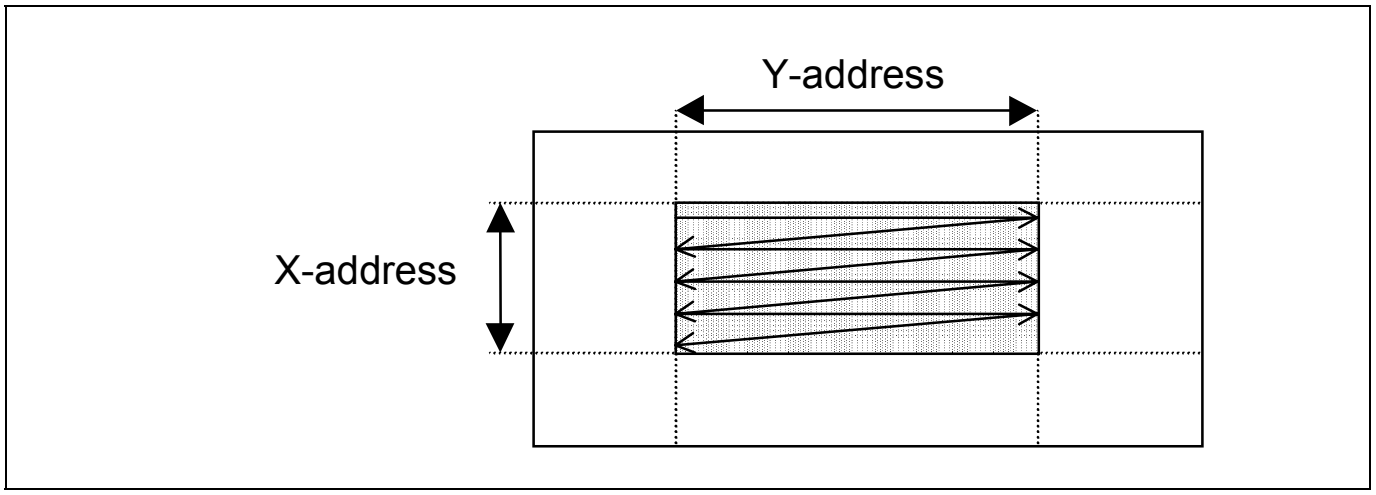


Figure 9. DDRAM Address Area

Table 13. X address Control

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	0	0	0	0	1
P1	X start address set(Initial Status = 00H)							
P2	X end address set(Initial Status = A1H)							

Table 14. Y address Control

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	1	0	0	0	1
P1	Y start address set (Initial status = 00H)							
P2	Y end address set (Initial status =83H)							

RAM Addressing Count up

By selecting the X address and Y address area by the internal instructions, the address counts up from its start address to end address after data access operation. When one address is equal to the end address, it returns to the start address. At this time, the other address is increased by 1.

Y address count mode (Y address = 00h to 83h, X address = 00h to A1h)

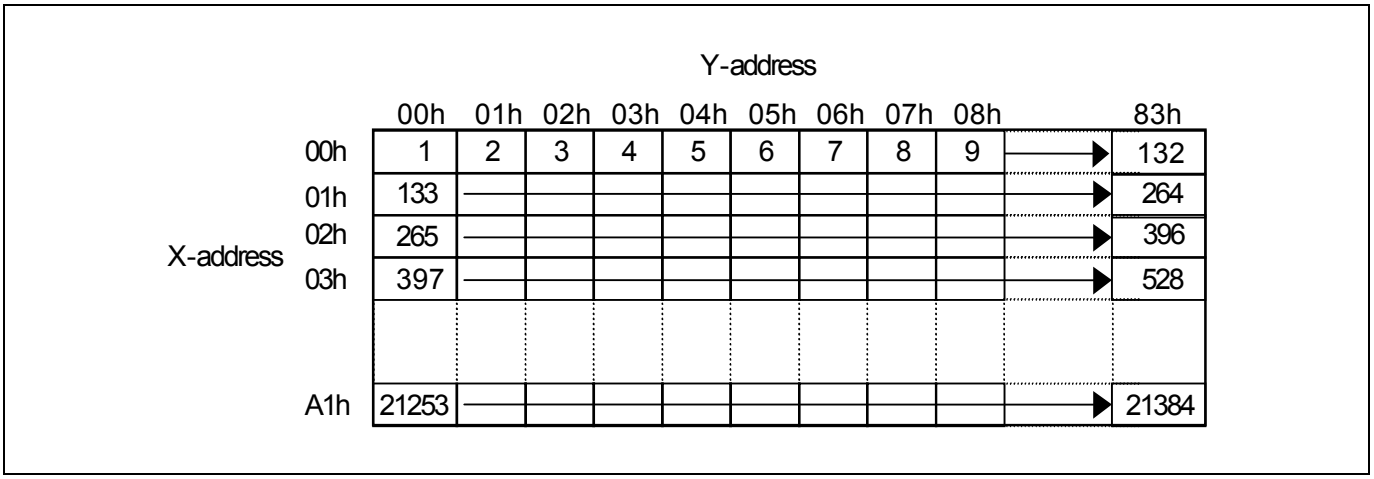


Figure 10. Y address count mode

X address count mode (Y address =00h to 83h, X address = 00h to A1h)

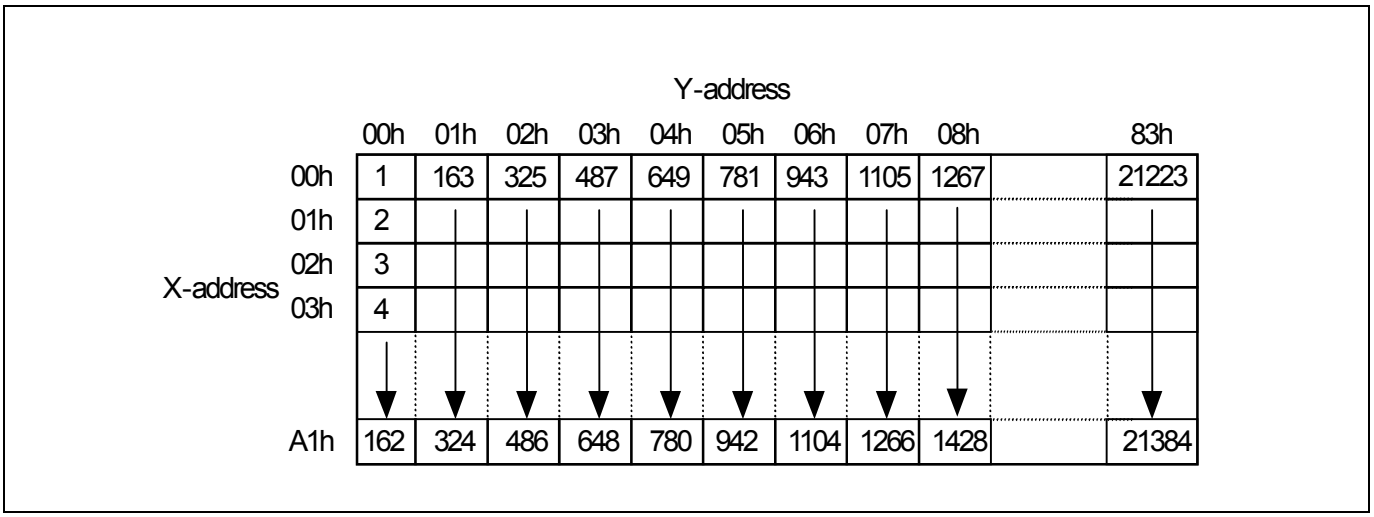


Figure 11. X address count mode

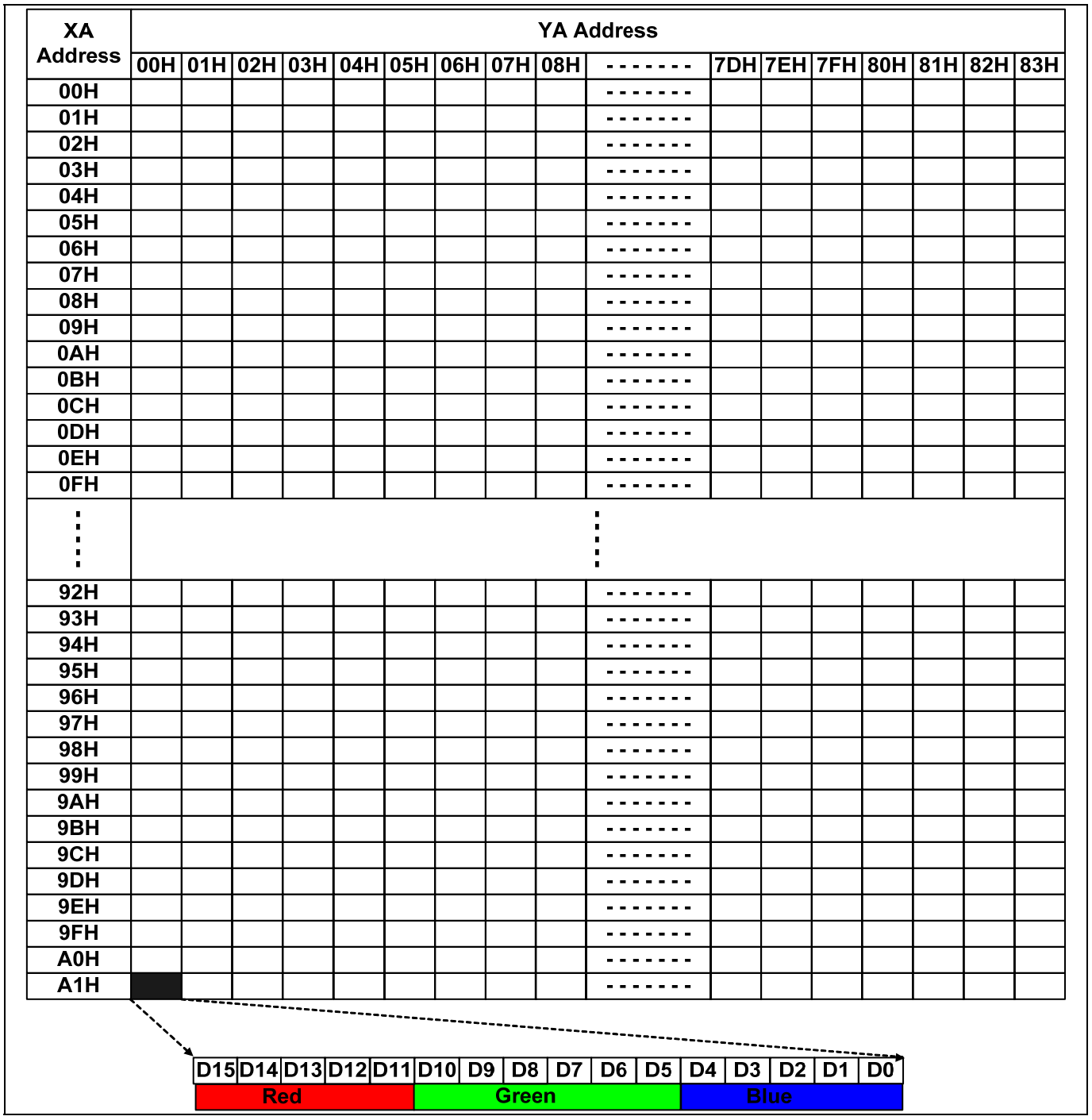


Figure 12. Display Data RAM Map

Partial Display Mode

The S6B33BL realizes the partial display function with low duty driving for saving power consumption and showing the various display duties. It is set as display start/end line number.

Area Scroll Function

The S6B33BL realizes the specific area scroll function. (1/162 duty case).

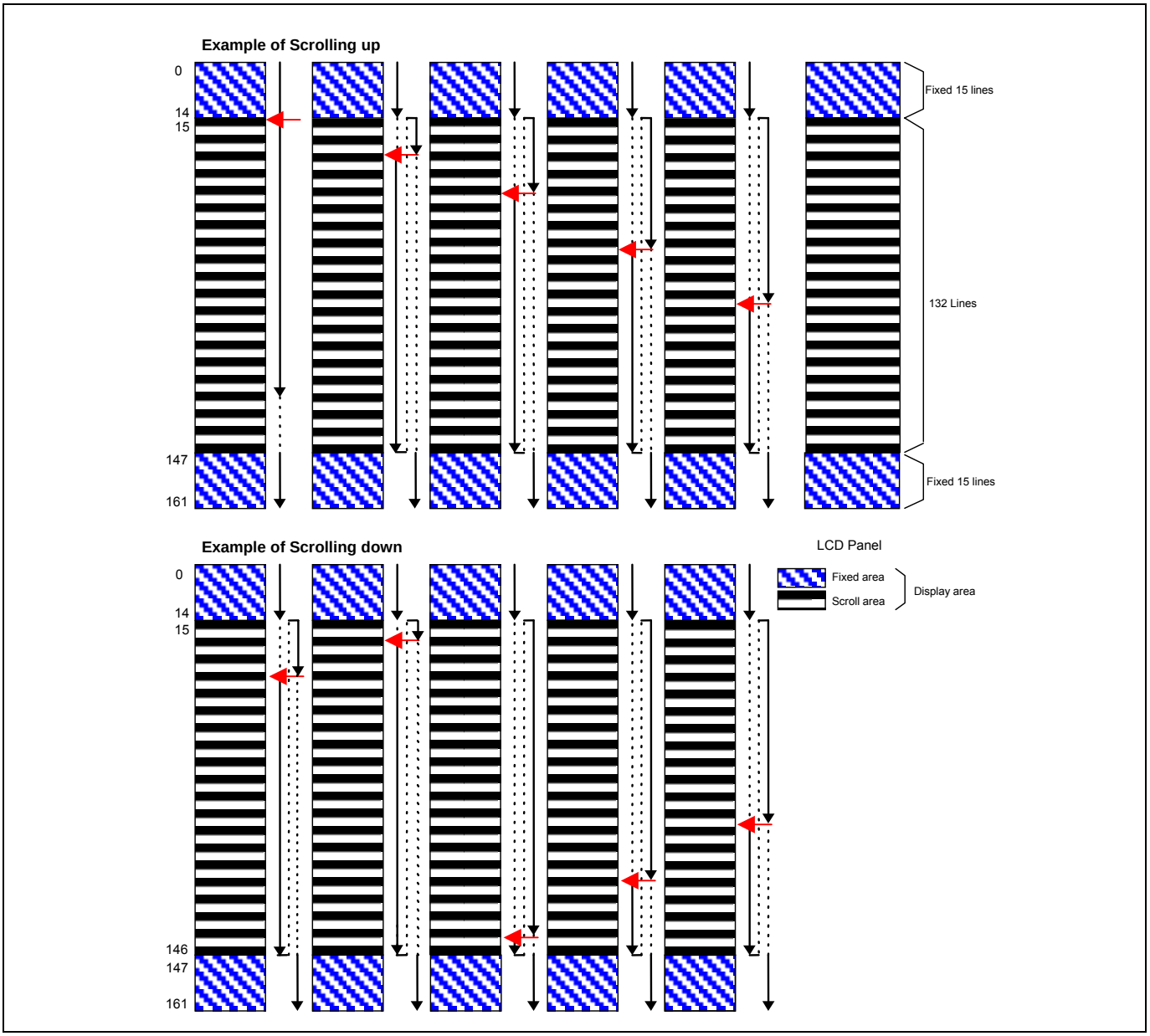


Figure 13. Area scroll examples (duty = 1/162, center scroll mode)

Display Direction

SDIR

The SDIR flag of Driver Output Mode Set instruction selects the direction of segment display.

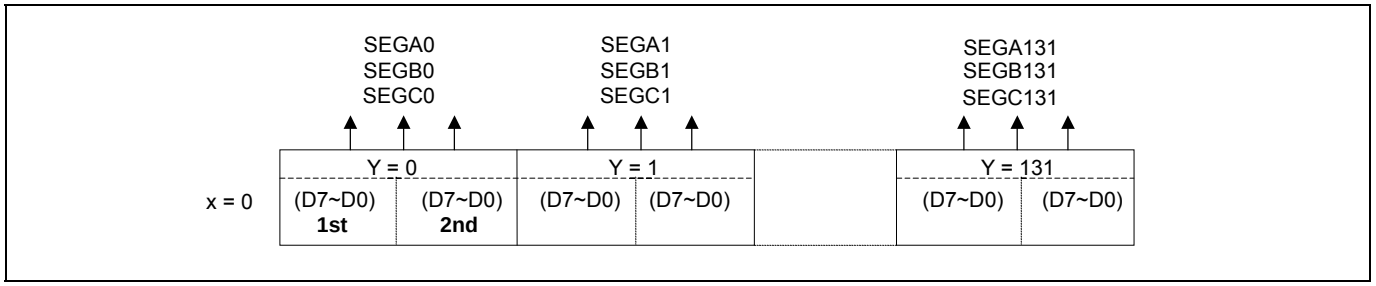


Figure 14. 8-bit data bus mode when SDIR = L

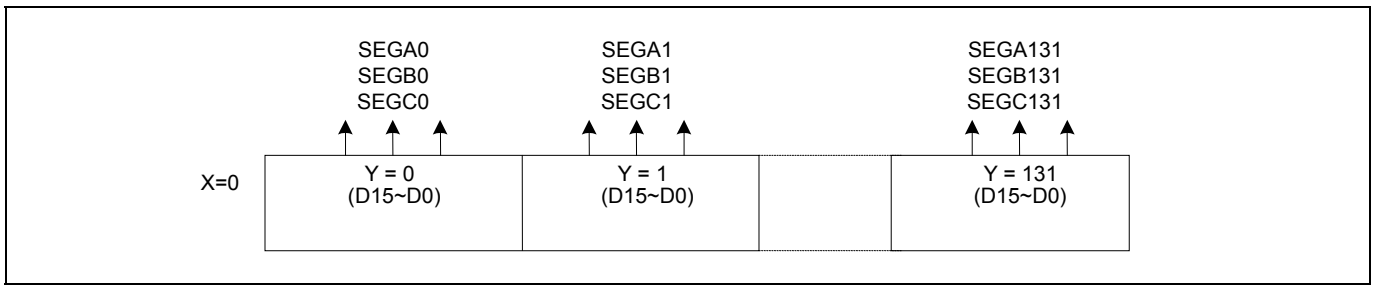


Figure 15. 16-bit data bus mode when SDIR = L

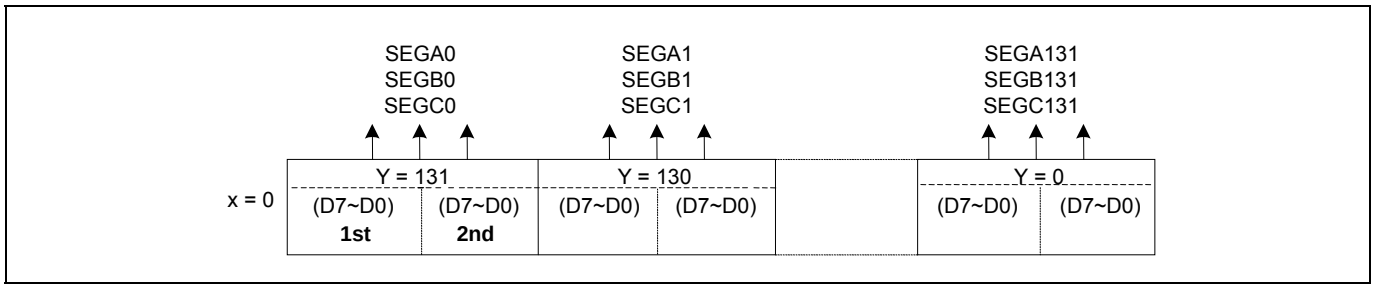


Figure 16. 8-bit data bus mode when SDIR = H

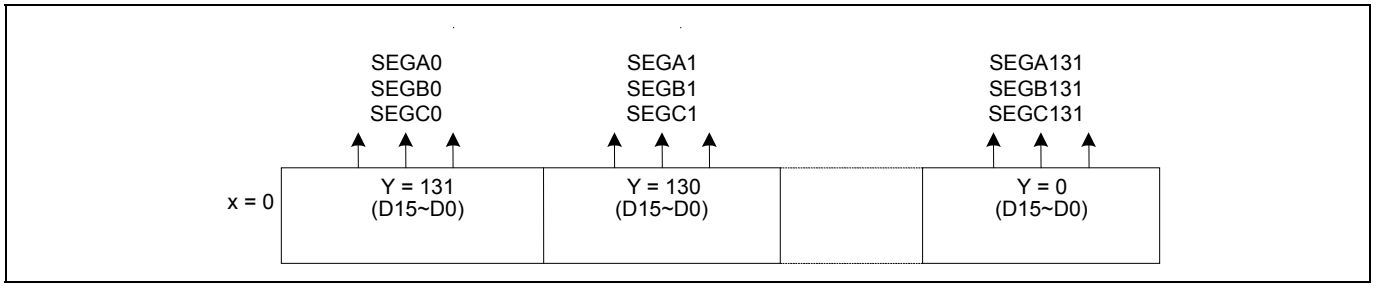
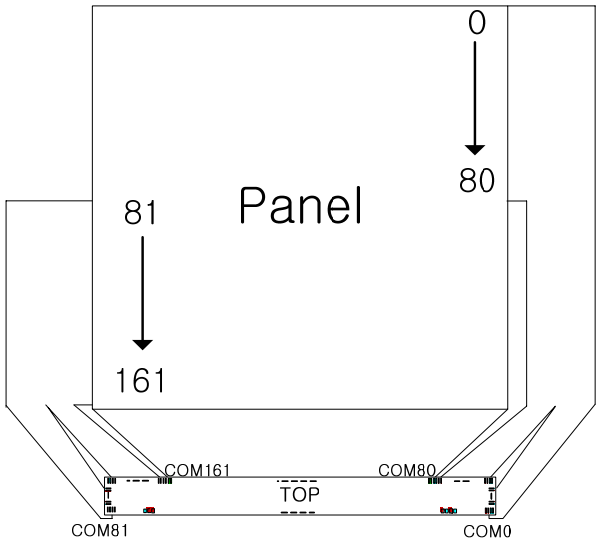


Figure 17. 16-bit data bus mode when SDIR = H

COM Group Scan Mode

There is ZIGZAG_MODE pin for COM group scan mode selection.

ZIGZAG_MODE=0
COM group scanning operates in sequence.



ZIGZAG_MODE=1
COM group scanning operates in zigzag.

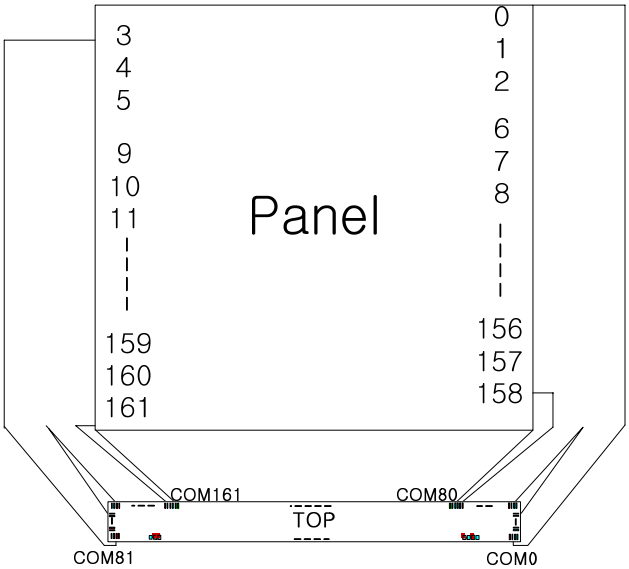


Figure 18. The relationship between COM outputs and Panel

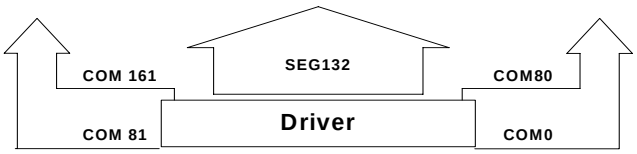
The relationship between COM outputs and display line of panel (CDIR=0)

Display Line Number	Common Number ZIGZAG_ MODE=0	Common Number ZIGZAG_ MODE=1	Display Line Number	Common Number ZIGZAG _MODE =0	Common Number ZIGZAG_ MODE=1	Display Line Number	Common Number ZIGZAG_ MODE=0	Common Number ZIGZAG_ MODE=1
Line Number0	COM0	COM0	Line Number51	COM51	COM105	Line Number102	COM102	COM51
Line Number1	COM1	COM1	Line Number52	COM52	COM106	Line Number103	COM103	COM52
Line Number2	COM2	COM2	Line Number53	COM53	COM107	Line Number104	COM104	COM53
Line Number3	COM3	COM81	Line Number54	COM54	COM27	Line Number105	COM105	COM132
Line Number4	COM4	COM82	Line Number55	COM55	COM28	Line Number106	COM106	COM133
Line Number5	COM5	COM83	Line Number56	COM56	COM29	Line Number107	COM107	COM134
Line Number6	COM6	COM3	Line Number57	COM57	COM108	Line Number108	COM108	COM54
Line Number7	COM7	COM4	Line Number58	COM58	COM109	Line Number109	COM109	COM55
Line Number8	COM8	COM5	Line Number59	COM59	COM110	Line Number110	COM110	COM56
Line Number9	COM9	COM84	Line Number60	COM60	COM30	Line Number111	COM111	COM135
Line Number10	COM10	COM85	Line Number61	COM61	COM31	Line Number112	COM112	COM136
Line Number11	COM11	COM86	Line Number62	COM62	COM32	Line Number113	COM113	COM137
Line Number12	COM12	COM6	Line Number63	COM63	COM111	Line Number114	COM114	COM57
Line Number13	COM13	COM7	Line Number64	COM64	COM112	Line Number115	COM115	COM58
Line Number14	COM14	COM8	Line Number65	COM65	COM113	Line Number116	COM116	COM59
Line Number15	COM15	COM87	Line Number66	COM66	COM33	Line Number117	COM117	COM138
Line Number16	COM16	COM88	Line Number67	COM67	COM34	Line Number118	COM118	COM139
Line Number17	COM17	COM89	Line Number68	COM68	COM35	Line Number119	COM119	COM140
Line Number18	COM18	COM9	Line Number69	COM69	COM114	Line Number120	COM120	COM60
Line Number19	COM19	COM10	Line Number70	COM70	COM115	Line Number121	COM121	COM61
Line Number20	COM20	COM11	Line Number71	COM71	COM116	Line Number122	COM122	COM62
Line Number21	COM21	COM90	Line Number72	COM72	COM36	Line Number123	COM123	COM141
Line Number22	COM22	COM91	Line Number73	COM73	COM37	Line Number124	COM124	COM142
Line Number23	COM23	COM92	Line Number74	COM74	COM38	Line Number125	COM125	COM143
Line Number24	COM24	COM12	Line Number75	COM75	COM117	Line Number126	COM126	COM63
Line Number25	COM25	COM13	Line Number76	COM76	COM118	Line Number127	COM127	COM64
Line Number26	COM26	COM14	Line Number77	COM77	COM119	Line Number128	COM128	COM65
Line Number27	COM27	COM93	Line Number78	COM78	COM39	Line Number129	COM129	COM144
Line Number28	COM28	COM94	Line Number79	COM79	COM40	Line Number130	COM130	COM145
Line Number29	COM29	COM95	Line Number80	COM80	COM41	Line Number131	COM131	COM146
Line Number30	COM30	COM15	Line Number81	COM81	COM120	Line Number132	COM132	COM66
Line Number31	COM31	COM16	Line Number82	COM82	COM121	Line Number133	COM133	COM67
Line Number32	COM32	COM17	Line Number83	COM83	COM122	Line Number134	COM134	COM68
Line Number33	COM33	COM96	Line Number84	COM84	COM42	Line Number135	COM135	COM147
Line Number34	COM34	COM97	Line Number85	COM85	COM43	Line Number136	COM136	COM148
Line Number35	COM35	COM98	Line Number86	COM86	COM44	Line Number137	COM137	COM149
Line Number36	COM36	COM18	Line Number87	COM87	COM123	Line Number138	COM138	COM69
Line Number37	COM37	COM19	Line Number88	COM88	COM124	Line Number139	COM139	COM70
Line Number38	COM38	COM20	Line Number89	COM89	COM125	Line Number140	COM140	COM71
Line Number39	COM39	COM99	Line Number90	COM90	COM45	Line Number141	COM141	COM150
Line Number40	COM40	COM100	Line Number91	COM91	COM46	Line Number142	COM142	COM151
Line Number41	COM41	COM101	Line Number92	COM92	COM47	Line Number143	COM143	COM152
Line Number42	COM42	COM21	Line Number93	COM93	COM126	Line Number144	COM144	COM72
Line Number43	COM43	COM22	Line Number94	COM94	COM127	Line Number145	COM145	COM73
Line Number44	COM44	COM23	Line Number95	COM95	COM128	Line Number146	COM146	COM74
Line Number45	COM45	COM102	Line Number96	COM96	COM48	Line Number147	COM147	COM153
Line Number46	COM46	COM103	Line Number97	COM97	COM49	Line Number148	COM148	COM154
Line Number47	COM47	COM104	Line Number98	COM98	COM50	Line Number149	COM149	COM155
Line Number48	COM48	COM24	Line Number99	COM99	COM129	Line Number150	COM150	COM75
Line Number49	COM49	COM25	Line Number100	COM100	COM130	Line Number151	COM151	COM76
Line Number50	COM50	COM26	Line Number101	COM101	COM131	Line Number152	COM152	COM77
Display Line	Common	Common	Display Line	Common	Common	Display Line	Common	Common

Number	Number ZIGZAG_ MODE=0	Number ZIGZAG_ MODE=1	Number	Number ZIGZAG _MODE =0	Number ZIGZAG_ MODE=1	Number	Number ZIGZAG_ MODE=0	Number ZIGZAG_ MODE=1
Line Number153	COM153	COM156						
Line Number154	COM154	COM157						
Line Number155	COM155	COM158						
Line Number156	COM156	COM78						
Line Number157	COM157	COM79						
Line Number158	COM158	COM80						
Line Number159	COM159	COM159						
Line Number160	COM160	COM160						
Line Number161	COM161	COM161						

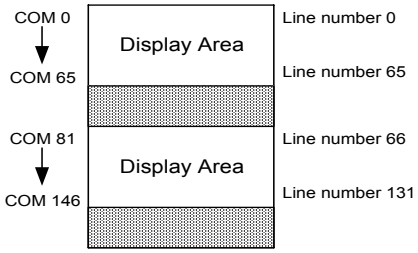
CDIR

The CDIR flag of Driver Output Mode Set Instruction selects the direction of common driver scanning. (ZIGZAG_MODE=0)
COM group scanning operates in sequence.

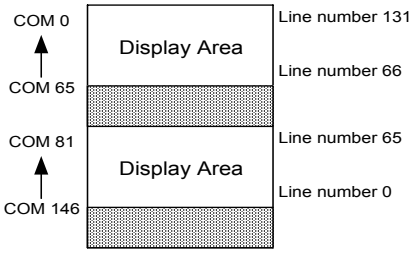


132 Display Lines (DLN=00)

<CDIR=0>

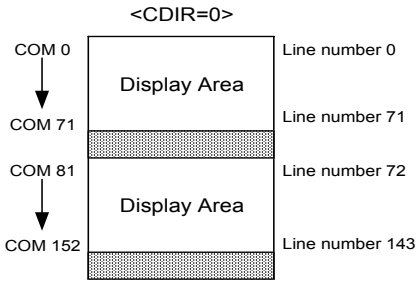


<CDIR=1>

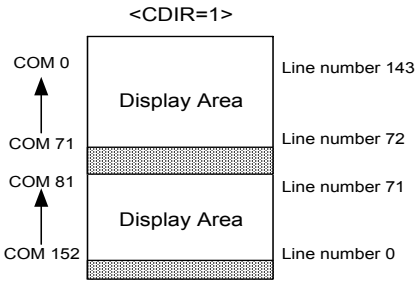


144 Display Lines (DLN=01)

<CDIR=0>

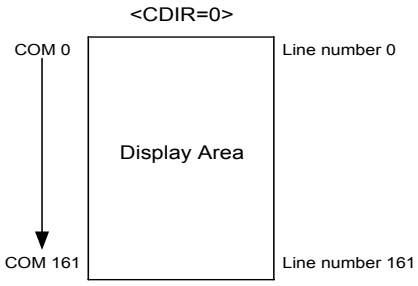


<CDIR=1>

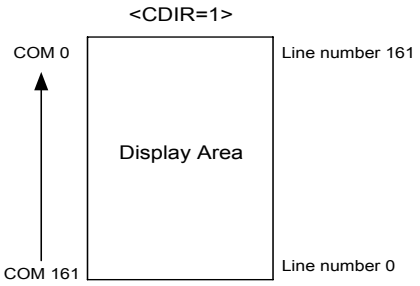


162 Display Lines (DLN=10)

<CDIR=0>

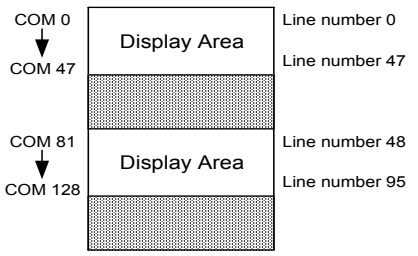


<CDIR=1>

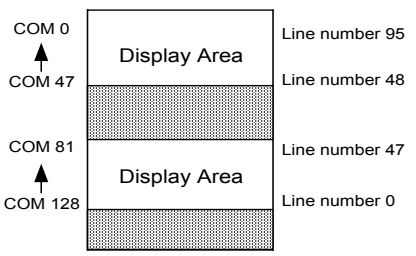


96 Display Lines (DLN=11)

<CDIR=0>



<CDIR=1>



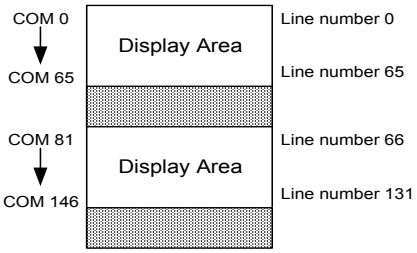
SAMSUNG ELECTRONICS

CDIR

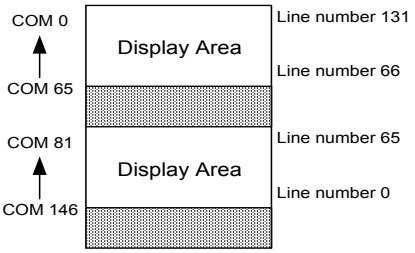
The CDIR flag of Driver Output Mode Set Instruction selects the direction of common driver scanning.
(ZIGZAG_MODE=1)
COM group scanning operates in zigzag

132 Display Lines (DLN=00)

<CDIR=0>

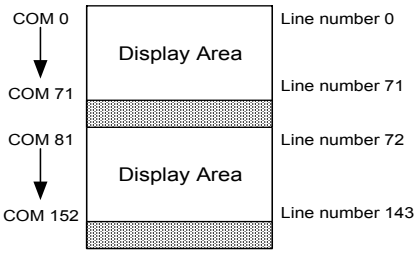


<CDIR=1>

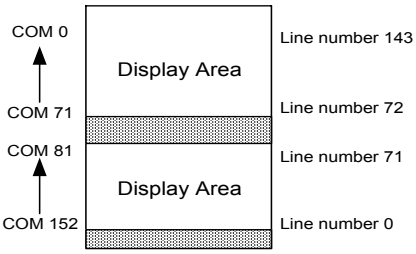


144 Display Lines (DLN=01)

<CDIR=0>

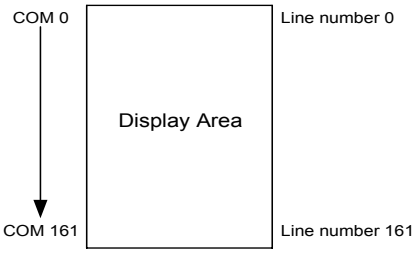


<CDIR=1>

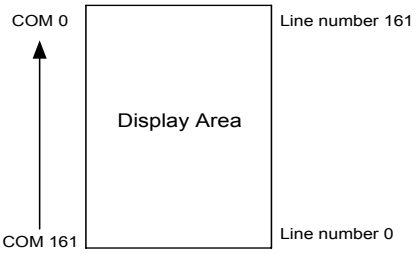


162 Display Lines (DLN=10)

<CDIR=0>

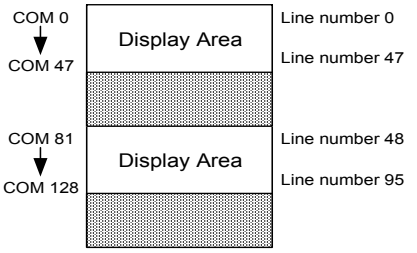


<CDIR=1>

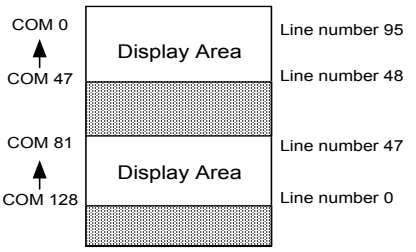


96 Display Lines (DLN=11)

<CDIR=0>

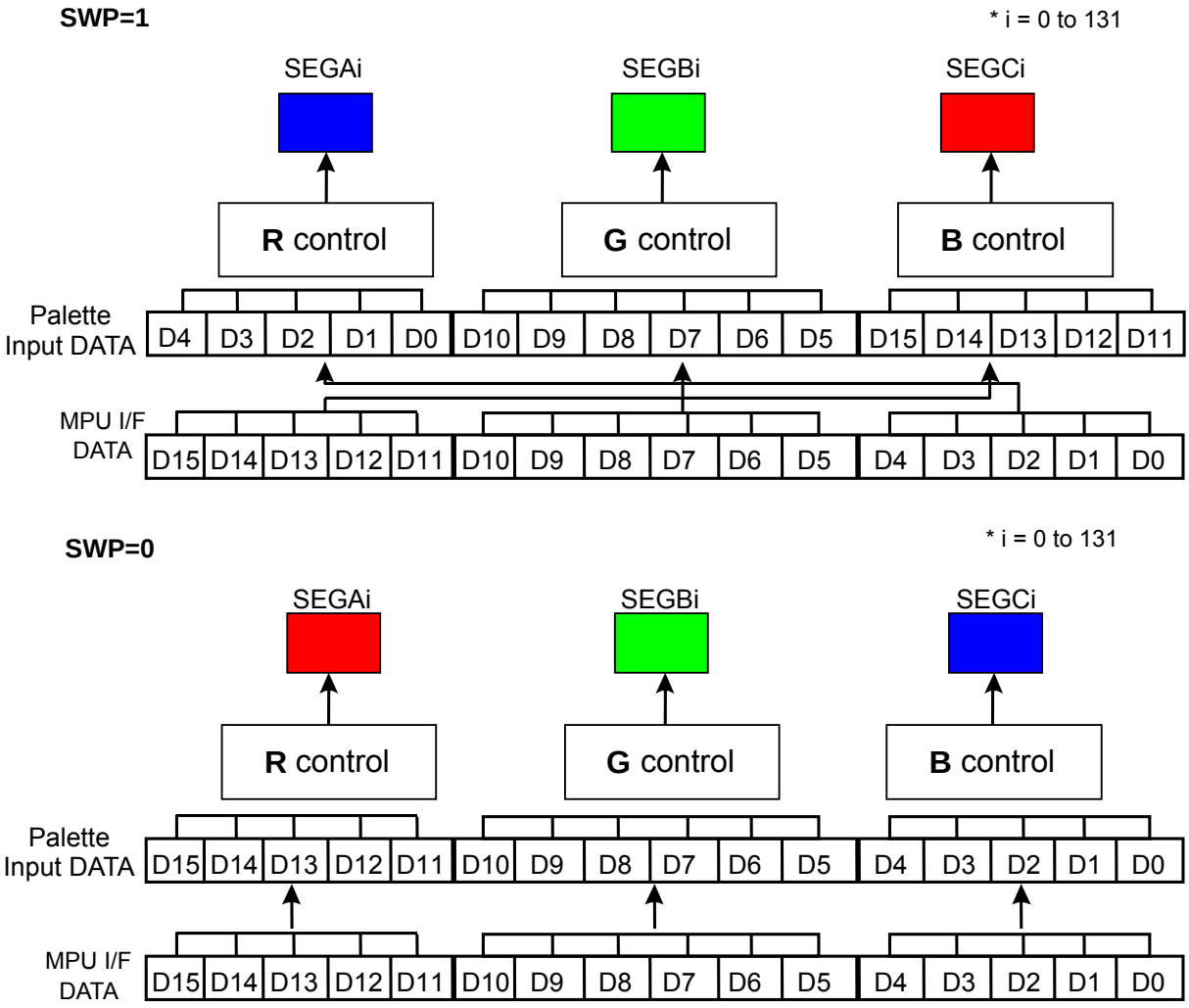


<CDIR=1>



SWP

The SWP flag of Driver Output Mode Set instruction selects the swapping of segment display.



	SEGAi	SEGBi	SEGCi	
SWP = 0	RED	GREEN	BLUE	Color
	D15 ~ D11	D10~ D5	D4 ~ D0	Assigned Bit
SWP = 1	BLUE	GREEN	RED	Color
	D4~ D0	D10 ~ D5	D15 ~ D11	Assigned Bit

Figure 19. The relationship between SEG outputs and RGB color

OSCILLATOR CIRCUIT

When internal oscillator is used(EXT=0): resistor between OSC1 and OSC2.

Note : In R-C oscillator, the oscillation frequency is changed according to the external resistance value, ITO wire length, or operating power-supply voltage (VDDO).
In Partial display mode1, oscillation frequency is set by PF[1:0] pin or Partial mode1 frequency control command (37h). Refer to Partial mode1 frequency control command

When external clock is used (EXT=1), clock frequency should be adjusted to display mode that is selected.

Example of external oscillator application

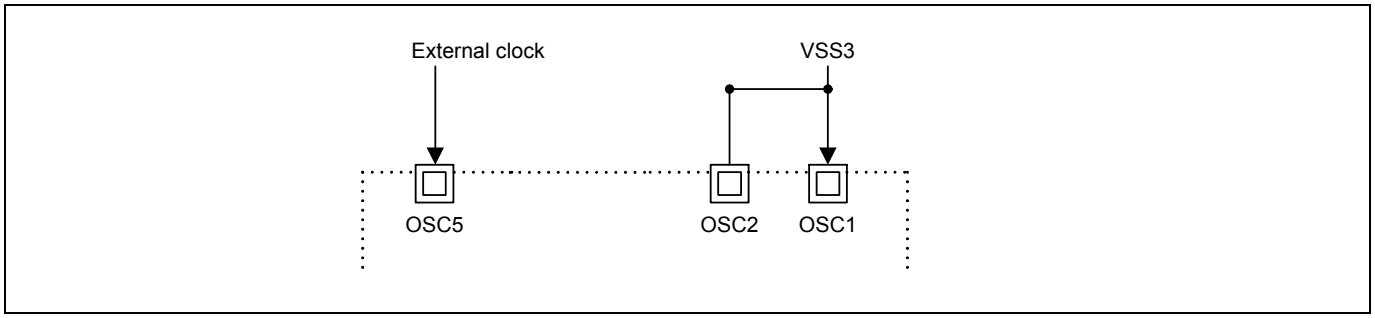


Figure 20. External oscillator application

Example of internal oscillator application

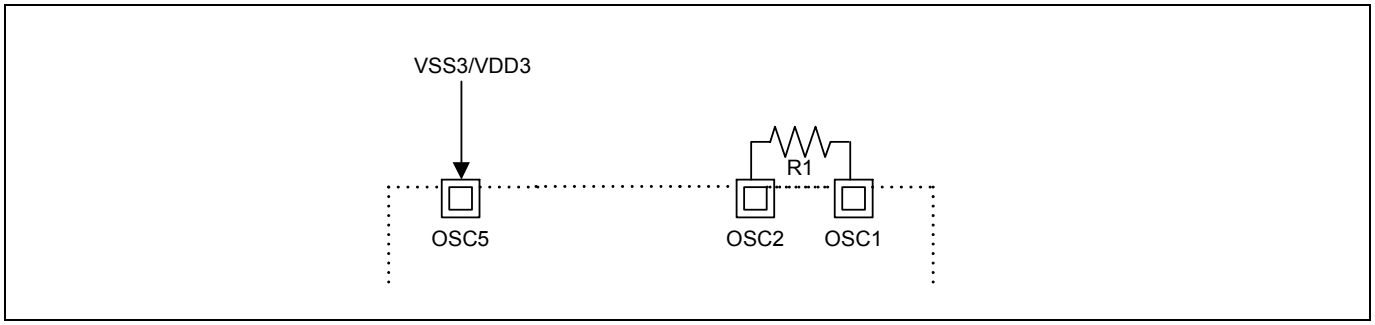
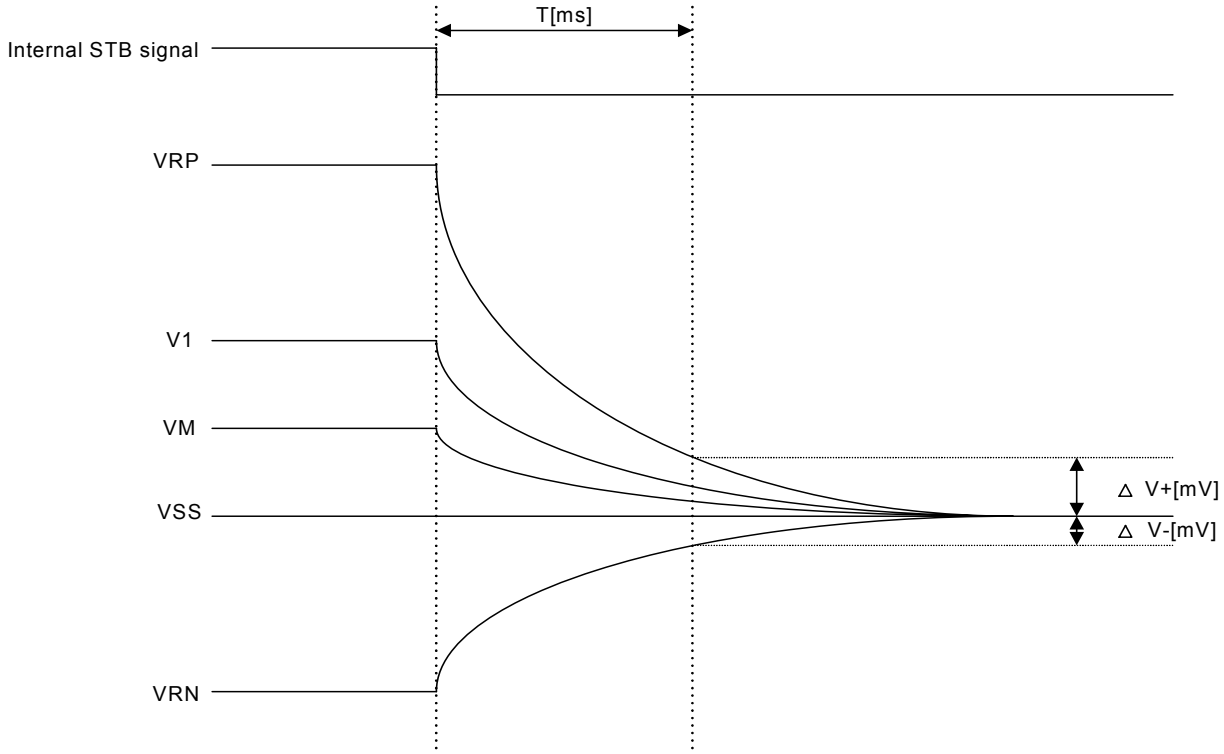


Figure 21. Internal oscillator application

DISCHARGE CIRCUIT

Driving voltage level discharge time at standby ON.



The relation between voltage level and discharge time from when “Standby ON” command is inputted.

LEVEL	CONDITION	T[ms]	ΔV+,ΔV-[mV]
VRP,V1,VM,VRN	VRP=12.0V, V1=3.0V, VM=1.5V, VRN=-9.0V at T=0	100	< 50
		300	< 20

INSTRUCTION DESCRIPTION

Table 15. Instruction Table

Instruction Name	RS	WRB	RDB	DB15 ~ DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.	Parameter
Non Operation	0	0	1	*	0	0	0	0	0	0	0	0	00	
Oscillation Mode Set	0	0	1	*	0	0	0	0	0	0	1	0	02	1Byte
Driver Output Mode Set	0	0	1	*	0	0	0	1	0	0	0	0	10	1Byte
Monitor Signal Control	0	0	1	*	0	0	0	1	1	0	0	0	18	1Byte
DC-DC Select	0	0	1	*	0	0	1	0	0	0	0	0	20	1Byte
Bias Set	0	0	1	*	0	0	1	0	0	0	1	0	22	1Byte
DCDC Clock Division Set	0	0	1	*	0	0	1	0	0	1	0	0	24	1Byte
DCDC and AMP ON/OFF set	0	0	1	*	0	0	1	0	0	1	1	0	26	1Byte
Temperature Compensation Set	0	0	1	*	0	0	1	0	1	0	0	0	28	1Byte
Contrast Control(1)	0	0	1	*	0	0	1	0	1	0	1	0	2A	1Byte
Contrast Control(2)	0	0	1	*	0	0	1	0	1	0	1	1	2B	1Byte
Standby Mode OFF	0	0	1	*	0	0	1	0	1	1	0	0	2C	-
Standby Mode ON	0	0	1	*	0	0	1	0	1	1	0	1	2D	-
Addressing Mode Set	0	0	1	*	0	0	1	1	0	0	0	0	30	1Byte
ROW Vector Mode Set	0	0	1	*	0	0	1	1	0	0	1	0	32	1Byte
N-line Inversion Set	0	0	1	*	0	0	1	1	0	1	0	0	34	1Byte
Frame Frequency control	0	0	1	*	0	0	1	1	0	1	1	0	36	1Byte
Partial Mode1 Frequency control	0	0	1	*	0	0	1	1	0	1	1	1	37	1Byte
256 Color Red Palette	0	0	1	*	0	0	1	1	1	0	0	0	38	8Byte
256 Color Green Palette	0	0	1	*	0	0	1	1	1	0	1	0	3A	8Byte
256 Color Blue Palette	0	0	1	*	0	0	1	1	1	1	0	0	3C	4Byte
Entry Mode Set	0	0	1	*	0	1	0	0	0	0	0	0	40	1Byte
X-address Area Set	0	0	1	*	0	1	0	0	0	0	1	0	42	2Byte
Y-address Area Set	0	0	1	*	0	1	0	0	0	0	1	1	43	2Byte
RAM Skip Area Set	0	0	1	*	0	1	0	0	0	1	0	1	45	1Byte
Display OFF	0	0	1	*	0	1	0	1	0	0	0	0	50	-
Display ON	0	0	1	*	0	1	0	1	0	0	0	1	51	-
Specified Display Pattern Set	0	0	1	*	0	1	0	1	0	0	1	1	53	1Byte
Partial Display Mode Set	0	0	1	*	0	1	0	1	0	1	0	1	55	1Byte
Partial Display Start Line Set	0	0	1	*	0	1	0	1	0	1	1	0	56	1Byte
Partial Display End Line Set	0	0	1	*	0	1	0	1	0	1	1	1	57	1Byte
Area Scroll Mode Set	0	0	1	*	0	1	0	1	1	0	0	1	59	4Byte
Scroll Start Line Set	0	0	1	*	0	1	0	1	1	0	1	0	5A	1Byte
Data Format Select (Format A)	0	0	1	*	0	1	1	0	0	0	0	0	60	-
Data Format Select (Format B)	0	0	1	*	0	1	1	0	0	0	0	1	61	-
Set Display Data Length	X	X	X	*	1	1	1	1	1	1	0	0	FC	1Byte
Display Data Write	1	0	1	Display Data Write									-	-
Display Data Read	1	1	0	Display Data Read									-	-
Status Read	0	1	0	0	Status Data Read								-	-
Test Mode	0	0	1	*	1	1	1	1	*	*	*	*	F*	1Byte
Test Key Command	0	0	1	*	1	0	0	0	1	1	0	0	8C	-
MTP Load	0	0	1	*	1	1	1	0	0	1	0	1	E5	
MTP Read	0	0	1	*	1	1	1	0	0	1	1	0	E6	1Byte
MTP Initial Disable	0	0	1	*	1	1	1	0	1	0	0	0	E8	
MTP Initial Enable	0	0	1	*	1	1	1	0	1	0	0	1	E9	
MTP Mode Off	0	0	1	*	1	1	1	0	1	0	1	0	EA	
MTP Mode On	0	0	1	*	1	1	1	0	1	0	1	1	EB	

Offset Volume Set	0	0	1	*	1	1	1	0	1	1	0	1	ED	1Byte
MTP Write Disable	0	0	1	*	1	1	1	0	1	1	1	0	EE	
MTP Write Enable	0	0	1	*	1	1	1	0	1	1	1	1	EF	

*: Don’t care

Parameter: The number of parameter bytes that follows instruction data.

Non Operation (00H)

This instruction is Non operation.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	0	0

Oscillation Mode Set (02H)

Setting internal function mode.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1	0
			0	0	0	0	0	0	EXT	OSC

EXT: External clock selecting
EXT = 0: Internal clock mode (Initial status)
EXT = 1: External clock mode

OSC: Internal oscillator ON/OFF
OSC = 0: Internal oscillator OFF(Initial status)
OSC = 1: Internal oscillator ON

Driver Output Mode Set(10H)

This instruction sets the display direction.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	0	0	0	0
			0	0	DLN		0	SDIR	SWP	CDR

DLN: Display Line number selecting

DB5	DB4	Display Duty
0	0	1/132 (Initial status)
0	1	1/144
1	0	1/162
1	1	1/96

SDIR: Segment direction
This bit is for controlling the direction of segment driver.
SDIR = 0 (Initial status)

SWP: Swap segment output SEGAi and SEGCi
This bit is for swapping the output of segment driver.
SWP = 0 (Initial status)

CDR: Software COM direction change register
This bit and CDIR pin are for controlling the direction of common driver.
CDR = 0 (Initial status)
In case software control of COM direction, CDIR pin must be fixed at VSS.
In case hardware control of COM direction, CDR register must be set at 0.

CDIR	CDR	**CDIR (Internal Register)**
0	0	**0**
	1	**1**
1	0	**1**
	1	**1**

Monitor Signal Control (18H)

This instruction configures the output enable and timing of monitor signal

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	1	0	0	0
			0	0	0	0	0	PM	CL	FR

PM: Enable to transfer field delimiter signal to output pin by active high
PM = 0 (Initial status)

CL: Enable to transfer shift signal to output pin by active high
CL = 0 (Initial status)

FR: Enable to transfer liquid crystal alternating signal to output pin by active high
FR = 0 (Initial status)

DC-DC Select (20H)

Selects DC-DC step-up of the common driver in normal and partial mode

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	0	0	0
			0	0	0	0	DC(2)		DC(1)	

DC(1) : 1'st DC-DC booster boosting step select for V1 generation in normal mode and partial mode 0.
DC(2) : 1'st DC-DC booster boosting step select for V1 generation in partial mode 1.

DC(2) : In partial mode 1			**Operating voltage range**
DB3	**DB2**	**DC-DC step up**	**VIN1**
0	**0**	**X1.0**	**2.4~3.6[V]**
0	**1**	**X1.5**	**2.4~3.6[V]**
1	**0**	**X2.0**	**2.4~3.0[V]**
1	**1**	**X2.0**	**2.4~3.0[V]**

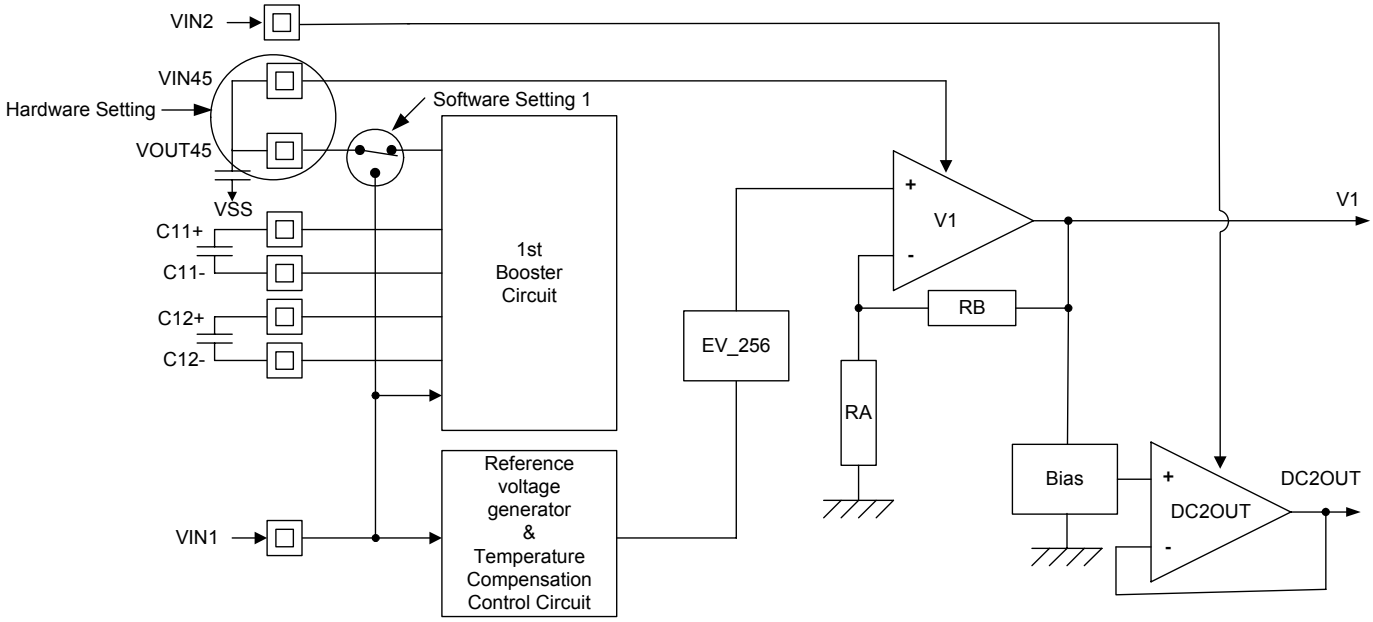
DC(1) : In normal mode partial mode 0			**Operating voltage range**
DB1	**DB0**	**DC-DC step up**	**VIN1**
0	**0**	**X1.0**	**2.4~3.6[V]**
0	**1**	**X1.5**	**2.4~3.6[V]**
1	**0**	**X2.0**	**2.4~3.0[V]**
1	**1**	**X2.0**	**2.4~3.0[V]**

DC-DC Select and power supply for V1 Op-Amp.

Even if VIN45 is connected to VOUT45 or VIN1, a setup by software must be able to be performed. Power supply for V1 Op-Amp. Is decided by Hardware setting and Software setting.

The example of usage is shown below.

Figure28. Example : Hardware Setting : VIN45 connected to VOUT45
Software Setting 1 : Power supply for V1 Op.Amp. uses 1'st booster output (not VIN1).



Hardware setting: VIN45 connected to (1) VOUT45 (when VOUT45 is used)
(2) VIN1 (when VOUT45 is not used)

Instruction setting: DC-DC Select (20H) – DC Register
Set value “00” Power supply for 1’st booster output uses 1XVIN1. (Initial status)
Set value “01” Power supply for 1’st booster output uses 1.5XVIN1.
Set value “10” or “11” Power supply for 1’st booster output uses 2XVIN1.

Software setting 1: DC/DC and AMP ON/OFF (26H) – DCDC1 Register
Set value “0” Power supply for VOUT45 uses VIN1. (Initial status)
Set value “1” Power supply for VOUT45 uses 1’st booster output.

Bias Set (22H)

This instruction set up the value of bias in normal mode and in partial mode.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB9	DB1	DB0
0	0	1	0	0	1	0	0	0	1	0
			0	0	Bias(2)		0	0	Bias(1)	

Bias(1): Bias value selecting in normal mode and partial mode0.
Bias(2): Bias value selecting in partial mode1.

Bias(2): In partial mode 1				
DB5	DB4	Bias	DCDC2 step up	DC2OUT
0	0	1/4	X(-3)	3/4xV1
0	1	1/5	X(-3)	V1
1	0	1/6	X(-4)	5/6xV1
1	1	1/7	X(-4)	V1

Bias(1):In normal, partial mode 0				
DB1	DB0	Bias	DCDC2 step up	DC2OUT
0	0	1/4	X(-3)	3/4xV1
0	1	1/5	X(-3)	V1
1	0	1/6	X(-4)	5/6xV1
1	1	1/7	X(-4)	V1

DCDC Clock Division Set(24H)

This instruction sets the internal booster clock frequency.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	1	0	0
			0	0	DIV(2)		0	0	DIV(1)	

DIV(1) : DC-DC Charge Pump Division Ratio in Normal Mode Display and Partial Display Mode0
- DIV(1) = 10 (Initial status)

DIV(2) : Division Ratio in Partial Display Mode1
- DIV(2) = 10 (Initial status)

DB5	DB4	DIV(2)	
0	0	fPCK = fOSC_P/8	fPCK1 = fOSC_P/4
0	1	fPCK = fOSC_P/16	fPCK1 = fOSC_P/8
1	0	fPCK = fOSC_P/32	fPCK1 = fOSC_P/16
1	1	fPCK = fOSC_P/64	fPCK1 = fOSC_P/32

DB1	DB0	DIV(1)	
0	0	fPCK = fOSC/16	fPCK1 = fOSC/8
0	1	fPCK = fOSC/32	fPCK1 = fOSC/16
1	0	fPCK = fOSC/64	fPCK1 = fOSC/32
1	1	fPCK = fOSC/128	fPCK1 = fOSC/64

Note:1. fPCK1 : 1st booster boosting frequency, fPCK : 2nd,3rd booster boosting frequency

2. fOSC : (ROUNDUP (Duty/3) + dummy) x 4 x 16 x frame frequency
3. fOSC_P : Oscillation frequency in Partial Display Mode1.
   In Partial Display Mode1, oscillation frequency is set by PF<1:0> pin or Partial mode1 frequency control command (37h).

DC/DC and AMP ON/OFF Set (26H)

This instruction set up the DC/DC and Op-amp in common start up setting.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	1	1	0
			0	0	0	0	AMP	DCDC3	DCDC2	DCDC1

AMP: Built-in OP-AMP ON/OFF.
- AMP=0: OP-AMP OFF (Initial status)
- AMP=1: OP-AMP ON

DCDC1: Built-in 1'st Booster ON/OFF
- DCDC1= 0: 1'st Booster OFF (Initial status)
- DCDC1= 1: 1'st Booster ON

DCDC2: Built-in 2'nd Booster ON/OFF
- DCDC2= 0: 2'nd Booster OFF (Initial status)
- DCDC2= 1: 2'nd Booster ON

DCDC3: Built-in 3'rd Booster ON/OFF
- DCDC3= 0: 3'rd Booster OFF (Initial status)
- DCDC3= 1: 3'rd Booster ON

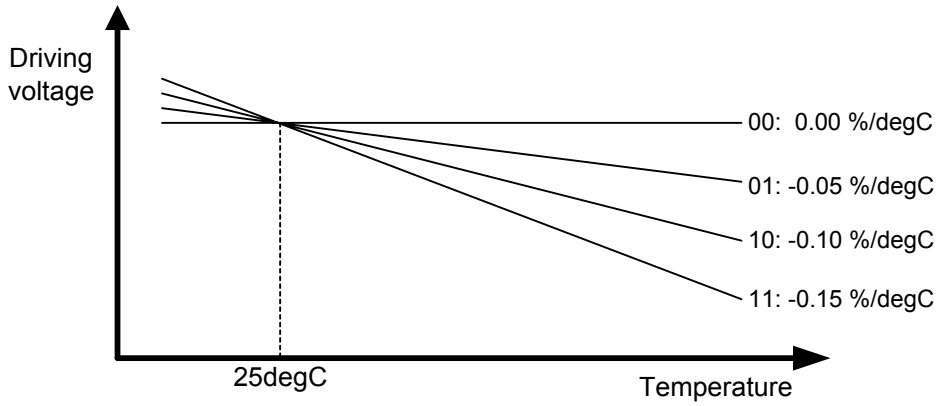
Temperature Compensation Set (28H)

This Instruction sets up the driving voltage slope for temperature compensation.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	0	0	0
			0	0	0	0	0	0	TCS	

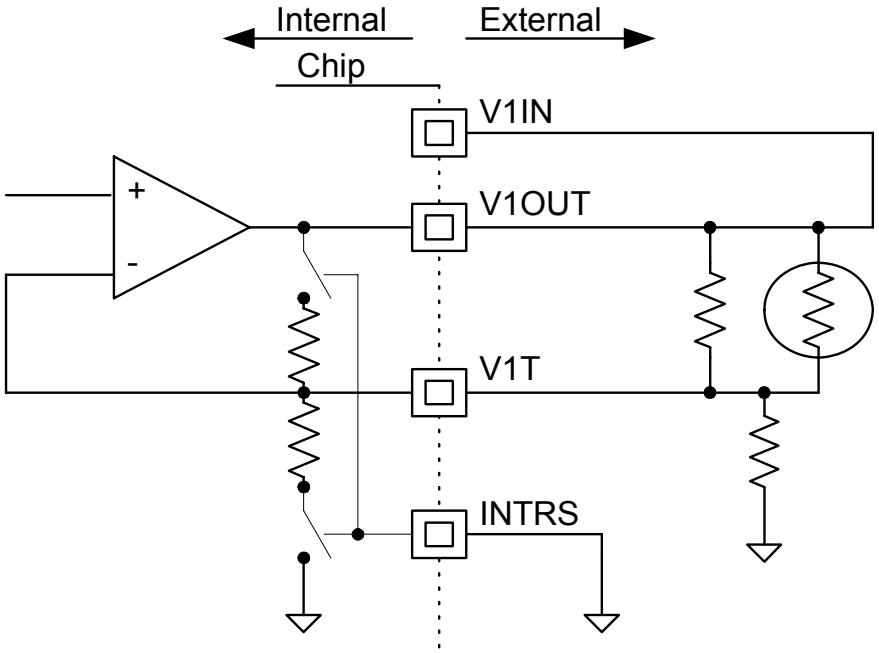
TCS: Temperature compensation slope set
- TCS = 00 : 0.00%/degC (Initial status)
- TCS = 01 : -0.05%/degC
- TCS = 10 : -0.10%/degC
- TCS = 11 : -0.15%/degC

TCS Register Set *		Temp. Coefficient
DB1	DB0	
0	0	0.00%/°C
0	1	-0.05%/°C
1	0	-0.10%/°C
1	1	-0.15%/°C



Temperature Compensation's Example

If external temperature compensation is needed, circuit diagram is described as below.
To use temperature compensation, two resistors and one thermistor are needed.



Contrast Control (1) (2AH)

This instruction updates the contrast control value in normal display mode and partial display mode 0.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	0	1	0
			Contrast control value (0 to 255)							

The relation between V1 voltage (typ.) and Contrast(1) set value (3bit step case)

Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]
00h	2.000	30h	2.376	60h	2.753	90h	3.129	C0h	3.506	F0h	3.882
08h	2.063	38h	2.439	68h	2.816	98h	3.192	C8h	3.569	F8h	3.945
10h	2.125	40h	2.502	70h	2.878	A0h	3.255	D0h	3.631	FFh	4.000
18h	2.188	48h	2.565	78h	2.941	A8h	3.318	D8h	3.694		
20h	2.251	50h	2.627	80h	3.004	B0h	3.380	E0h	3.757		
28h	2.314	58h	2.690	88h	3.067	B8h	3.443	E8h	3.820		

Contrast Control (2) (2BH)

This instruction updates the contrast control value in partial display mode 1.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	0	1	1
			Contrast control value (0 to 255)							

The relation between V1 voltage (typ.) and Contrast(2) set value (3 bit step case)

Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]
00h	2.000	30h	2.376	60h	2.753	90h	3.129	C0h	3.506	F0h	3.882
08h	2.063	38h	2.439	68h	2.816	98h	3.192	C8h	3.569	F8h	3.945
10h	2.125	40h	2.502	70h	2.878	A0h	3.255	D0h	3.631	FFh	4.000
18h	2.188	48h	2.565	78h	2.941	A8h	3.318	D8h	3.694		
20h	2.251	50h	2.627	80h	3.004	B0h	3.380	E0h	3.757		
28h	2.314	58h	2.690	88h	3.067	B8h	3.443	E8h	3.820		

Note :
S6B33BL has a hardware protection for “2VR < 20V”. It means the limitation of contrast value in each bias.
If 1/6 bias is set, max contrast value is limited to A9h, and if 1/7 bias is set, max contrast value is limited to 6Dh.

Standby Mode OFF (2CH)

This instruction releases the standby mode.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	1	0	0

The internal statuses during standby off are as following:

- All common output: VRP or VRN or VM or VSS
- All segment output: VSS or V1
- Oscillator circuit: On (EXT = 0, OSC=1), OFF (others)
- Displaying clocks (FR, PM, CL): In operation

Function and Pin condition at standby OFF

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	ON(Operate)
COM outputs	VRP or VM or VSS or VRN
SEG outputs	V1 or VSS

Standby Mode ON (2DH)

This instruction enters the standby mode to reduce the power consumption to the static power consumption value (Initial status). The following instructions, standby off and display on, cause returning to the normal operation status.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	1	0	1

The internal statuses during standby on are as following:

- All common and segment output: VSS
- Oscillator circuit: OFF
- Displaying clocks (FR, PM, CL) are held.

Function and Pin condition at standby ON

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	OFF
SEG and COM outputs	VSS

LCD driving power output condition at Standby ON.

Level	Condition
VRP	VSS
V1	VSS
VM	VSS
VRN	VSS

Addressing Mode Set (30H)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	0	0	0
			0	GSM		DSG	SGF	SGP		SGM

GSM: Gray Scale Mode
- 00: 65,536 color mode (Initial status)
- 01: 4,096 color mode (refer to “Data Format Select (60H/61H)”)
- 10: 256 color mode
- 11: 256 color mode

Note : 256 color mode only supports 8bit access mode.(refer to “Display Data Write/Read”)

DSG: Duty Adjust Setting
- 0: Dummy subgroup is one subgroup
- 1: Dummy subgroup is none (Initial status)

SGF: Sub Group Frame Inversion mode setting
- 0: SG Frame inversion OFF
- 1: SG Frame inversion ON (Initial status)

SGM: Sub Group inversion mode setting
- 0: SG inversion OFF
- 1: SG inversion ON (Initial status)

SGP: Sub Group Phase mode setting
- 00: Same phase in all pixels
- 01: Different phase by 1pixel-unit
- 10: Different phase by 2pixel-unit (Initial status)
- 11: Different phase by 4pixel-unit

Row Vector Mode Set (32H)

Setting ROW function.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	0	1	0
			0	0	0	0	INC			VEC

INC: Row Vector Increment Mode. This Parameter set up Row vector increment period

DB3	DB2	DB1	Row Vector Increment Period
0	0	0	Every subgroup
0	0	1	Every 2subgroup
0	1	0	Every 4subgroup
0	1	1	Every 8subgroup
1	0	0	Every 16subgroup
1	0	1	Every 16subgroup
1	1	0	Every 16subgroup
1	1	1	Every sub-frame (initial status)

VEC: ROW Vector Sequence Mode
- 0: R1->R2->R3->R4 -> R1… (Initial status)
- 1: R1->R3->R2->R4 -> R1...

N-block inversion Set (34H)

This instruction set up N block inversion for AC driving.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	1	0	0
			FIM	FIP	0	N-block inversion				

FIM: Forcing Inversion Mode
FIM = 0: Forcing Inversion OFF
FIM = 1: Forcing Inversion ON (Initial status)
FIP: Forcing Inversion Period
FIP = 0: Forcing Inversion Period is one frame (Initial status)
FIP = 1: Forcing Inversion Period is two frame
N-block Inversion: This parameter indicates the basic period of polarity inversion.
The whole period of polarity inversion is decided by FIM, FIP and this parameter.
(Initial status: 01101)

DB7	DB6	DB5	DB4 – DB0	Polarity Inversion Period
x	X	x	0	every frame
0	X	x	1	every 1 block
:	:	:	:	:
0	X	x	31	every 31 blocks
1	0	x	1	every 1 block and every frame
:	:	:	:	:
1	0	x	31	every 31 blocks and every frame
1	1	x	1	every 1 block and every 2 frames
:	:	:	:	:
1	1	x	31	every 31 blocks and every 2 frames

Frame Frequency Control (36H)

This instruction controls the internal frame frequency.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	1	1	0
			0	0	0	0	0	0	0	LFS

LFS: Low frame frequency set for low power consumption.
LFS = 0 : Low frequency set OFF (Initial status)
LFS = 1 : Low frequency set ON

Note : fFR @(LFS=1) = fFR @(LFS=0) / 2

Partial mode1 frequency control (37H)

Setting oscillation frequency in partial mod1

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	1	1	1
			0	0	0	0	0	CMD_ SEL	PDMD1_SEL	

CMD_SEL : Partial mode1 oscillation frequency can be set by hardware or software.
CMD_SEL=0 : Partial mode1 oscillation frequency is set by PF[1:0] pin. (initial status)
CMD_SEL=1 : Partial mode1 oscillation frequency is set by PDMD1_SEL[1:0].

PDMD1_SEL : When CMD_SEL=1, this parameter set oscillation frequency in partial mode1.

PDMD1_SEL[1:0]	Partial mode 1 OSC frequency
00	fOSC / 2
01	fOSC / 3 (initial status)
10	fOSC / 4
11	fOSC / 5

Note : fOSC is a oscillation frequency generated by CR oscillator.

256 Color Mode Palettes

At 256-color mode, the instruction and parameter below set each Gray Scale level of the Red/Green/Blue. Gray scale level is determined by GS data.

Red Palette (38H)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	1	0	0	0
			0	0	GS data “000” to RAM data					
			0	0	GS data “001” to RAM data					
			0	0	GS data “010” to RAM data					
			0	0	GS data “011” to RAM data					
			0	0	GS data “100” to RAM data					
			0	0	GS data “101” to RAM data					
			0	0	GS data “110” to RAM data					
			0	0	GS data “111” to RAM data					

Green Palette (3AH)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	1	0	1	0
			0	GS data “000” to RAM data						
			0	GS data “001” to RAM data						
			0	GS data “010” to RAM data						
			0	GS data “011” to RAM data						
			0	GS data “100” to RAM data						
			0	GS data “101” to RAM data						
			0	GS data “110” to RAM data						
			0	GS data “111” to RAM data						

Blue Palette (3CH)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	1	1	0	0
			0	0	GS data “00” to RAM data					
			0	0	GS data “01” to RAM data					
			0	0	GS data “10” to RAM data					
			0	0	GS data “11” to RAM data					

Initial value for each Palette

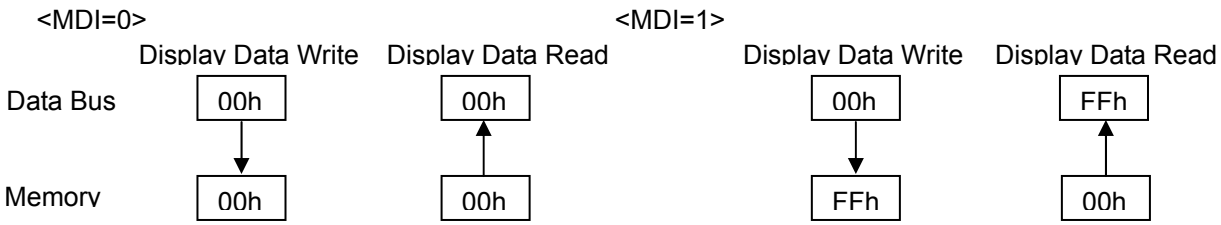
Gray Scale Data	Initial Gray Scale Level		
	Red	Green	Blue
000	0	0	0
001	12	24	14
010	14	28	18
011	16	32	31
100	18	36	-
101	20	40	-
110	24	44	-
111	31	63	-

Entry Mode Set (40H)

Setting internal function mode.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	0	0
			0	0	0	0	0	MDI	X/Y	RMW

MDI: Memory data inversion setting for low power consumption.
MDI = 0: Memory data inversion OFF (Initial status)
MDI = 1: Memory data inversion ON



X/Y: Memory address counter mode setting
X/Y = 0: Y address counter mode (Initial status)
X/Y = 1: X address counter mode

RMW: Read modify write mode ON/OFF select
RMW = 0: Read modify write OFF (Initial status)
RMW = 1: Read modify write ON. When this mode is on, X(Y) address of on-chip display RAM is not increment in reading display data but in writing display data.

X Address Area Set (42H)

This instruction and parameter set up the X address areas of the on-chip display data RAM.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	1	0
			X start address set (Initial Status = 00H)							
			X end address set (Initial Status = A1H)							

The current X address of the on-chip display data RAM is the X start address by setting this instruction. In X address count mode (X/Y = “H”), the X address is increased from X start address to X end address. When X address is equal to the X end address, the Y address is increased by 1 and the X address returns to X start address. The X start and X end addresses must be set as a pair and X start address must be less than X end address.

Y Address Area Set (43H)

This instruction and parameter set up the Y address areas of the on-chip display data RAM.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	1	1
			Y start address set (Initial Status = 00H)							
			Y end address set (Initial Status = 83H)							

The current Y address of the on-chip display data RAM is the Y start address by setting this instruction. In Y address count mode (X/Y = "L"), the Y address is increased from Y start address to Y end address. When Y address is equal to the Y end address, the X address is increased by 1 and the Y address returns to Y start address. The Y start and Y end address must be set as a pair and Y start address must be less than Y end address.

RAM Skip Area Set (45H)

This instruction and parameter set up the X address areas of the on-chip display data RAM.

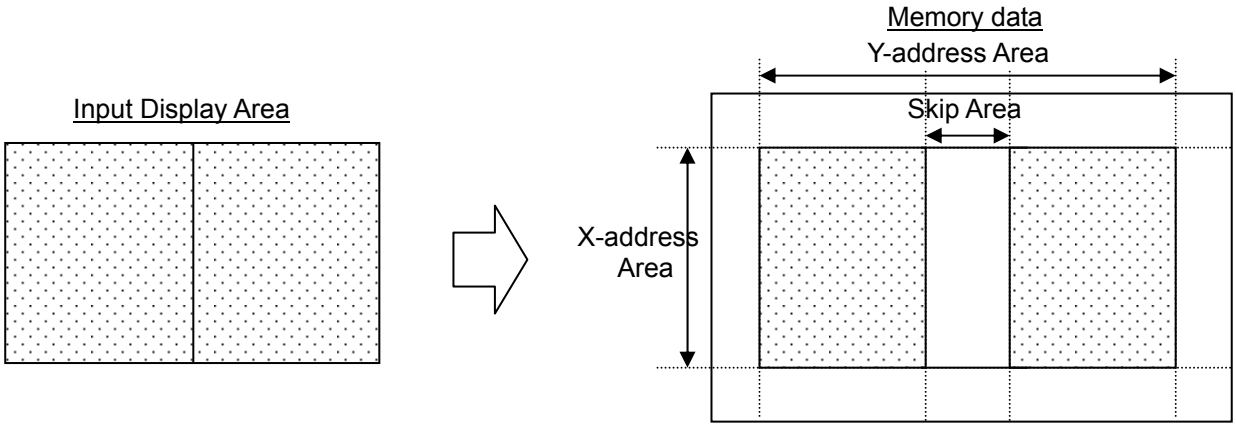
RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	0	1
			0	0	0	0	0	0	RSK	

RSK : RAM Skip function ON/OFF set

- RSK = 00 : No Skip
- RSK = 01 : Y address 40h – 43h skip(128 RGB)
- RSK = 10 : Y address 3Ch – 47h skip(120 RGB)
- RSK = 11 : Y address 30h – 53h skip(96 RGB)

RAM Skip Area Set

RAM Skip Area Set can skip a part of RAM Y-address area. After setting RAM skip area, Y-address count skip this area and count. In other words, Y address after skip area is changed into Y address which added a part for skip area.



Display OFF (50H)

Turn the display OFF(Initial status).
When display is off, all segment and common output are VSS level.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	0

Function and Pin condition at Display OFF

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	ON(Operate)
SEG and COM outputs	VSS

Display ON (51H)

Turns the display ON.
In case of being standby mode, this instruction does not work. This instruction is executed after standby mode off.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	1

Function and Pin condition at Display ON

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	ON(Operate)
COM outputs	VRP or VM or VRN
SEG outputs	V1 or VSS

Specified Display Pattern Set (53H)

This instruction sets the specified display pattern.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	1	1
			0	0	0	0	0	0	SDP	

SDP : Specified Display Pattern set
- SDP = 00 : Normal display
- SDP = 01 : Reverse display : Display data reversing mode setting without the contents of the display RAM
- SDP = 10 : Whole display pattern becomes OFF regardless of the RAM data.
- SDP = 11 : Whole display pattern becomes ON regardless of the RAM data.

Partial Display Mode Set (55H)

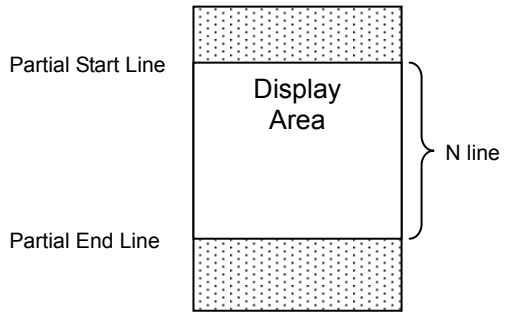
RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	0	1
			0	0	0	0	0	0	PDM	PT

PT: Partial Display ON/OFF
- PT = 0: Partial display OFF = Normal mode (Initial status)
- PT = 1: Partial display ON

PDM: Partial Display mode set
- PDM = 0: Partial mode 0 : Duty ratio is same as Normal display mode(initial status)
- PDM = 1: Partial mode 1 : Duty ratio is changed from Normal display mode
  (DSG = 0 : 69 line fixed(including 1 dummy subgroup),
  DSG = 1 : 66 line fixed(no dummy subgroup))

Applied parameter in PDM0 and PDM1 are summarized as below

PDM	Contrast	Duty	Bias	DC-DC Select	OSC	PCK
0	Contrast control(1)	Normal	Bias(1)	DC(1)	OSC1-OSC2	DIV(1)
1	Contrast control(2)	1/69	Bias(2)	DC(2)	Set by PF<1:0>	DIV(2)



No display Area : No COM Scanning field (COM = Vm fixed)
Except Partial Display Area : COM Timing is existing, but COM = Vm fixed
Partial Display Area : Real display field

Operation in Partial Display Mode 0 (PDM=0)

On scanning except partial display area
- SEG output select V0 or V1 level depend on “FR” value. Refer to Page56.
- All of COM output is fixed VM level.

On scanning partial display area
- It is equal to be in normal mode

Operation in Partial Display Mode 1 (PDM=1)

Display area is from partial start line to partial end line.
(COM driver output is fixed VM except display area, only max69 line output COM signal.

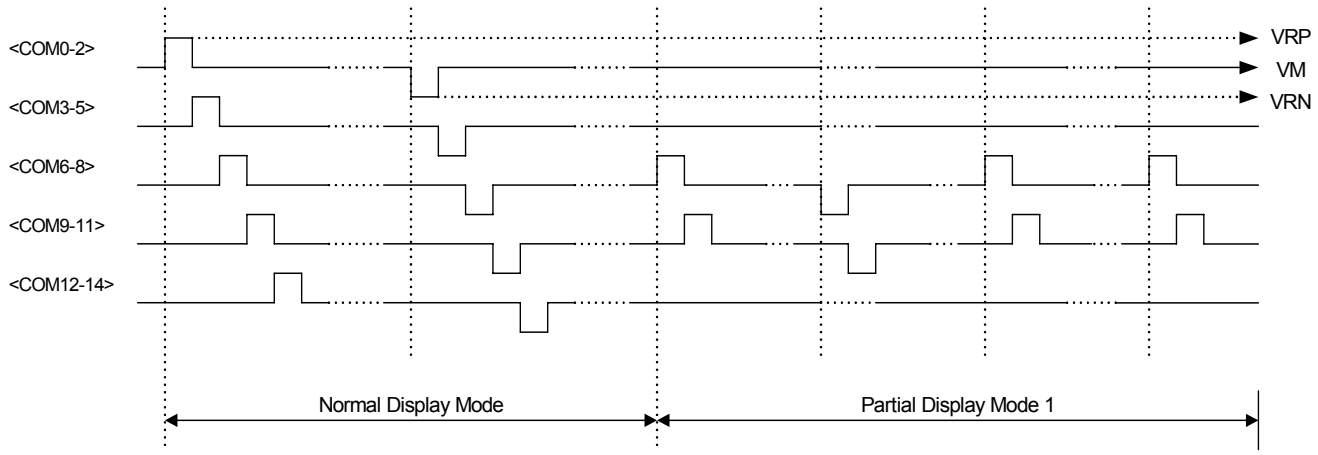
On scanning except partial display area
- SEG output select V0 or V1 level depend on “FR” value. Refer to Page56.
- All of COM output is fixed VM level.

On scanning partial display area
- It is equal to be in normal mode

Partial Display Mode0

Item	Partial Display Area	Out of Partial Display Area
Duty	Same as normal display mode	
Bias	Same as normal display mode (Bias(1) setting)	
Contrast	Same as normal display mode (Contrast(1) setting)	
Oscillator	Same as normal display mode (OSC1 – OSC2)	
SEG Output level	Same as normal mode (V1,V0)	Depends on Internal “FR” signal See page 56
COM Output level	Same as normal mode (VRP,VM,VRN)	VM fixed

In case of COM 6 to COM11 Partial display



Partial display mode1

Item	Partial Display Area	Out of Partial Display Area	Out of Display Area
Duty	1/66duty		
Bias	Bias(2) setting		
Contrast	Contrast(2) setting		
Oscillator	Oscillation frequency is set by PF<1:0>		
SEG Output level	Same as normal mode (V1,V0)	Depends on “FR” signal See page 56	-
COM Output level	Same as normal mode (VRP, VM, VRN)	VM fixed	VM fixed

Partial Display Start Line Set (56H), Partial Display End Line Set(57H)

These 2 instructions set the partial display area and it is possible to display a part as 3-lines unit.

Partial Display Start Line Set (56H)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1	0
			Partial start line							

EX) Partial start line : 0, 3, 6, 9, …, 156, 159 (3 Lines step)

CDIR = 0		CDIR = 1
COM 0	line 0	COM 161
COM 1	Setting disable	COM 160
COM 2	Setting disable	COM 159
COM 3	line 3	COM 158
	:	
	:	
	:	
COM 158	Setting disable	COM 3
COM 159	line 159	COM 2
COM 160	Setting disable	COM 1
COM 161	Setting disable	COM 0

Partial Display End Line Set (57H)

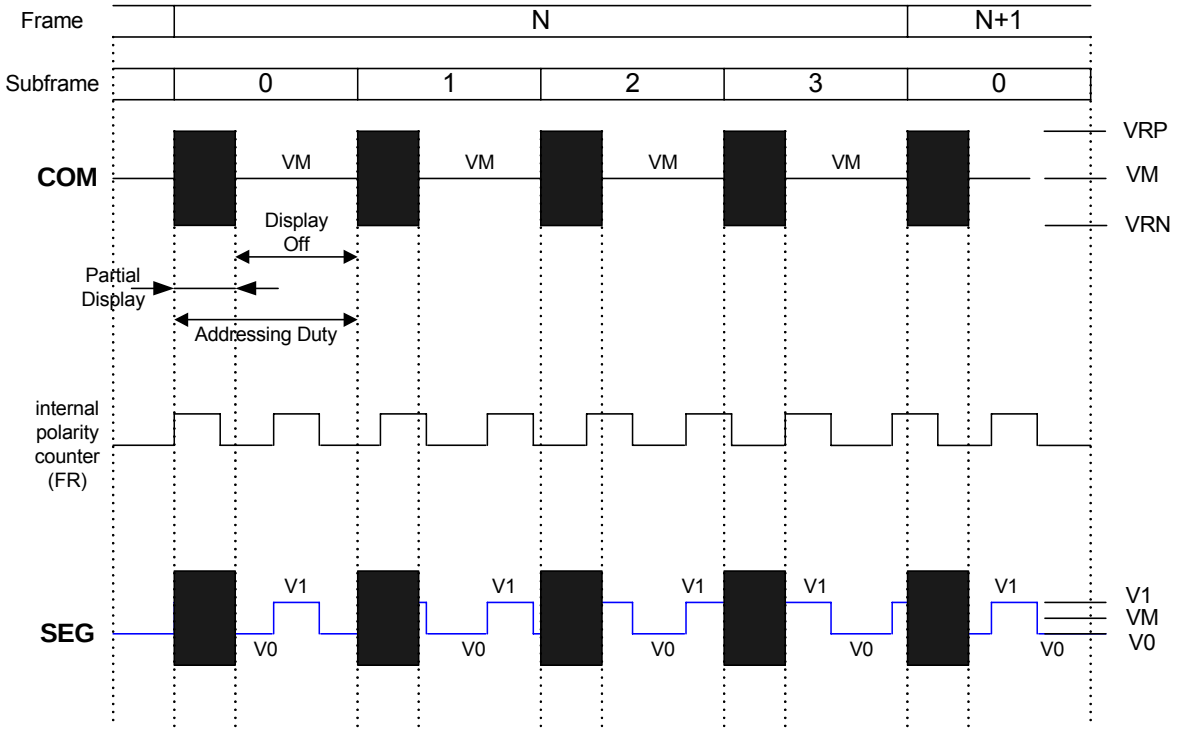
RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1	1
			Partial end line							

EX) Partial end line : 2, 5, 8, 11, …, 158, 161 (3 Lines step)

CDIR = 0		CDIR = 1
COM 0	Setting disable	COM 161
COM 1	Setting disable	COM 160
COM 2	line 2	COM 159
COM 3	Setting disable	COM 158
	:	
	:	
	:	COM 3
		COM 2
COM 158	line 158	COM 1
COM 159	Setting disable	COM 0
COM 160	Setting disable	
COM 161	line 161	

Parameter set appoints display line number. At PDM 0, Parameter size is able to be set as 3-line unit. But that is not able to be over max 69 line at PDM 1. Partial end line must set bigger number than Partial start line.

Example of Segment Voltage in non-display area



Area scroll Set (59H)

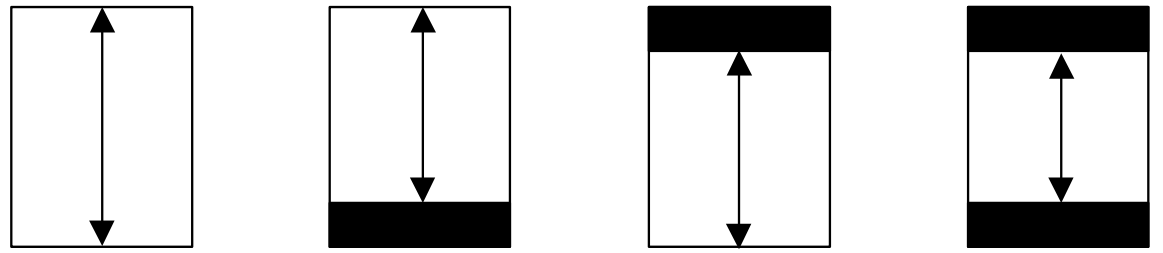
This instruction sets up area scroll field (start line, end line, Lower fixed line number), and it is possible to make screen to display as partial scroll field.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	0	1
			0	0	0	0	0	0	SCM	
			Scroll area start line							
			Scroll area end line							
			Lower fixed number							

Note : In lower and center scroll mode, scroll area end line must be smaller than (duty – lower fixed number).

SCM: Scroll mode setting

DB1	DB0	Mode
0	0	Entire display(Initial status)
0	1	Upper scroll display
1	0	Lower scroll display
1	1	Center scroll display



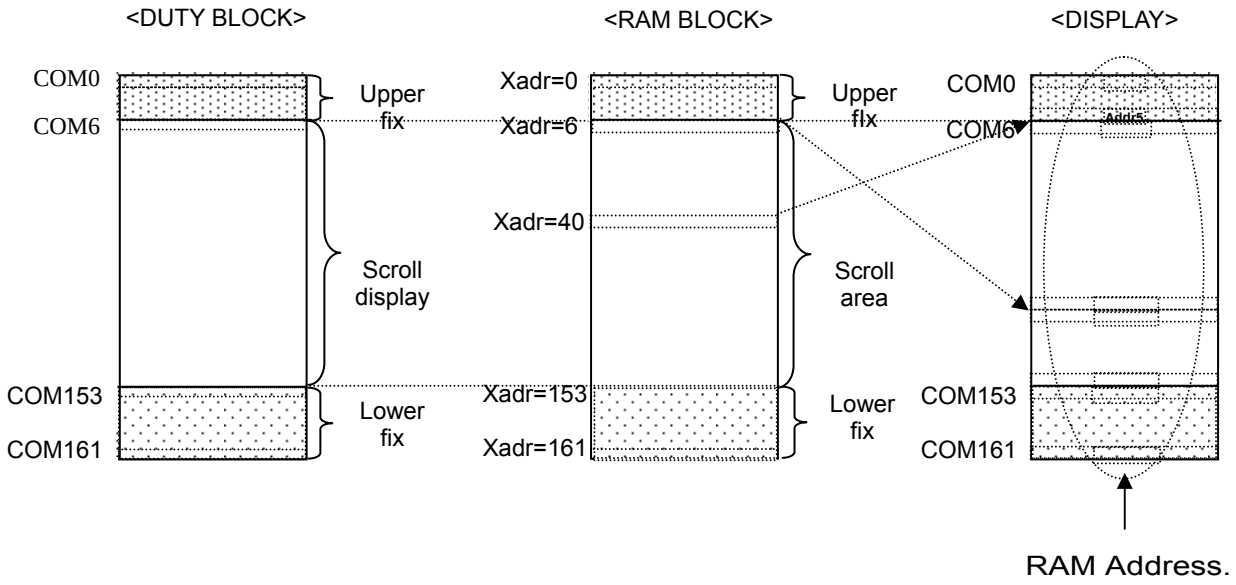
Scroll Start Line Set (5AH)

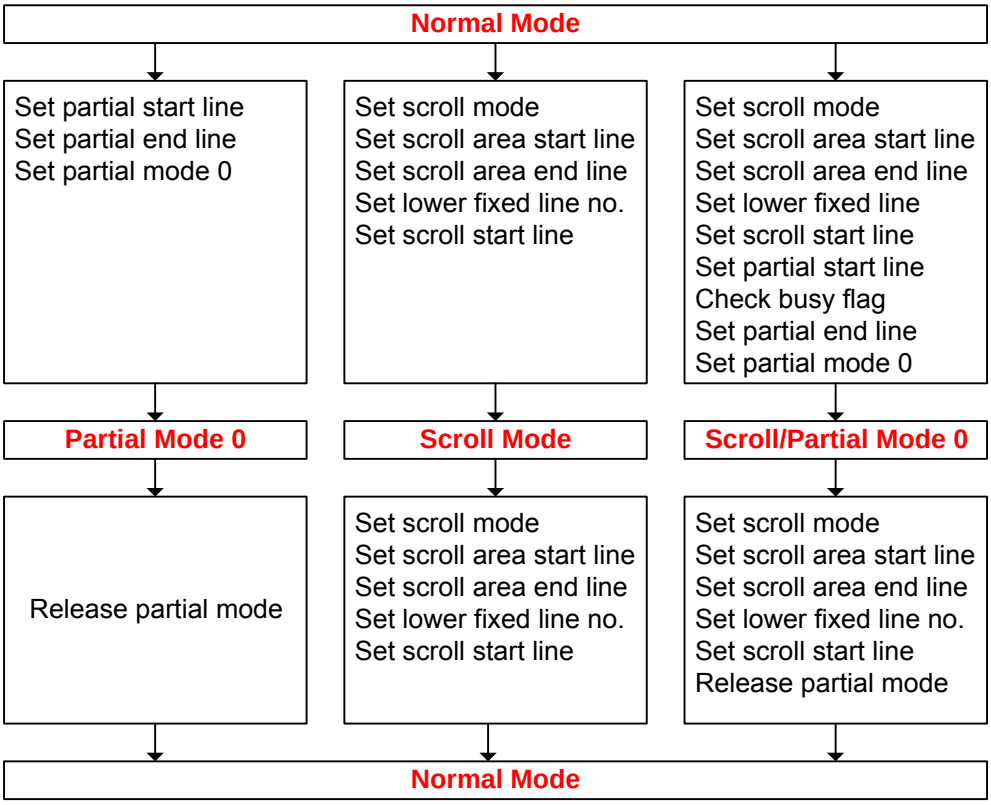
This instruction and parameter set up scroll start line. On this instruction, scroll start line becomes the first of area scroll field. Scroll operation is occurred every issue of this instruction.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	1	0
			Scroll start line							

<Example>

-DLN : 2'b10 (1/162 duty)
-SCM : 2'b11 (Center display mode)
-Scroll area start line : 6
-Scroll area end line : 152
-Lower fixed number : 9
-Scroll start line : 40





Data Format Select (60H/61H)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	0	0	0	0	DFS

DFS: 4,096 Color Mode Data Format Select
- 0 : 4,096 Color Data Format A (Initial Status)
  - 8 bit mode :
    - DB[7:0] : XXXXRRRR (1'st write)
    - DB[7:0] : GGGGBBBB(2'nd write)
  - 16 bit mode :
    - DB[15:0] :XXXXRRRRGGGGBBBB (12 bit)
- 1 : 4,096 Color Data Format B
  - 8 bit mode :
    - DB[7:0] : RRRRGGGG(1'st write)
    - DB[7:0] : BBBBXXXX(2'nd write)
  - 16 bit mode :
    - DB[15:0] :RRRRGGGGBBBBXXXX (12 bit)

Display Data Write/Read

RS	WRB	RDB	DB15 ~ DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	Display RAM write in data								
1	1	0	Display RAM read out data								

GSM = 00(65,536 Color Mode)

(1) 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1'st cycle	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
2'nd cycle	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

(2) 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	R4	R3	R2	R1	R0	G5	G4	G3
2'nd cycle	G2	G1	G0	B4	B3	B2	B1	B0
3'rd cycle	R4	R3	R2	R1	R0	G5	G4	G3
4'th cycle	G2	G1	G0	B4	B3	B2	B1	B0

GSM = 01(4,096 Color Mode), DFS = 0

(1) 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1'st cycle	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0
2'nd cycle	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0

(2) 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	X	X	X	X	R3	R2	R1	R0
2'nd cycle	G3	G2	G1	G0	B3	B2	B1	B0
3'rd cycle	X	X	X	X	R3	R2	R1	R0
4'th cycle	G3	G2	G1	G0	B3	B2	B1	B0

GSM = 01(4,096 Color Mode), DFS = 1

(3) 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1'st cycle	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	X	X	X	X
2'nd cycle	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	X	X	X	X

(4) 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	R3	R2	R1	R0	G3	G2	G1	G0
2'nd cycle	B3	B2	B1	B0	X	X	X	X
3'rd cycle	R3	R2	R1	R0	G3	G2	G1	G0
4'th cycle	B3	B2	B1	B0	X	X	X	X

GSM = 10 or 11 (256 Color Mode)

- 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	R2	R1	R0	G2	G1	G0	B1	B0
2'nd cycle	R2	R1	R0	G2	G1	G0	B1	B0

Status Read

MTP_RD = 0: Normal Status Read (Initial status)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	BSY	X/Y	MPRT	PDM	PT	STB	REV	DP

This instruction indicates the internal status of the S6B33BL.

DP: (0 : Display OFF Status, 1 : Display ON Status)
REV: (0 : Display Image Non-Reversing, 1 : Display Image Reversing)
STB: (0 : Standby Mode OFF Status, 1 : Standby Mode ON Status)
PT: (0 : Partial Display Mode OFF Status, 1 : Partial Display Mode ON Status)
PDM: (0 : Partial Display Mode 0, 1 : Partial Display Mode 1)
MPRT: (0: MTP mode non-protection status, 1: MTP mode protection status)
X/Y: (0 : Y-address Count Mode, 1 : X-address Count Mode)
BSY: (0 : No Busy, 1 : Busy)

MTP_RD = 1: MTP Status Read

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	MPRT	MOV5	MOV4	MOV3	MOV2	MOV1	MOV0

Test Key Command (8CH)
This instruction sets MTP cell can be written or erased.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	0	1	1	0	0

Test Key Command Disable(8DH)
This instruction sets MTP cell can not be written or erased.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	0	1	1	0	1

MTP Load (E5H)
This command is used to load MTP cell.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	1	0	1

This command is valid at standby ON.

MTP Initial Disable (E8H)
MTP cell turns initial mode off. (initial status)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	0	0	0

MTP Initial Enable (E9H)
MTP cell turns initial mode on.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	0	0	1

MTP Mode Off (EAH)
This instruction sets MTP mode off.

RS	RW_WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	0	1	0

MTP Mode On (EBH)
This instruction sets MTP mode on. (Initial status)

RS	RW_WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	0	1	1

MTP Read Mode (E6H)
This instruction sets MTP cell can be read.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	1	1	0
			0	0	0	0	0	0	0	MTP_RD

MTP_RD: MTP Read Mode
- MTP_RD = 0: Normal Status Mode (Initial status)
- MTP_RD = 1: MTP Status Mode

Offset Volume Set (EDH)

This instruction sets offset value x (-32 to +31) to electronic volume by 2s complement.

RS	RW_WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	0	1
0	0	0	0	P15	P14	P13	P12	P11	P10

0 : MTP cell is able to be programmed
1 : MTP cell isn't able to be programmed

P15	P14	P13	P12	P11	P10	Offset Volume(x)
0	1	1	1	1	1	31
:	:	:	:	:	:	
0	0	0	0	0	1	1
0	0	0	0	0	0	0
1	1	1	1	1	1	-1
	:	:	:	:	:	:
1	0	0	0	0	0	-32

MTP Write Disable (EEH)

RS	RW_WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

MTP Write Enable (EFH)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	1	1	1

INSTRUCTION PARAMETER

Table 16. Instruction Parameter

Instruction	Hex	Para.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Oscillation Mode Set	02H	1	0	0	0	0	0	0	EXT	OSC
			Initial value (00h)							
Driver Output Mode Set	10H	1	0	0	DLN		0	SDIR	SWP	CDR
			Initial value (00h)							
Monitor Signal Control	18H	1	0	0	0	0	0	PM	CL	FR
			Initial value (00h)							
DC-DC Set	20H	1	0	0	0	0	DC(2)		DC(1)	
			Initial value (00h)							
Bias Set	22H	1	0	0	Bias(2)		0	0	Bias(1)	
			Initial value (00h)							
DCDC Clock Division Set	24H	1	0	0	DIV(2)		0	0	DIV(1)	
			Initial value (22h)							
DCDC and AMP ON/OFF Set	26H	1	0	0	0	0	AMP	DCDC3	DCDC2	DCDC1
			Initial value (00h)							
Temperature Compensation Set	28H	1	0	0	0	0	0	0	TCS	
			Initial value (00h)							
Contrast Control (1)	2AH	1	Contrast control value in normal and partial display mode 0 (0 to 255)							
			Initial value (00h)							
Contrast Control(2)	2BH	1	Contrast control value in partial display mode 1(0 to 255)							
			Initial value (00h)							
Addressing Mode Set	30H	1	0	GSM		DSG	SGF	SGP		SGM
			Initial value (1Dh)							
ROW Vector Mode Set	32H	1	0	0	0	0	INC			VEC
			Initial value (0Eh)							
N-line Inversion Set	34H	1	FIM	FIP	0	N-block Inversion				
			Initial value (8Dh)							
Frame Frequency Control	36H	1	0	0	0	0	0	0	0	LFS
			Initial value (00h)							
Partial Mode1 Frequency control	37H	1	0	0	0	0	0	CMD_SEL	PDMD1_SEL	
			Initial value (01h)							
Entry Mode Set	40H	1	0	0	0	0	0	MDI	X/Y	RMW
			Initial value (00h)							
X-address Area Set	42H	2	X Start address set							
			Initial value (00h)							
			X end address set							
			Initial value (A1h)							
Y-address Area Set	43H	2	Y start address set							
			Initial value (00h)							
			Y end address set							
			Initial value (83h)							
RAM Skip Area Set	45H	1	0	0	0	0	0	0	RSK	
			Initial value (00h)							
Specified Display Pattern Set	53H	1	0	0	0	0	0	0	SDP	
			Initial value (00h)							
Partial Display Mode Set	55H	1	0	0	0	0	0	0	PDM	PT
			Initial value (00h)							
Partial Display Start Line Set	56H	1	Partial start line							
			Initial value (00h)							
Partial Display End Line Set	57H	1	Partial end line							

			Initial value (A1h)

Table 16. Instruction Parameter (Continued)

Instruction	Hex	Para.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Area Scroll Mode Set	59H	4	0	0	0	0	0	0	SCM	
			Initial value (00h)							
			Scroll area start line							
			Initial value (00h)							
			Scroll area end line							
			Initial value (A1h)							
			Lower Fixed number							
			Initial value (00h)							
Scroll Start Line Set	5AH	1	Scroll start line							
			Initial value (00h)							
MTP Read	E6H	1	0	0	0	0	0	0	0	MTP_RD
			Initial value (00h)							
Offset Volume Set	EDH	1	0	0	OV5	OV4	OV3	OV2	OV1	OV0
			Initial value (00h)							

RESET OPERATION

When RSTB becomes “L”, following procedure is occurred.

- X start address: 0, X end address: 161, - Y start address: 0, Y end address: 131
- Display OFF
- Read Modify Write Mode OFF
- Function Mode Set

MDI = 0: Memory Data Inversion OFF
OSC = 0: Oscillator OFF
EXT = 0: Internal Oscillator Mode
REV = 0: Reversing mode OFF
X/Y = 0: Y-address Count Mode
Standby Mode ON

- DCDC Clock Division Set

DIV(1) = 10: fPCK = fOSC/64
DIV(2) = 10: fPCK = fOSC/32

- Duty Set

Display Duty = 00: 1/132 duty

- DC-DC Select

DC(1) = 0: X1 step-up
DC(2) = 0: X1 step-up

- Bias Set

Bias(1) = 0H: 1/4 bias
Bias(2) = 0H: 1/4 bias

- DC/DC and AMP ON/OFF Set

AMP =0: Built-in OP-AMP OFF
DCDC1 =0: Built-in 1’st booster OFF
DCDC2 =0: Built-in 2’nd booster OFF
DCDC3 =0: Built-in 3’rd booster OFF

- N-block inversion

FIM =1: Forcing Inversion ON
FIP =0: Forcing Inversion Period in one frame
N-block inversion = 0DH: 13 block inversion

- Frame Frequency Control

LFS =0: Low Frequency Set OFF

- Partial Display Mode

PT = 0: Partial Display Mode OFF

- Partial Display Area Set

Partial start line = 00H
Partial end line = 81H

-Area Scroll Set

Mode = 00H : Entire Display Scroll Mode
Area Start Line: 00H
Area End Line: A1H
Lower Fixed Line Number: 00H

- Scroll Start Line Set

Scroll Start Line: 00H

- Addressing Mode Set

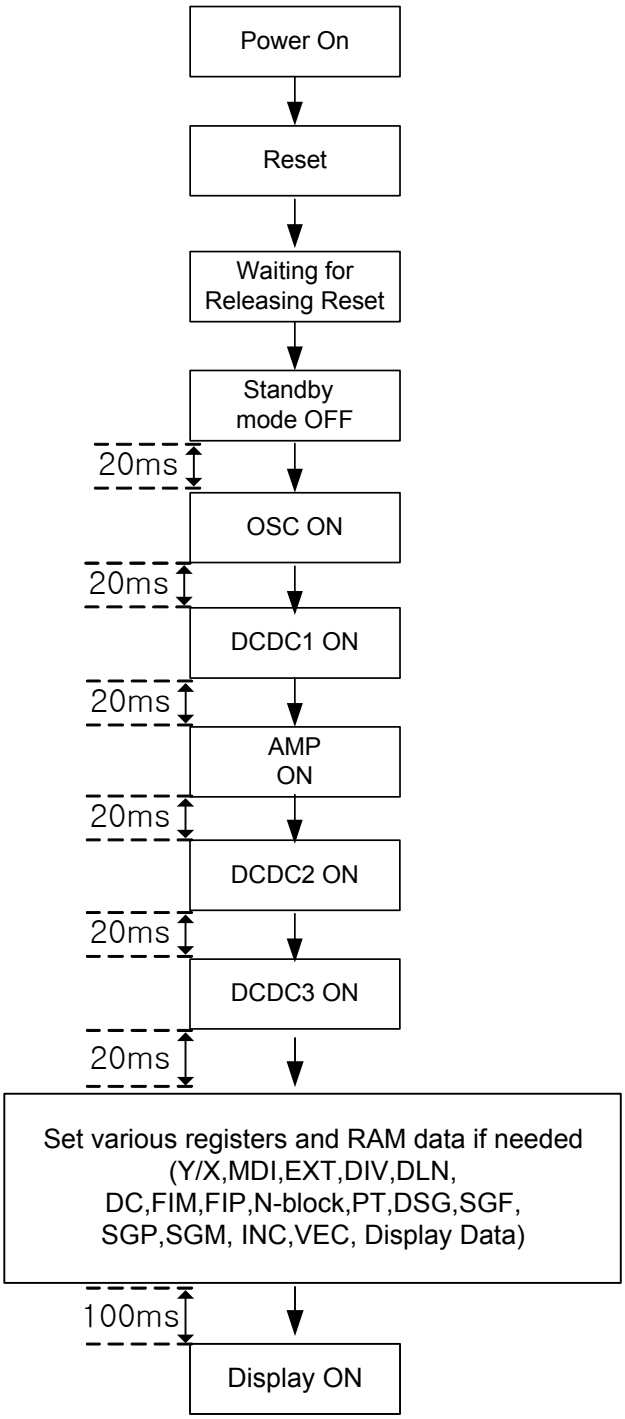
GSM=00: 65,536 Color Mode
DSG = 1: No dummy subgroup
SGF = 1: SG Frame Inversion ON
SGM = 1: SG Inversion Mode ON
SGP=10: Different phase by 2pixel-unit

- Row Vector Mode Set

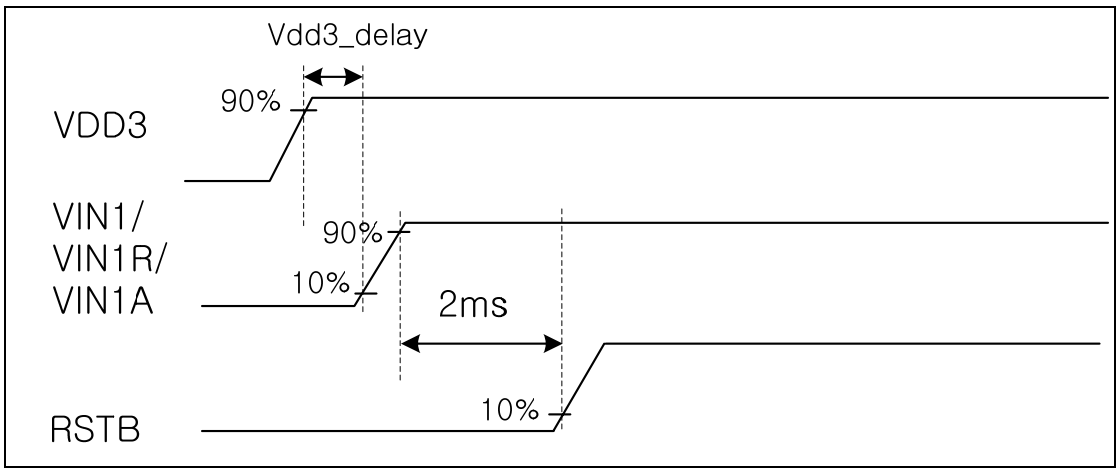
INC =111: Increment every sub-frame
VEC=0: R1->R2->R3->R4->R1->…

POWER ON/OFF SEQENCE

POWER ON SEQUENCE

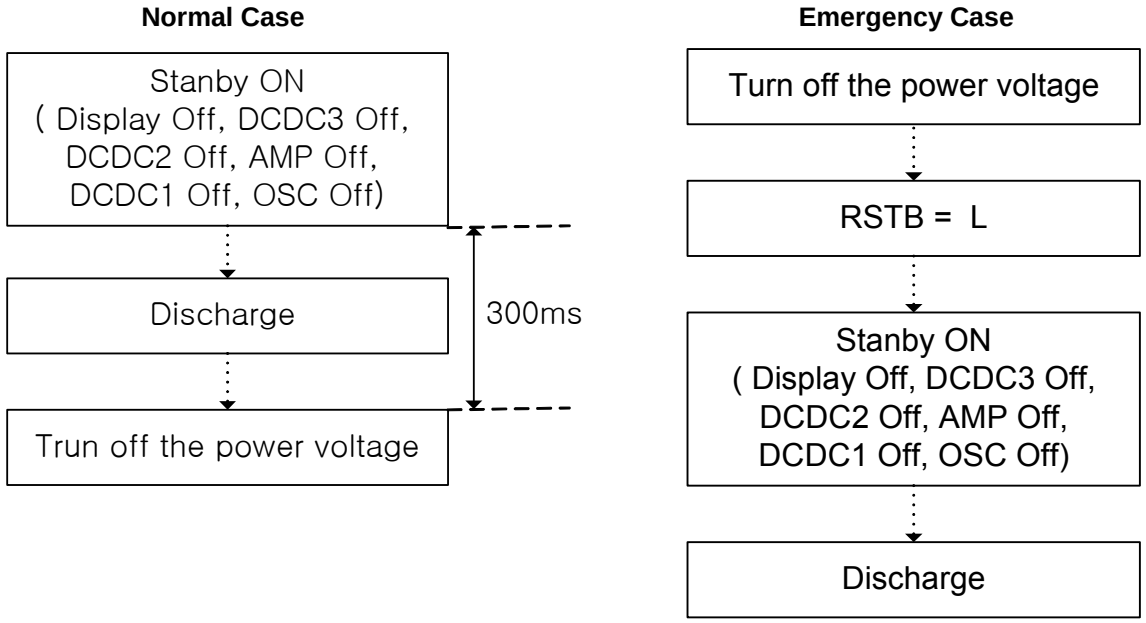


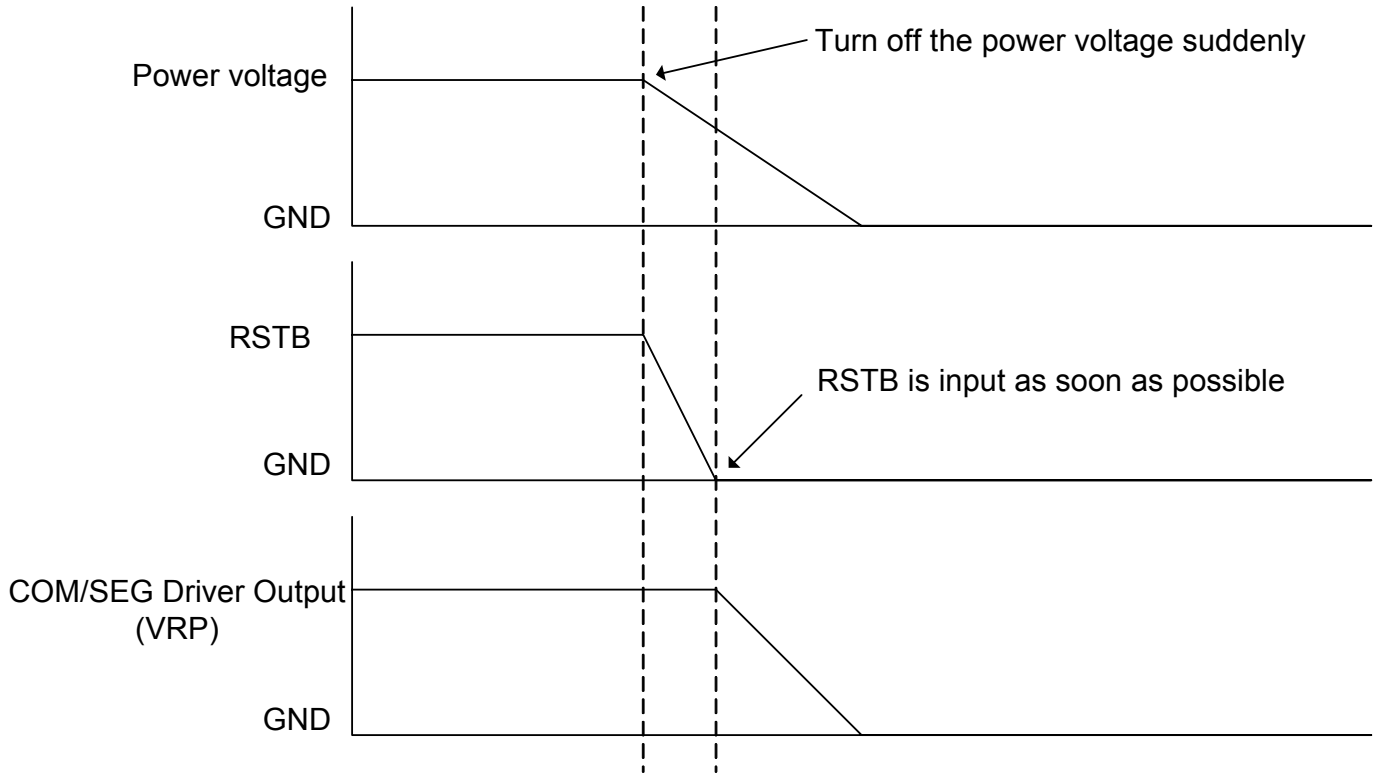
EXTERNAL POWER INPUT SEQUENCE



VDD3 must be applied earlier than VIN1/VIN1R/VIN1A or at least applied simultaneously with these signals. When C1 of regulator application is 1μF, RSTB must be applied after VIN1/VIN1R/VIN1A have been applied. The applied time gap between VIN1/VIN1R/VIN1A and RSTB is minimum 2ms. As C1 becomes larger, this time gap must be increased. Otherwise function is not guaranteed.

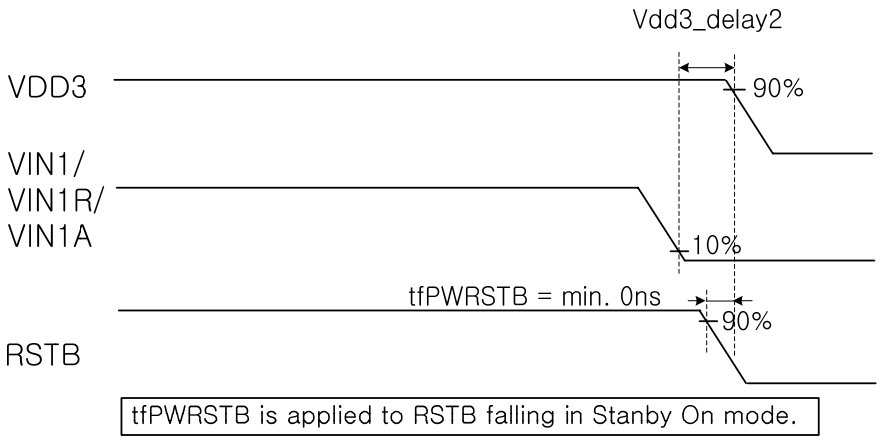
POWER OFF SEQUENCE





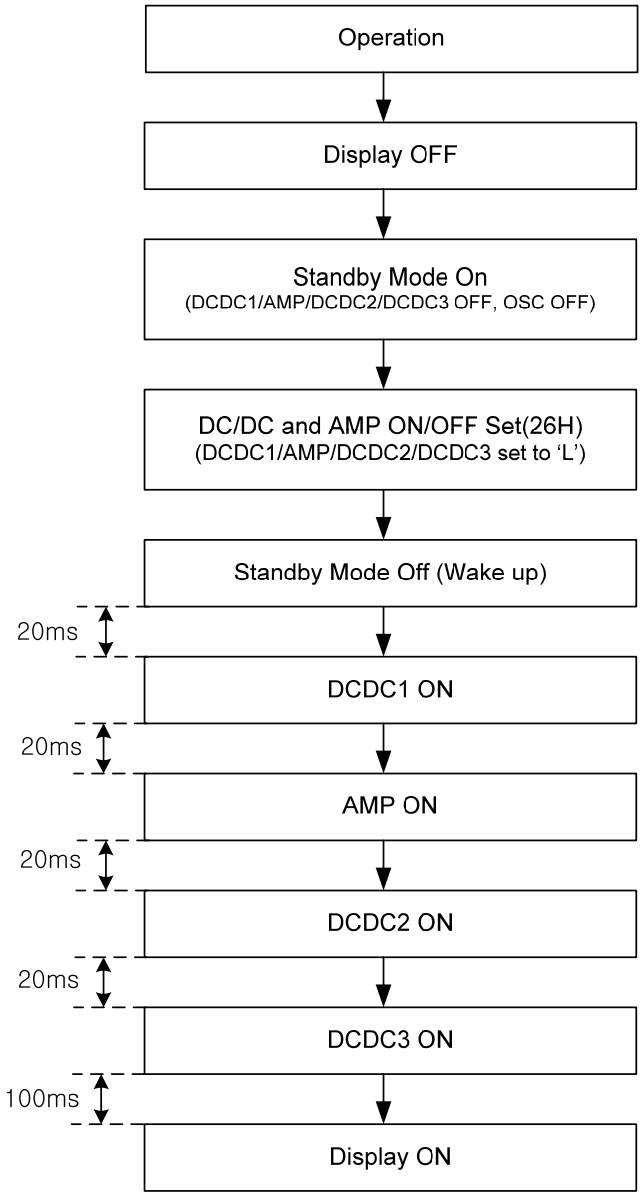
Note: When the signal of the hardware reset comes during the power-off period, COM/SEG output is forcibly lowered to the GND levels. Discharge resistor must be added at VCC pin. Refer application system diagram.

EXTERNAL POWER OFF SEQUENCE



VDD3 must be powered down later than VIN1/VIN1R/VIN1A or at least powered down simultaneously with these signals. The time gap of powered down between RSTB and VDD3 is minimum 0ns after 300ms discharge time in standby-on mode. Refer to Power Off Sequence (Normal Case). Otherwise function is not guaranteed.

WAKE UP SEQUENCE



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage range	VDD3	-0.3 to +4.0	V
	VDD	-0.3 to +2.3	
	VIN1	-0.3 to +4.0	
LCD Supply Voltage range	|VCC – VEE|	22	V
Input Voltage range	Vin	- 0.3 to VDD3 +0.3	V
Operating Temperature range	TOPR	-30 to +70	°C
Storage Temperature range	TSTR	-55 to +150	°C

OPERATING VOLTAGE

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage (1)	VDD3 (*1)	1.65	-	3.3	V
Supply Voltage (2)	VIN1 (*1)	2.4	3.0	3.6	V
Supply Voltage (3)	VIN2	2.4	3.0	5.5	

(*1) VIN1 = VIN1R, VIN1A

DC CHARACTERISTICS (1)

(Vss = 0V, V_{DD3} = 1.65 to 3.3V, Ta = -30 to 70 °C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Remarks
Operating voltage		VDD3		1.65		3.3	V	VDD3
Operating voltage		VDD		1.45		1.55	V	VDD
Operating voltage		VIN1		2.4	-	3.6	V	VIN1,VIN1A
Operating voltage		VIN2		2.4	-	6.0	V	
Operating voltage		VIN45		2.4	-	6.0	V	VOUT45
Operating voltage		DC2IN	1/4 Bias	1.5	-	3.0	V	DC2OUT
			1/5 Bias	2.0	-	4.0		
			1/6 Bias	1.67	-	3.33		
			1/7 Bias	2.0	-	4.0		
Operating voltage		2Vr	2Vr = |(VRP) – (VRN)|	4.0	-	20	V	VRP, VRN
Output voltage		VREG	REG_OUT voltage	1.5 ± 0.05			V	VREG
Driving voltage input range		VM	External power supply mode	1.0		2.0	V	VMOUT
		VCC		5.0		12.0	V	VRP
		VEE		-3.0		-8.0	V	VRN
Input voltage	High	V_{IH}		0.8VDD3	-	VDD3	V	
	Low	V_{IL}		VSS	-	0.2VDD3		
Output voltage	High	V_{OH}	I_{OH} = 0.5mA	0.8VDD3	-	VDD3	V	
	Low	V_{OL}	I_{OL} = 0.5mA	VSS	-	0.2VDD3		
Input leakage current		I_{IL}	VIN = VDD or VSS	-1.0	-	+1.0	μA	
Output leakage current		I_{OZ}	VIN = VDD or VSS	-3.0	-	+3.0	μA	
Oscillator Frequency Tolerance	Normal or Partial 0	F_{OSC1}	(*R1)=72k Ohm, (fFR=80Hz target), DSG=0, 162 Duty, VDDO=1.5V, Ta=25°C	253.4	281.6	309.7	kHz	OSC1 - OSC2
	Partial 1	F_{OSC2}	DSG=0, 66 Duty VDDO=1.5V, Ta=25°C	84.46	93.86	103.23	kHz	fOSC1/3
Driving voltage input range		V1 VM		2.0 1.0	-	4.0 2.0	V	
Regulator output range		REG_OUT	RTEST = “L”	1.45	1.5	1.55	V	

Note : (*R1) resistances are only recommended to get target frame frequency. But the value is not absolute.

DC CHARACTERISTICS (2)

Item		Symbol	Condition	Min	Typ	Max	Unit	Remarks
Driver output resistance	SEG	R_{ON-Seg}	V1=3.0 V, V0=0V, Ta = 25°C, Iload=50uA	-	1.5	2.0	kΩ	SEGn
	COM	R_{ON-Com}	VCC=10.5 V, VM=1.5V, VEE=-7.5V, Ta = 25°C, Iload=100uA	-	1.0	1.5	kΩ	COMn
Current consumption	Normal Mode	IDD	VDD3=VIN1=3.0V, V1=3.0V, Bias(1)=1/6, DC(1)=x1.5, Ta=25°C, Display line=162 DSG=0 fOSC1=281.6kHz (fFR=80Hz) No load, No access, All white pattern	-	500	600	μA	VDD3 + VIN1
	Partial1 Mode		VDD3=VIN1=3.0V, V1=3.0V, Bias(2)=1/5, DC(2)=x1.5, Ta=25°C, 1/66 duty fOSC2=93.86kHz (fFR=66Hz) No load, No access, All white pattern	-	400	500	μA	

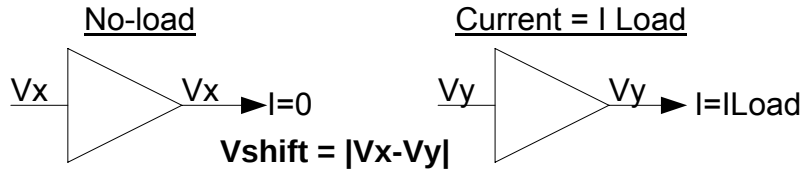
- : “IDD” is determined from lowest power consumption for dc-dc converter.

DC CHARACTERISTICS (3)

(Vss = 0V, V_{DD3} = 1.65 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Voltage shift range(*1)	Δ (VRP)	Isource = 80uA	-	-	200	mV	VRP
	Δ (V1)	Isource = 250uA	-	-	50	mV	V1
	Δ (VM)	Isource,sink = 250uA	-	-	50	mV	VM
	Δ (VRP)	Isink = 80uA	-	-	200	mV	VRN

(*1) Voltage shift means output voltage deference between output current = Iload and no-load.
Refer to the following figure. (in case of source current mode)



Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Tolerance of Bias ratio	Δ (VRP)_0 Δ (VRN)_0(*1)	No load	-200	-	+200	mV	VRP VRN

(*1) Tolerance of bias ratio definition
Δ (VRP)_0 = ((VRP) – VM) – VM / Bias
Δ (VRN)_0 = (VM – (VRN)) – VM / Bias

DC CHARACTERISTICS (4)

(Vss = 0V, V_{DD3} = 1.65 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

Item	Symbol	Condition		Min	Typ	Max	Unit	Remarks
Temperature compensation	ΔVt	VDD3=VIN1=V1=3.0V, -20 to 70 °C		-0.02	-	+0.02	%/°C	V1
Tolerance of Contrast step of V1	ΔVstep			3.92	7.84	11.76	mV	V1
Voltage range	ΔV1 ΔVM	Contrast set = FFh	V1	3.95	4.00	4.05	V	V1
			VM	1.95	2.00	2.05	V	VM
		Contrast set = 00h	V1	1.95	2.00	2.05	V	V1
			VM	0.95	1.00	1.05	V	VM

Item			Condition		Max	Unit	Ref
			Load current	Voltage range			
Offset Voltage	||VRP-VM| -|VM –(VRN)||		I Load = +100uA (VRP) I Load = -100uA (VRN)	VRP=5.0~12.0 V V1=2.0~4.0V VM=1.0~2.0V VRN=-3.0~-8.0 V	150	mV	Fig.1
	||V1-VM| -|VM-V0||	A	I Load = +100uA (V1, VM)		50	mV	Fig.2
		B	I Load = +100uA (VRP) I Load = -100uA (VRN)				

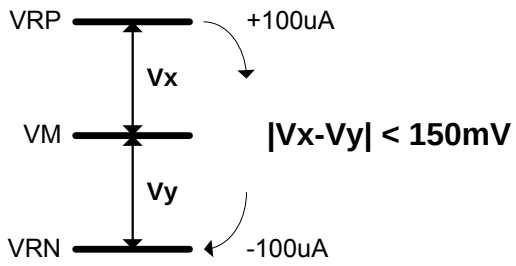


Fig. 1: Offset voltage definition (VRP,VM,VRN)

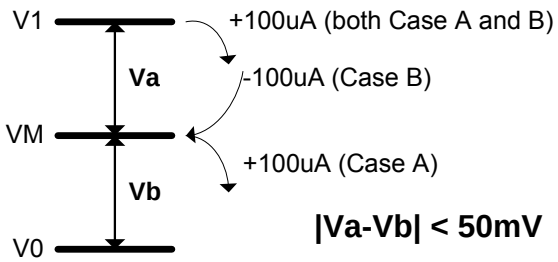


Fig. 2: Offset voltage definition (V1,VM,V0)

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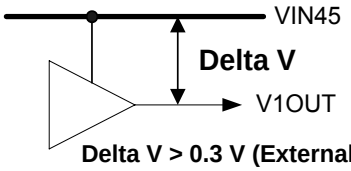
DC CHARACTERISTICS (5)

(Vss = 0V, V_{DD3} = 1.65 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

Item		Range	
		Min	Max
Voltage Level	V1OUT	2.0 V	4.0 V (DC(1) and DC(2) = X2) (*1)
	VMOUT	1.0 V	2.0 V (DC(1) and DC(2) = X2) (*2)
	DC2OUT	1.5V (1/4 Bias, V1OUT = 2V)	4.0V (DC(1) and DC(2) = X2) (*3) (1/5 bias, V1OUT = 4V)

(*1) This definition is shown as below



Delta V > 0.3 V (External VIN45)

Delta V > 0.5 V (VIN45 = VOUT45)

If V1OUT input voltage is set over VIN45, V1OUT output voltage must be clipped near VIN45. In this case, V1OUT output level must not be unstable. Refer to Fig.1

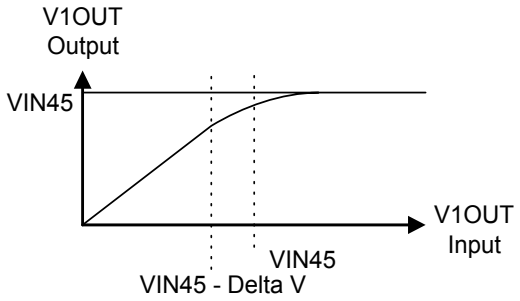
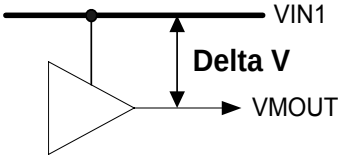


Fig. 1

(*2) This definition is shown as below



Delta V > 0.3 V

If VMOUT input voltage is set over VIN1, VMOUT output voltage must be clipped near VIN1. In this case, VMOUT output level must not be unstable. Refer to Fig.2

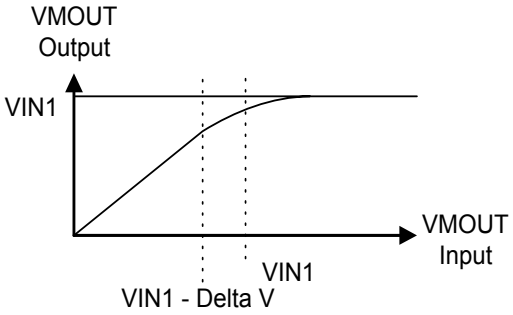
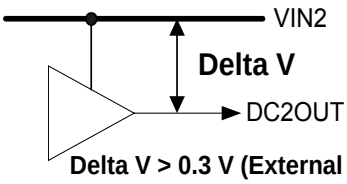


Fig. 2

(*3) This definition is shown as below



Delta V > 0.3 V (External VIN2)

Delta V > 0.5 V (VIN2 = VOUT45)

If DC2OUT input voltage is set over VIN2, DC2OUT output voltage must be clipped near VIN2. In this case, DC2OUT output level must not be unstable. Refer to Fig.3

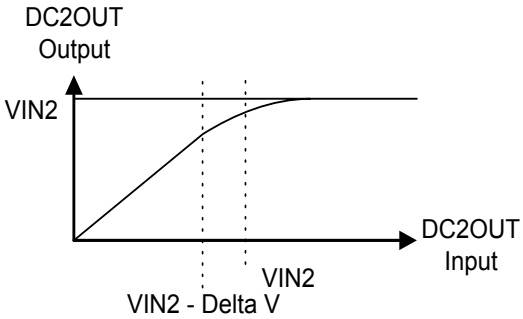


Fig. 3

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)

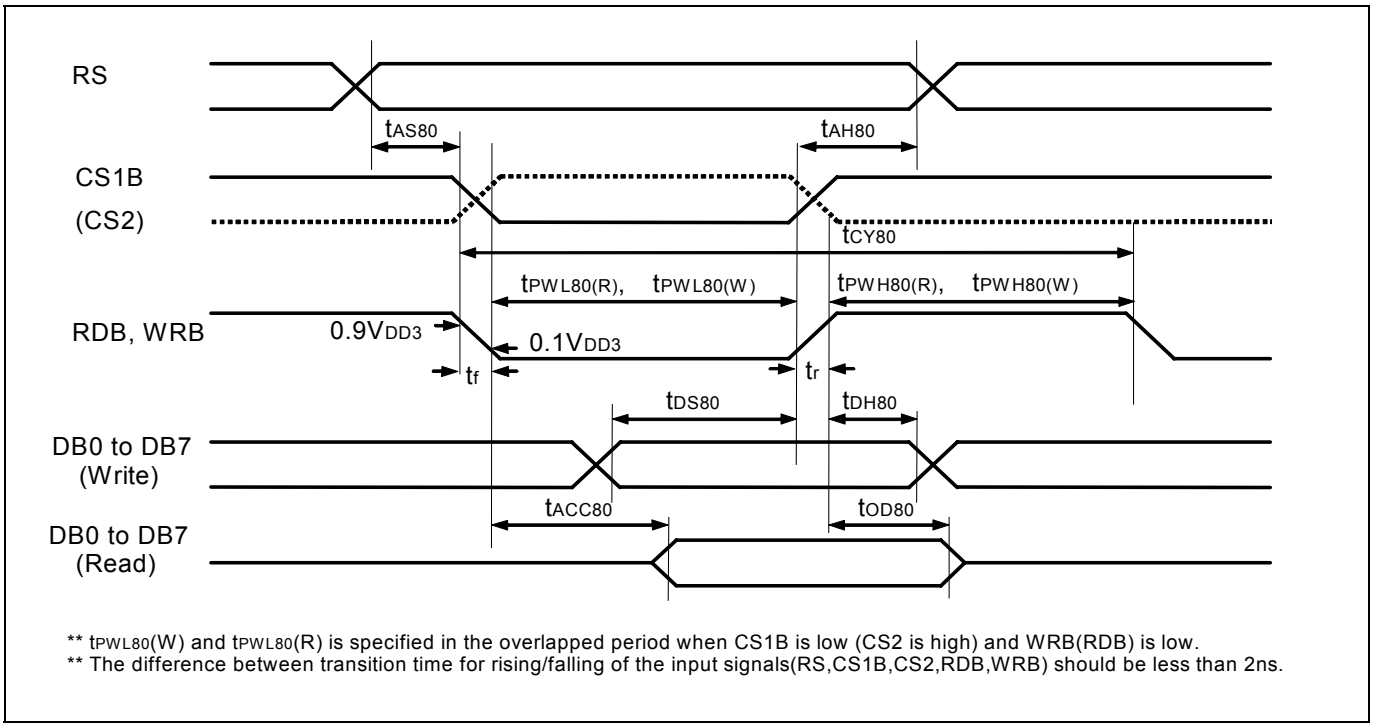


Figure 22. Parallel Interface (8080-series MPU) Timing Diagram

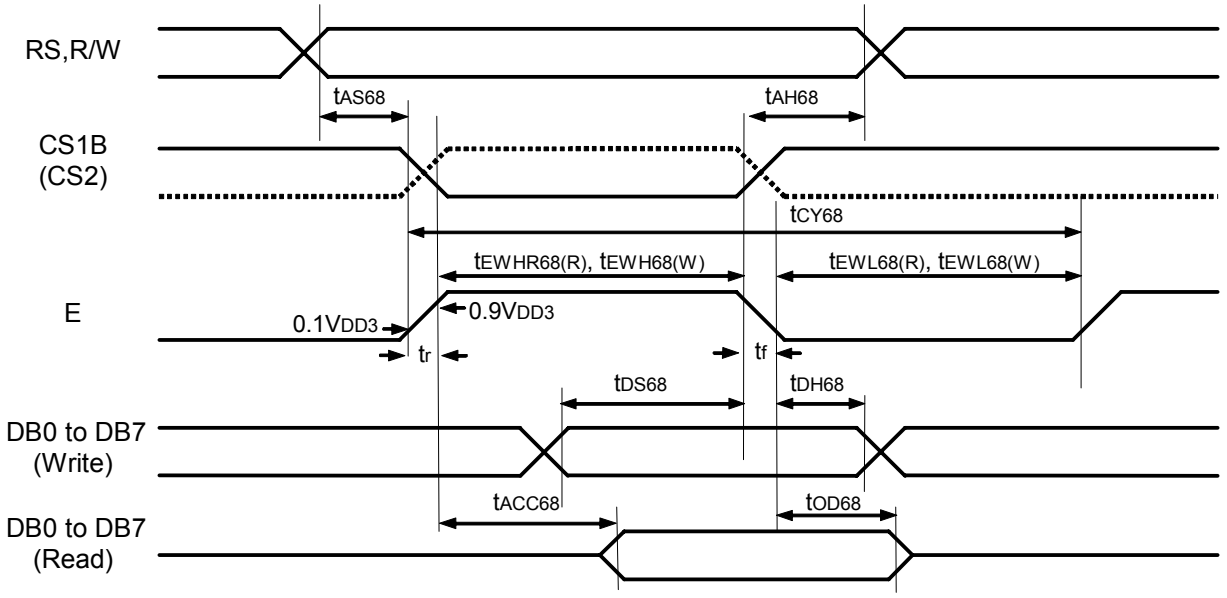
Table 17.AC Characteristics (8080-series Parallel Mode)

(V_{DD3} = 1.65 ~ 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min	Max	Unit
Address setup time Address hold time	RS	t_{AS80} t_{AH80}		0 0		ns
System cycle time(For write)		t_{CY80}		100		ns
Pulse width low for write Pulse width High for write	WRB (WRB)	$t_{PWL80(W)}$ $t_{PWH80(W)}$		40 40		ns
Pulse width low for read Pulse width high for read	RDB (RDB)	$t_{PWL80®}$ $t_{PWH80®}$		120 40		ns
Data setup time Data hold time	DB0 to DB15	t_{DS80} t_{DH80}		10 10		ns
Read access time		t_{ACC80}	CL = 50 pF		150	ns
Output disable time		t_{OD80}	no load	20		ns

NOTE: *1. (tr + tf) < (t_{CY80} – $t_{PWL80(W)}$ – $t_{PWH80(W)}$) for write, (tr + tf) < (t_{CY80} – t_{PWLR80} – t_{PWHR80}) for read.

Read / Write Characteristics (6800-series Microprocessor)



** t_{EWH68}(W) and t_{EWH68}(R) is specified in the overlapped period when CS1B is low (CS2 is high) and E is high.
** The difference between transition time for rising/falling of the input signals(RS,R/W,CS1B,CS2,E) should be less than 2ns.

Figure 23. Parallel Interface (6800-series MPU) Timing Diagram

Table 18.AC Characteristics (6800-series Parallel Mode)

(V_{DD3} = 1.65 ~ 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min	Max	Unit
Address setup time Address hold time	RS, WRB (R/W)	t_{AS68} t_{AH68}		0 0		ns
System cycle time(For write)		t_{CY68}		100		ns
Enable width high for write Enable width low for write	RDB (E)	$t_{EWH68(W)}$ $t_{EWL68(W)}$		40 40		ns
Enable width high for read Enable width low for read	RDB (E)	$t_{EWH68®}$ $t_{EWL68®}$		120 40		ns
Data setup time Data hold time	DB0 to DB15	t_{DS68} t_{DH68}		10 10		ns
Read access time		t_{ACC68}	C_L = 50 pF		150	ns
Output disable time		t_{OD68}	no load	20		ns

NOTE: *1. (tr + tf) < (t_{CY68} – $t_{EWH68(W)}$ – $t_{EWL68(W)}$) for write, (tr + tf) < (t_{CY68} – $t_{EWH68®}$ – $t_{EWL68®}$) for read.

Serial Data Interface (4 Pin) Timing

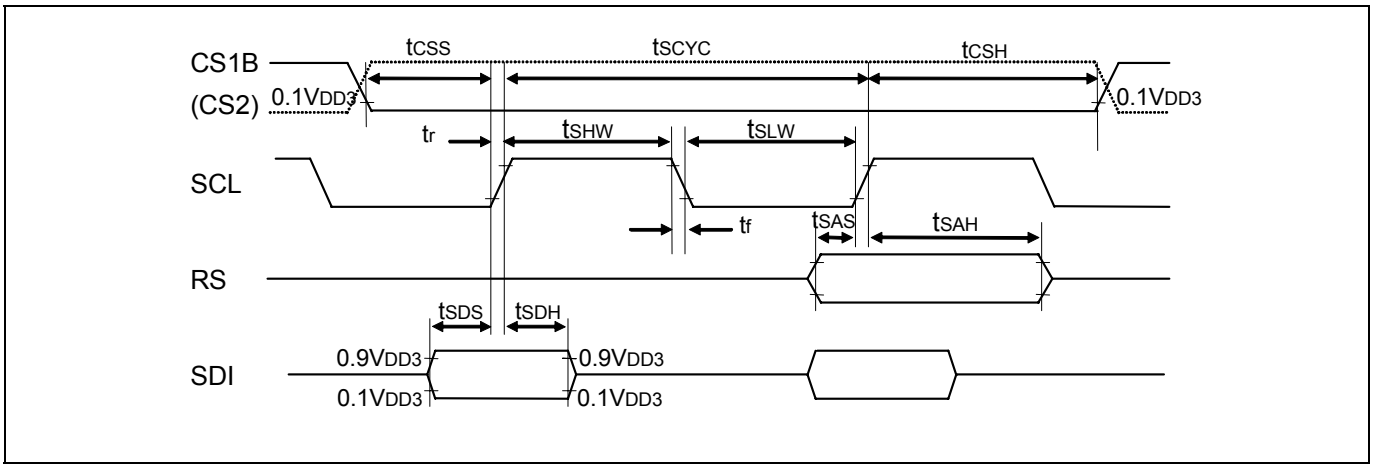


Figure 24. Serial Interface (4 Pin) Timing Diagram

Table 19.Serial Data Interface Timing

(V_{DD3} = 1.65 ~ 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min	Unit
SCL Cycle Time	SCL	t_{SCYC}		75	ns
SCL High Pulse Width	SCL	t_{SHW}		20	ns
SCL Low Pulse Width	SCL	t_{SLW}		20	ns
SDI Setup time	SDI	t_{SDS}		10	ns
SDI Hold time	SDI	t_{SDH}		10	ns
RS Setup time	RS	t_{SAS}		10	ns
RS Hold time	RS	t_{SAH}		10	ns
Chip Select Setup time	CS1B (CS2)	t_{CSS}		10	ns
Chip Select Hold time	CS1B (CS2)	t_{CSH}		0	ns

NOTE: *1. (tr + tf) < (t_{SCYC} – t_{SHW} – t_{SLW}) for write.

Serial Data Interface (3 Pin) Timing

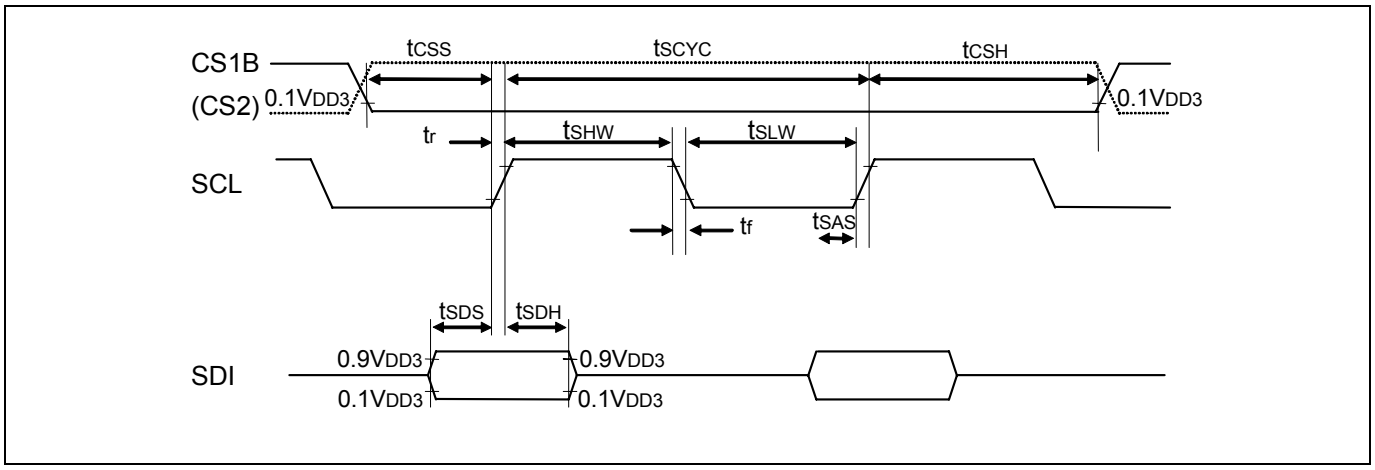


Figure 25. Serial Interface (3 Pin) Timing Diagram

Table 20.Serial Data Interface Timing

(V_{DD3} = 1.65 ~ 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min	Unit
SCL Cycle Time	SCL	t_{SCYC}		75	ns
SCL High Pulse Width	SCL	t_{SHW}		20	ns
SCL Low Pulse Width	SCL	t_{SLW}		20	ns
SDI Setup time	SDI	t_{SDS}		10	ns
SDI Hold time	SDI	t_{SDH}		10	ns
Chip Select Setup time	CS1B (CS2)	t_{CSS}		10	ns
Chip Select Hold time	CS1B (CS2)	t_{CSH}		0	ns

NOTE: *1. (tr + tf) < (t_{SCYC} – t_{SHW} – t_{SLW}) for write.

RESET INPUT TIMING

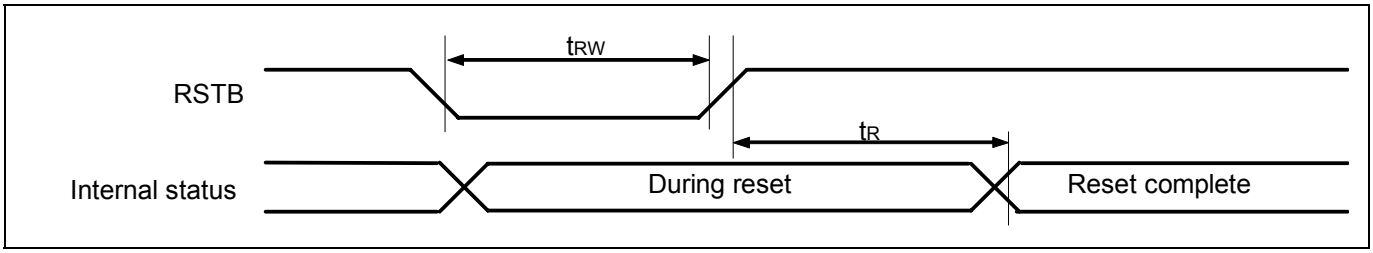


Figure 26. Reset Input Timing Diagram

Table 21.AC Characteristics (Reset mode)

(V_{DD3} = 1.65 ~ 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset low pulse width	RSTB	T_{RW}		1000	-	ns
Reset time	-	t_R		-	1000	ns

MTP CALIBRATION MODE

SEQUENCE FOR SETTING THE MODIFIED ELECTRONIC VOLUME

- Next figure is a Block Diagram of Sequence for Setting the Modified Electronic Volume.

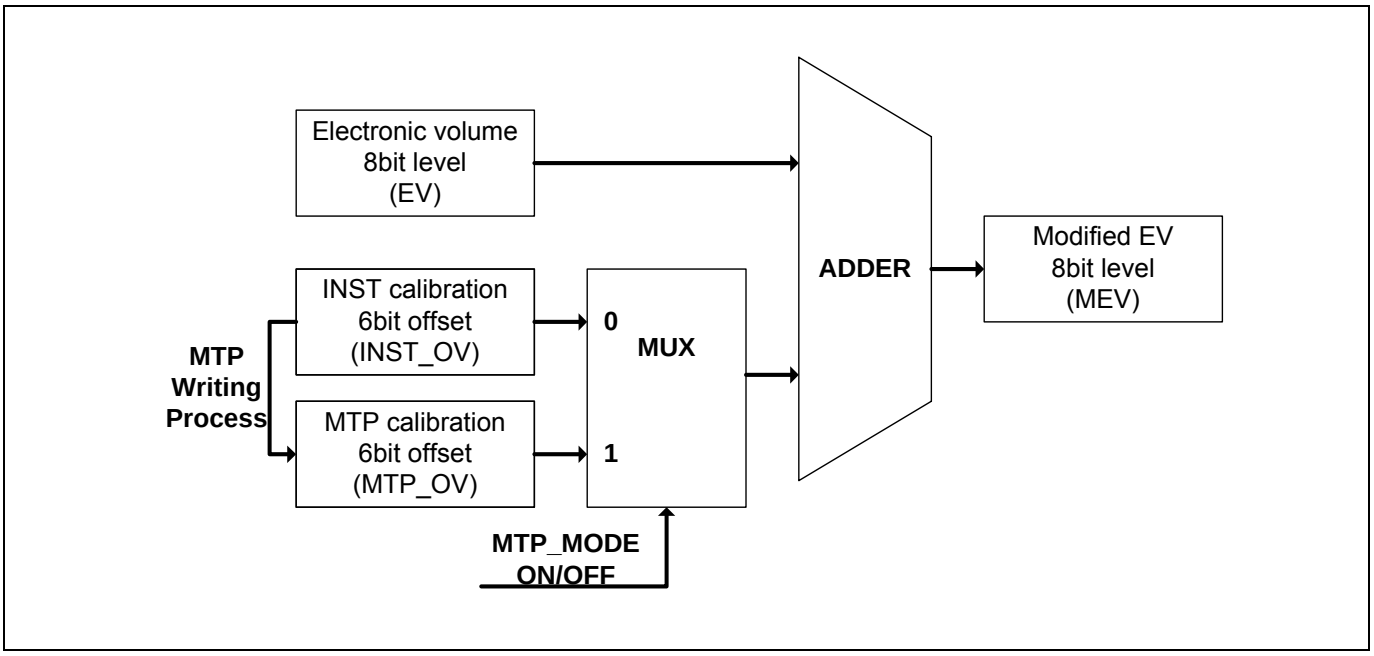


Figure 27. Sequence for Setting the Modified Electronic Volume

Initially, MTP cell is not programmed and has 6'b00000 value. When the external reset is applied, MTP mode is On. MEV is EV + MTP_OV. Since MTP_OV is 6'b00000, MEV is EV. For V1OUT calibration The instruction "MTP mode off" is executed, and then MEV is EV + OV and user can adjust MEV value using the instruction "Set offset volume register". When MEV overflows or underflows, MEV will be saturated. Repeat this step until end of the calibration. If V1OUT calibration is suitable, MTP writing process is executed, and then MTP cell is programmed and MTP_OV is programmed with OV. Finally, V1OUT calibration process is finished. Again, when the external reset is applied, MTP mode is ON. MEV is EV + MTP_OV. Accordingly MEV is the EV that has always the offset with MTP_OV value. However, if programmed MTP_OV is unlike, the instruction "MTP mode off" can be executed and then MEV will be EV + OV. Accordingly OV can be adjusted with instructions although MTP cell is programmed.

EEPROM CELL STRUCTURE

MTP (Multi Time Programmable) has been implemented on the S6B33BL. The EEPROM stores the offset volume for V1OUT calibration after the device has been assembled and calibrated on a LCD module. For MTP programming, MTPV pin is used. These pins should be available to on the module glass by ITO.
The MTP block of the S6B33BL consists of 7 bits. 1 bit is used for MTP mode protection bit (MPRT), and 6 bits are used for V1OUT calibration (MOV5~MOV0). MPRT can be read or written automatically in this LSI.

EEPROM block

MSB						LSB
MPRT	**MOV5**	**MOV4**	**MOV3**	**MOV2**	**MOV1**	**MOV0**

Description

MPRT : The Offset Volume(OV) can be written to EEPROM cells only when MPRT bit = '0'
MOV5~MOV0 : The MOV is used for calibrating the V1OUT voltage as an offset to the EV register value.

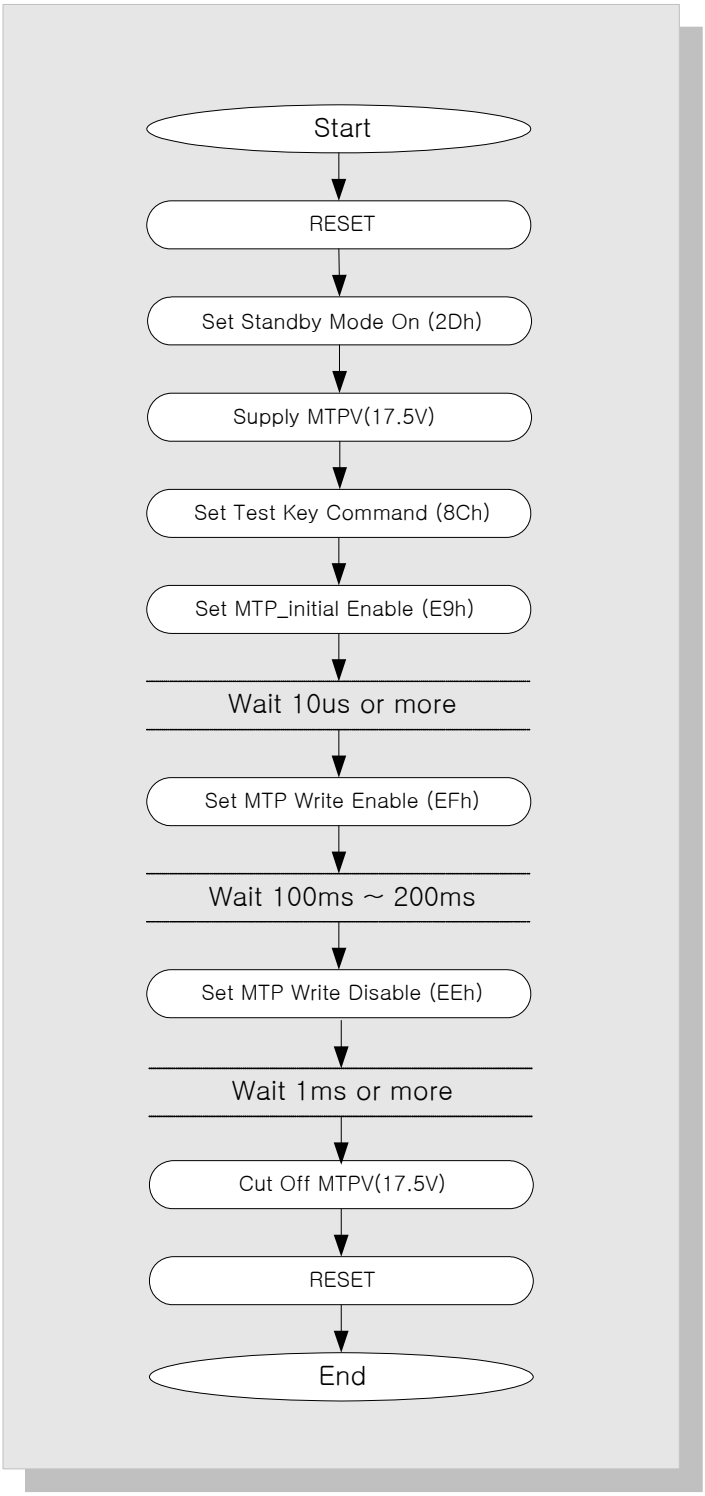
V1OUT CALIBRATION FLOW

V1OUT may be calibrated with MTP in the following order.(ex : EV = 32, OV=-3)

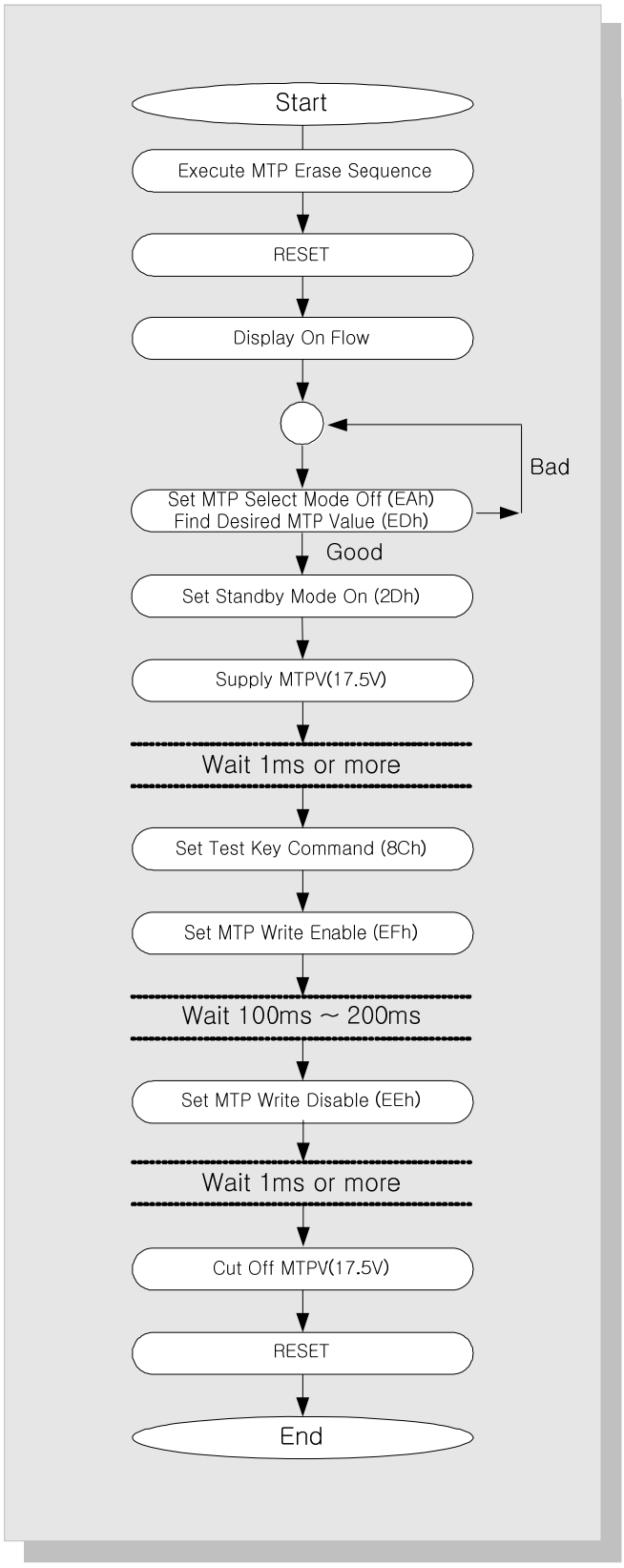
STEP	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
1.											Execute MTP erase sequence.
2.											Apply external reset. (MTP data load)
3.	0	0	0	0	1	0	1	0	1	0	Set contrast control using instruction. (EV = 32)
	0	0	0	0	1	0	0	0	0	0	
4.	0	0	1	1	1	0	1	0	1	0	MTP select mode off by using the instruction.
5.	0	0	1	1	1	0	1	1	0	1	Set offset volume by using the instruction. (OV = -3)
	0	0	0	0	1	1	1	1	0	1	
6.											Repeat STEP 4. Until the end of the calibration.
7	0	0	0	0	1	0	1	1	0	1	Standby on by using the instruction.
8.											Apply programming voltages for MTP programming. (MTPV=17.5V±500㎷) Wait 1ms or more.
9..	0	0	1	0	0	0	1	1	0	0	TEST Key Command.
10.	0	0	1	1	1	0	1	1	1	1	Set MTP write enable. (Only available when MPRT= 0) Wait 100ms ~ 200ms.
11.	0	0	1	1	1	0	1	1	1	0	Set MTP write disable. Wait 1ms or more.
12.											Cut off programming voltages for MTP programming (MTPV)
13.											Apply external reset.

After the external reset, the calibrated data are automatically transferred to the 6-bit reference voltage control register.
*MTP_WRITING PROCESS is available when MPRT is zero (if MPRT = 1, MTP cell could not be programmed).

MTP ERASE SEQUENCE



MTP WRITE SEQUENCE



VOLTAGES AND WAVEFORMS FOR MTP PROGRAMMING

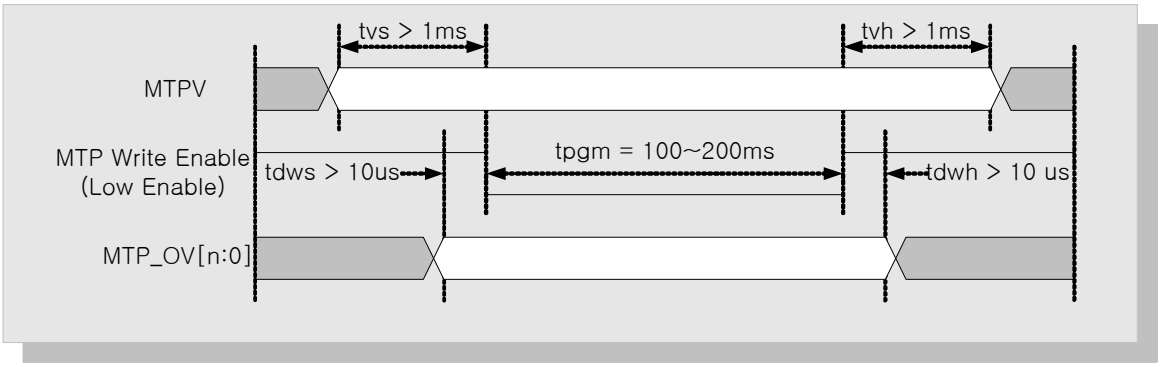


Figure 28. Voltages and waveforms for MTP programming

Specific timings

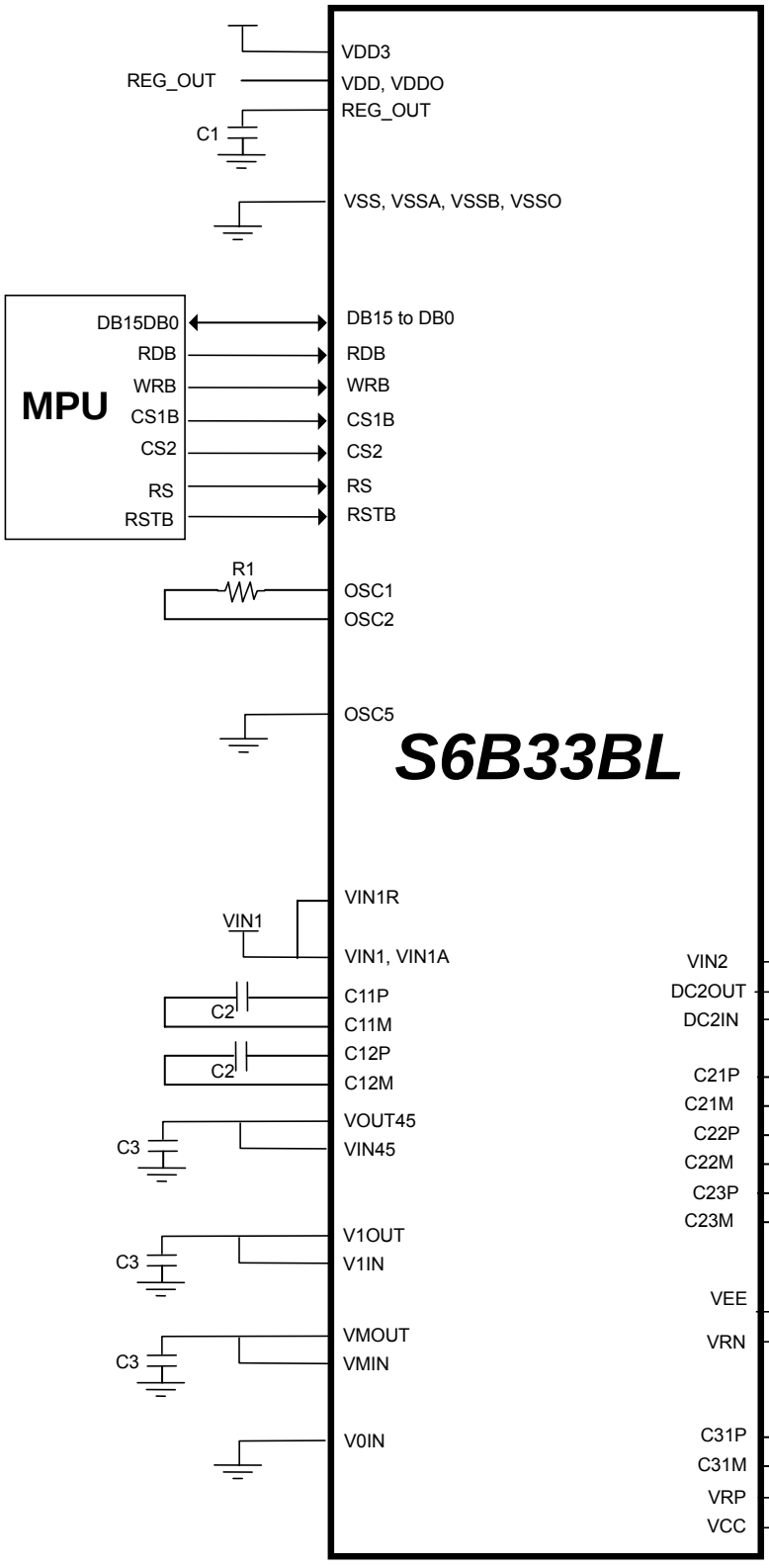
Timing	Min	Max
tvs	1ms	-
tvh	1ms	-
tdws	10us	-
tdwh	10us	-
tpgm	100ms	200ms

MTPV Voltage Tolerance

Item	Pgm	Min	Typ	Max	Unit	Remarks
Tolerance of MTPV	Erase		17.5		V	± 500 mV
	Write		17.5			

SYSTEM APPLICATION DIAGRAM

INTERNAL POWER MODE



The value of ITO resistance from VRN to C3 must be 50Ω and below

External Component

Name	Device
R1,R2	Resistors
C1,C2,C3	Capacitors

Values of external Components

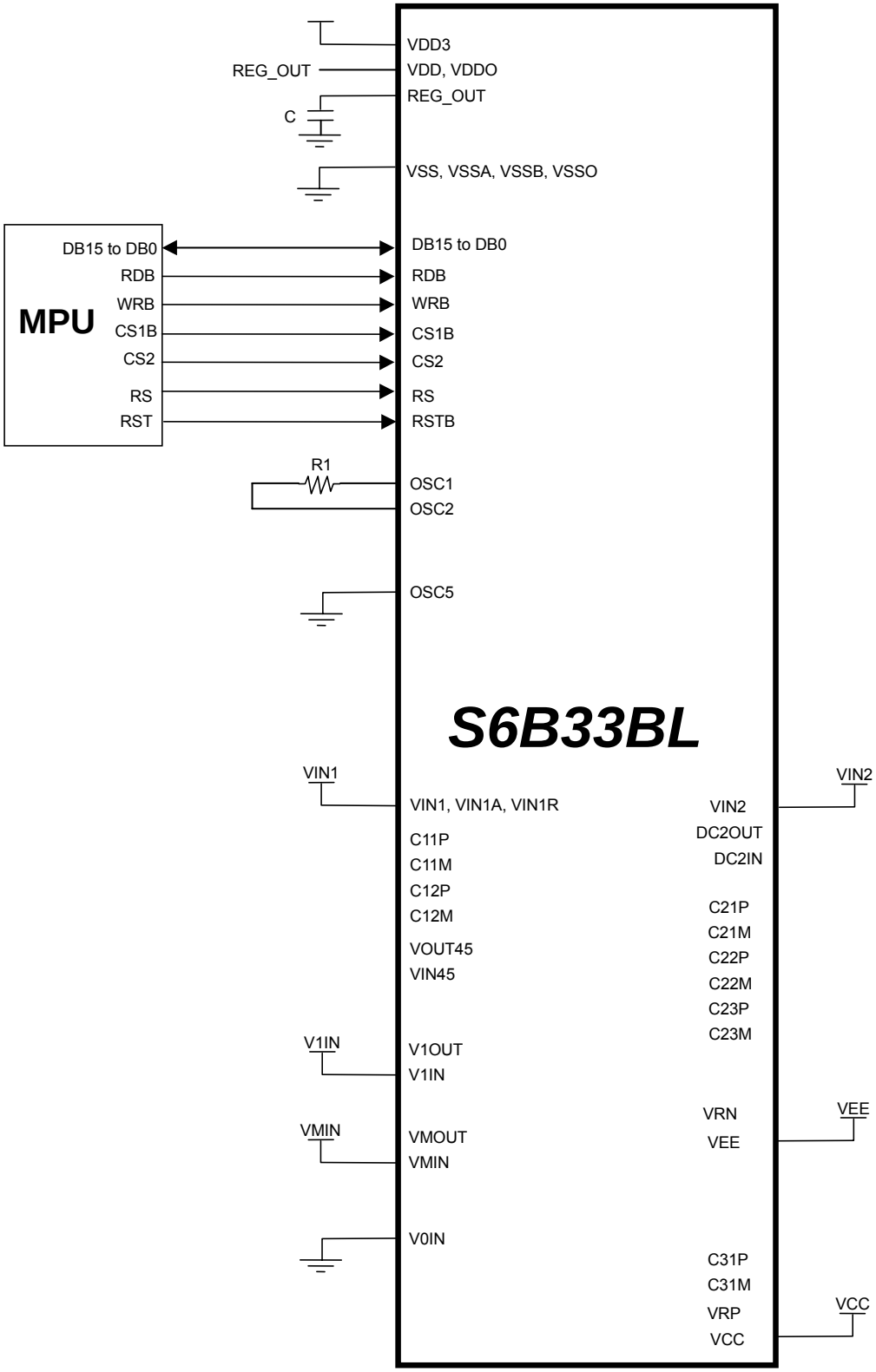
Item	Capacitance
C1	1.0 to 4.7μF
C2	1.0 to 2.2μF
C3	1.0 to 2.2μF

Note : Employing Rd is recommended when abnormal I display occurs in recovery sequence after detaching battery. (It depends on module or panel characteristics.)

Maximum rating voltage of capacitors

Item	Maximum rating voltage
REG_OUT to VSS	3V
VOUT45 to VSS	10V
C11P to C11M	6V
C12P to C12M	6V
VMOUT to VSS	3V
DC2OUT to VSS	5V
V1OUT to VSS	6V
C21P to C21M	5V
C22P to C22M	10V
C23P to C23M	13V
VSS to VRN	13V
C31P to C31M	17V
VRP to VSS	18V

EXTERNAL POWER MODE



REVISION HISTORY

Version	Content	Date
0.00	Original	March 28, 2007
0.01	Define TBD items(IDD)	October 16, 2007
1.00	Changed bump align key (page 4) Improved DC characteristics (page 36, 71) - Modified VIN1 operating range in 2x step-up : Max. 2.75V → Max. 3.0V - Modified VIN45/VIN2 voltage max. : 5.5V → 6.0V Changed maximum rating voltage of VIN45 capacitor (page 86)	October 19, 2007
1.10	Changed bump align key in figure2 (page 3), figure4(page5) Added bump tolerance (bump top size, height) in table1 (page 3)	November 20, 2007
1.20	Add license information	December 18, 2008

NOTICE

Precautions for Light

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.
2. Always test and inspect products under the environment with no penetration of light.

Patent Notice

This product contains patents licensed by Motif Inc. including U.S. Patent 5,420,604.