Specification

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Written by Department	Written by / Date	Approved by QRA Manager	Issued by D.C.C.
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文件變更履歷頁

Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	生效日期 Eff. Date
001	--	■ New Release	E01020006	1/22/2002

接續頁 CONTINUATION --- ☐ 是 YES; ☒ 否 NO

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320-Channel Low-voltage Segment Driver for Dot-Matrix STN Liquid Crystal Display

Description

The IST3033 is a 320-channel segment driver for driving a dot-matrix STN liquid-crystal panel at a low voltage. The driver can also correspond to 240-channel output by switching mode. It operates at a low voltage: a liquid-crystal drive voltage of 4.5 V and a logic drive voltage of 3 V, and is used together with common driver IST3032.

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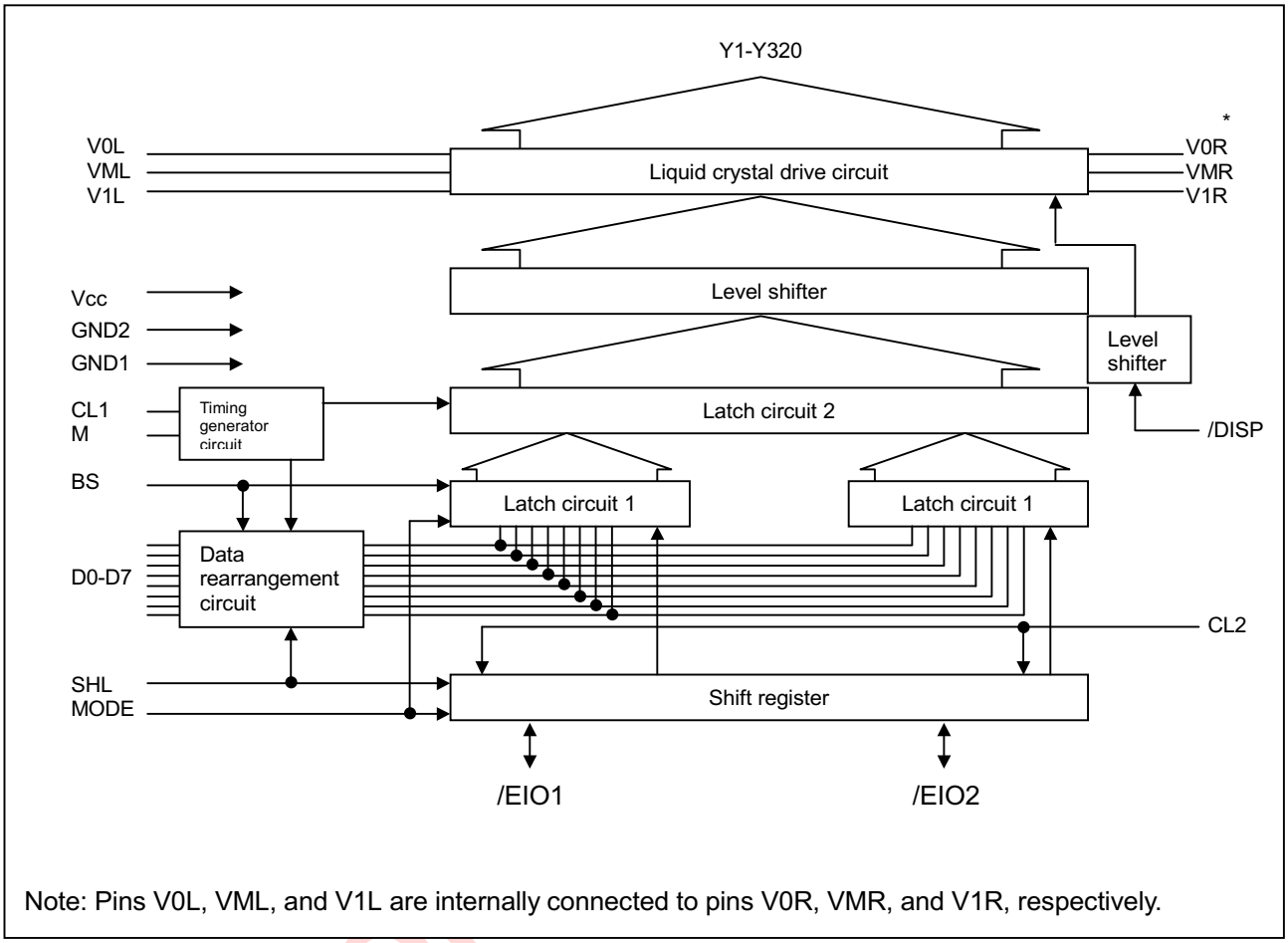
Features

- Display duty: Up to 1/240
- Liquid crystal drive voltage: 2.6 to 4.5 V
- Number of liquid crystal drive circuits: 320 circuits
- Operating voltage: 2.5 to 5.5 V
- Number of data bits: 4 or 8 bits
- Shift clock speed: 8 MHz max/5V
  6.5 MHz max/3V
- Together with the common drivers IST3032
- Low power consumption
- Switching output mode: 320 output mode
  240 output mode
- Display-off function
- COG package
- Automatic generation of chip-enable signals
- Standby function

Internal Block Diagram



Note: Pins V0L, VML, and V1L are internally connected to pins V0R, VMR, and V1R, respectively.

1. Liquid crystal drive circuit
   Selects and outputs the liquid crystal drive level V0, VM, or V1 by /DISP and a combination of data for latch circuit 2 and signal M.

2. Level shifter
   Converts logic signals to liquid crystal drive signals.

3. Latch circuit 2
   320-bit latch circuit, which latches the data of latch circuits 1 at the fall of CL1 and outputs the data to the level shifter.

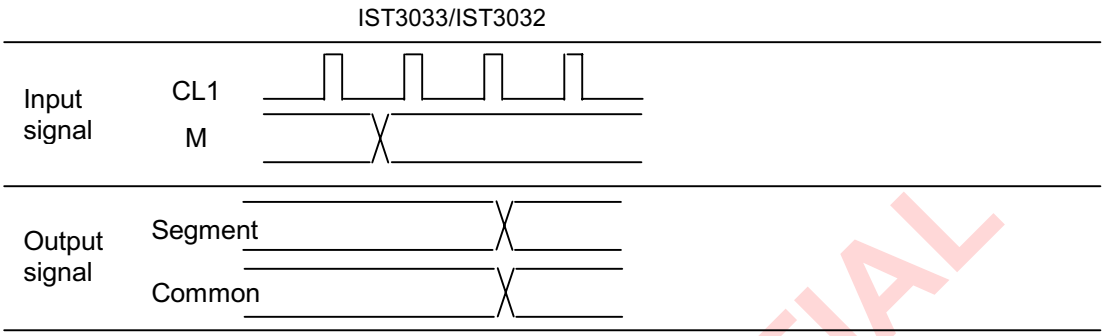
4. Latch circuit 1
   4/8-bit parallel data latch circuit, which latches display data D0 to D7 according to signals transmitted from the shift register.

5. Shift register
   80-bit shift register, which generates data-capture signals for latch circuits 1 at the fall of CL2.

6. Data rearrangement circuit
   Inverts the order of data output crosswise.

7. Timing generator circuit
The timing generator circuit generates data latch pulses for latch circuit 2 and changes pulse the LCD drive outputs to AC.

Low Voltage driver timing



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PAD CONFIGURATION :

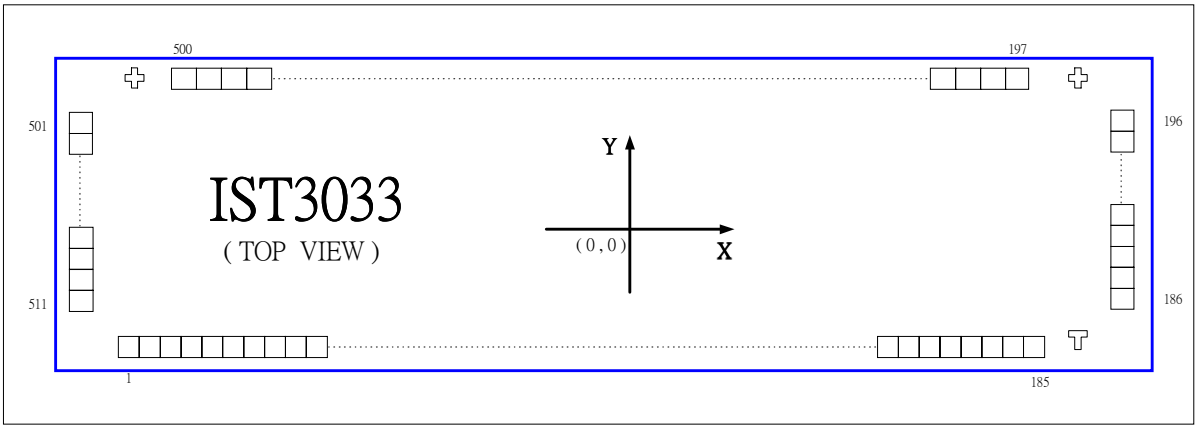

Figure 1 : IST3033 Chip Configuration

Table 1. IST3033 Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	511	17107	1000	um
Pad pitch	1~185	60 (Min.)		
	186~511	55 (Min.)		
Bumped pad size	2~184	40	80	
	187~195, 502~510	97	36	
	198~499	36	97	
	1, 185	58	80	
	186, 196, 501, 511	97	54	
	197, 500	54	97	
Bumped pad height	All pads	15		

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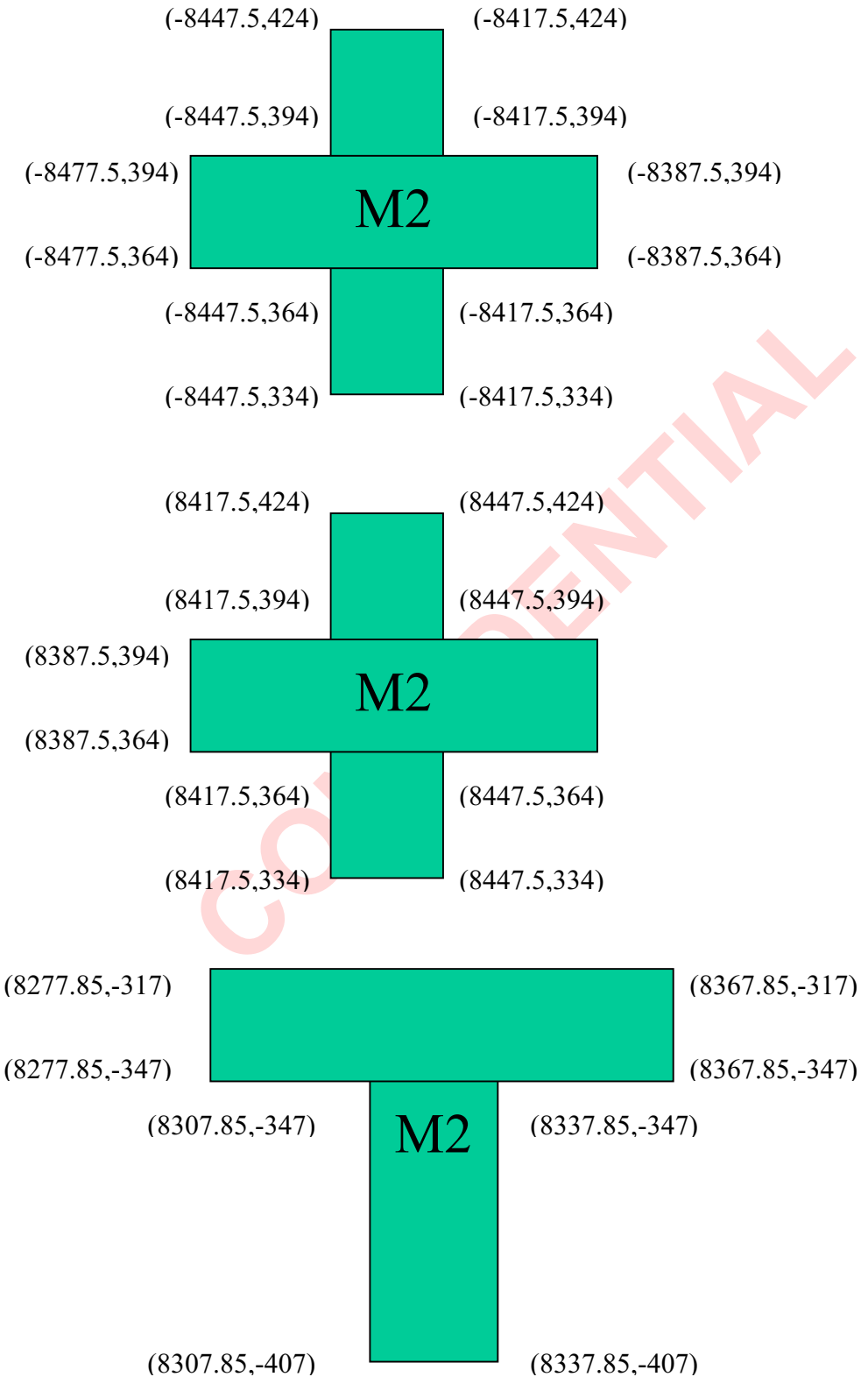
COG Align Key Coordinate :



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PAD CENTER COORDINATES :

Table 2 : Pad Center Coordinates

Unit : um

PAD NO	PAD NAME	COORDINATES X	COORDINATES Y	PAD NO	PAD NAME	COORDINATES X	COORDINATES Y
1	DUMMY	-8249.95	-361	36	V1	-5129.5	-361
2	VM	-8108.65	-361	37	DUMMY	-4997.35	-361
3	VM	-8048.65	-361	38	VCC	-4937.35	-361
4	VM	-7988.65	-361	39	VCC	-4877.35	-361
5	DUMMY	-7856.5	-361	40	VCC	-4817.35	-361
6	VM	-7724.35	-361	41	DUMMY	-4685.05	-361
7	VM	-7664.35	-361	42	VCC	-4625.05	-361
8	VM	-7604.35	-361	43	VCC	-4565.05	-361
9	DUMMY	-7472.05	-361	44	VCC	-4505.05	-361
10	VM	-7339.75	-361	45	DUMMY	-4372.75	-361
11	VM	-7279.75	-361	46	VCC	-4312.75	-361
12	VM	-7219.75	-361	47	VCC	-4252.75	-361
13	DUMMY	-7087.6	-361	48	VCC	-4192.75	-361
14	V0	-7027.6	-361	49	DUMMY	-4060.45	-361
15	V0	-6967.6	-361	50	MODE	-3928.15	-361
16	V0	-6907.6	-361	51	MODE	-3868.15	-361
17	DUMMY	-6775.3	-361	52	MODE	-3808.15	-361
18	V0	-6715.3	-361	53	DUMMY	-3676	-361
19	V0	-6655.3	-361	54	GND	-3616	-361
20	V0	-6595.3	-361	55	GND	-3556	-361
21	DUMMY	-6463	-361	56	GND	-3496	-361
22	V0	-6403	-361	57	DUMMY	-3363.7	-361
23	V0	-6343	-361	58	VCC	-3303.7	-361
24	V0	-6283	-361	59	VCC	-3243.7	-361
25	DUMMY	-6150.7	-361	60	VCC	-3183.7	-361
26	V1	-6018.4	-361	61	DUMMY	-3051.4	-361
27	V1	-5958.4	-361	62	BS	-2919.1	-361
28	V1	-5898.4	-361	63	BS	-2859.1	-361
29	DUMMY	-5766.25	-361	64	BS	-2799.1	-361
30	V1	-5634.1	-361	65	DUMMY	-2666.95	-361
31	V1	-5574.1	-361	66	GND	-2606.95	-361
32	V1	-5514.1	-361	67	GND	-2546.95	-361
33	DUMMY	-5381.8	-361	68	GND	-2486.95	-361
34	V1	-5249.5	-361	69	DUMMY	-2354.65	-361
35	V1	-5189.5	-361	70	GND	-2294.65	-361

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Table 2 : Pad Center Coordinates (Continued)

Unit : um

PAD NO	PAD NAME	COORDINATES X	COORDINATES Y	PAD NO	PAD NAME	COORDINATES X	COORDINATES Y
71	GND	-2234.65	-361	106	D4	1093.4	-361
72	GND	-2174.65	-361	107	D4	1153.4	-361
73	DUMMY	-2042.35	-361	108	D4	1213.4	-361
74	SHL	-1910.05	-361	109	DUMMY	1345.55	-361
75	SHL	-1850.05	-361	110	D5	1477.7	-361
76	SHL	-1790.05	-361	111	D5	1537.7	-361
77	DUMMY	-1657.9	-361	112	D5	1597.7	-361
78	VCC	-1597.9	-361	113	DUMMY	1730	-361
79	VCC	-1537.9	-361	114	D6	1862.3	-361
80	VCC	-1477.9	-361	115	D6	1922.3	-361
81	DUMMY	-1345.6	-361	116	D6	1982.3	-361
82	/EIO1	-1213.3	-361	117	DUMMY	2114.45	-361
83	/EIO1	-1153.3	-361	118	D7	2246.6	-361
84	/EIO1	-1093.3	-361	119	D7	2306.6	-361
85	DUMMY	-961.15	-361	120	D7	2366.6	-361
86	/DISP	-829	-361	121	DUMMY	2498.9	-361
87	/DISP	-769	-361	122	GND	2558.9	-361
88	/DISP	-709	-361	123	GND	2618.9	-361
89	DUMMY	-576.7	-361	124	GND	2678.9	-361
90	D0	-444.4	-361	125	DUMMY	2811.2	-361
91	D0	-384.4	-361	126	CL2	2943.55	-361
92	D0	-324.4	-361	127	CL2	3003.55	-361
93	DUMMY	-192.25	-361	128	CL2	3063.55	-361
94	D1	-60.1	-361	129	DUMMY	3195.7	-361
95	D1	-0.1	-361	130	CL1	3327.85	-361
96	D1	59.9	-361	131	CL1	3387.85	-361
97	DUMMY	192.2	-361	132	CL1	3447.85	-361
98	D2	324.5	-361	133	DUMMY	3580.15	-361
99	D2	384.5	-361	134	M	3712.45	-361
100	D2	444.5	-361	135	M	3772.45	-361
101	DUMMY	576.65	-361	136	M	3832.45	-361
102	D3	708.8	-361	137	DUMMY	3964.6	-361
103	D3	768.8	-361	138	/EIO2	4096.75	-361
104	D3	828.8	-361	139	/EIO2	4156.75	-361
105	DUMMY	961.1	-361	140	/EIO2	4216.75	-361

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Table 2 : Pad Center Coordinates (Continued)

Unit : um

PAD NO	PAD NAME	COORDINATES X	COORDINATES Y	PAD NO	PAD NAME	COORDINATES X	COORDINATES Y
141	DUMMY	4349.05	-361	176	VM	7316.15	-361
142	GND	4408.9	-361	177	DUMMY	7448.3	-361
143	GND	4468.9	-361	178	VM	7580.45	-361
144	GND	4528.9	-361	179	VM	7640.45	-361
145	DUMMY	4661.2	-361	180	VM	7700.45	-361
146	GND	4793.5	-361	181	DUMMY	7832.75	-361
147	GND	4853.5	-361	182	VM	7965.05	-361
148	GND	4913.5	-361	183	VM	8025.05	-361
149	DUMMY	4973.5	-361	184	VM	8085.05	-361
150	V1	5105.85	-361	185	DUMMY	8226.2	-361
151	V1	5165.85	-361	186	DUMMY	8430.5	-346
152	V1	5225.85	-361	187	Y320	8430.5	-276.35
153	DUMMY	5358	-361	188	Y319	8430.5	-221.35
154	V1	5490.15	-361	189	Y318	8430.5	-166.35
155	V1	5550.15	-361	190	Y317	8430.5	-111.35
156	V1	5610.15	-361	191	Y316	8430.5	-56.35
157	DUMMY	5742.45	-361	192	Y315	8430.5	-1.35
158	V1	5874.75	-361	193	Y314	8430.5	53.65
159	V1	5934.75	-361	194	Y313	8430.5	108.65
160	V1	5994.75	-361	195	Y312	8430.5	163.65
161	DUMMY	6126.9	-361	196	DUMMY	8430.5	227.65
162	V0	6186.9	-361	197	DUMMY	8343.5	377
163	V0	6246.9	-361	198	Y311	8277.5	377
164	V0	6306.9	-361	199	Y310	8222.5	377
165	DUMMY	6439.25	-361	200	Y309	8167.5	377
166	V0	6499.25	-361	201	Y308	8112.5	377
167	V0	6559.25	-361	202	Y307	8057.5	377
168	V0	6619.25	-361	203	Y306	8002.5	377
169	DUMMY	6751.55	-361	204	Y305	7947.5	377
170	V0	6811.55	-361	205	Y304	7892.5	377
171	V0	6871.55	-361	206	Y303	7837.5	377
172	V0	6931.55	-361	207	Y302	7782.5	377
173	DUMMY	7063.85	-361	208	Y301	7727.5	377
174	VM	7196.15	-361	209	Y300	7672.5	377
175	VM	7256.15	-361	210	Y299	7617.5	377

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Table 2 : Pad Center Coordinates (Continued)

Unit : um

PAD NO	PAD NAME	COORDINATES X	COORDINATES Y	PAD NO	PAD NAME	COORDINATES X	COORDINATES Y
211	Y298	7562.5	377	246	Y263	5637.5	377
212	Y297	7507.5	377	247	Y262	5582.5	377
213	Y296	7452.5	377	248	Y261	5527.5	377
214	Y295	7397.5	377	249	Y260	5472.5	377
215	Y294	7342.5	377	250	Y259	5417.5	377
216	Y293	7287.5	377	251	Y258	5362.5	377
217	Y292	7232.5	377	252	Y257	5307.5	377
218	Y291	7177.5	377	253	Y256	5252.5	377
219	Y290	7122.5	377	254	Y255	5197.5	377
220	Y289	7067.5	377	255	Y254	5142.5	377
221	Y288	7012.5	377	256	Y253	5087.5	377
222	Y287	6957.5	377	257	Y252	5032.5	377
223	Y286	6902.5	377	258	Y251	4977.5	377
224	Y285	6847.5	377	259	Y250	4922.5	377
225	Y284	6792.5	377	260	Y249	4867.5	377
226	Y283	6737.5	377	261	Y248	4812.5	377
227	Y282	6682.5	377	262	Y247	4757.5	377
228	Y281	6627.5	377	263	Y246	4702.5	377
229	Y280	6572.5	377	264	Y245	4647.5	377
230	Y279	6517.5	377	265	Y244	4592.5	377
231	Y278	6462.5	377	266	Y243	4537.5	377
232	Y277	6407.5	377	267	Y242	4482.5	377
233	Y276	6352.5	377	268	Y241	4427.5	377
234	Y275	6297.5	377	269	Y240	4372.5	377
235	Y274	6242.5	377	270	Y239	4317.5	377
236	Y273	6187.5	377	271	Y238	4262.5	377
237	Y272	6132.5	377	272	Y237	4207.5	377
238	Y271	6077.5	377	273	Y236	4152.5	377
239	Y270	6022.5	377	274	Y235	4097.5	377
240	Y269	5967.5	377	275	Y234	4042.5	377
241	Y268	5912.5	377	276	Y233	3987.5	377
242	Y267	5857.5	377	277	Y232	3932.5	377
243	Y266	5802.5	377	278	Y231	3877.5	377
244	Y265	5747.5	377	279	Y230	3822.5	377
245	Y264	5692.5	377	280	Y229	3767.5	377

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Table 2 : Pad Center Coordinates (Continued)

Unit : um

PAD NO	PAD NAME	COORDINATES X	COORDINATES Y	PAD NO	PAD NAME	COORDINATES X	COORDINATES Y
281	Y228	3712.5	377	316	Y193	1787.5	377
282	Y227	3657.5	377	317	Y192	1732.5	377
283	Y226	3602.5	377	318	Y191	1677.5	377
284	Y225	3547.5	377	319	Y190	1622.5	377
285	Y224	3492.5	377	320	Y189	1567.5	377
286	Y223	3437.5	377	321	Y188	1512.5	377
287	Y222	3382.5	377	322	Y187	1457.5	377
288	Y221	3327.5	377	323	Y186	1402.5	377
289	Y220	3272.5	377	324	Y185	1347.5	377
290	Y219	3217.5	377	325	Y184	1292.5	377
291	Y218	3162.5	377	326	Y183	1237.5	377
292	Y217	3107.5	377	327	Y182	1182.5	377
293	Y216	3052.5	377	328	Y181	1127.5	377
294	Y215	2997.5	377	329	Y180	1072.5	377
295	Y214	2942.5	377	330	Y179	1017.5	377
296	Y213	2887.5	377	331	Y178	962.5	377
297	Y212	2832.5	377	332	Y177	907.5	377
298	Y211	2777.5	377	333	Y176	852.5	377
299	Y210	2722.5	377	334	Y175	797.5	377
300	Y209	2667.5	377	335	Y174	742.5	377
301	Y208	2612.5	377	336	Y173	687.5	377
302	Y207	2557.5	377	337	Y172	632.5	377
303	Y206	2502.5	377	338	Y171	577.5	377
304	Y205	2447.5	377	339	Y170	522.5	377
305	Y204	2392.5	377	340	Y169	467.5	377
306	Y203	2337.5	377	341	Y168	412.5	377
307	Y202	2282.5	377	342	Y167	357.5	377
308	Y201	2227.5	377	343	Y166	302.5	377
309	Y200	2172.5	377	344	Y165	247.5	377
310	Y199	2117.5	377	345	Y164	192.5	377
311	Y198	2062.5	377	346	Y163	137.5	377
312	Y197	2007.5	377	347	Y162	82.5	377
313	Y196	1952.5	377	348	Y161	27.5	377
314	Y195	1897.5	377	349	Y160	-27.5	377
315	Y194	1842.5	377	350	Y159	-82.5	377

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Table 2 : Pad Center Coordinates (Continued)

Unit : um

PAD NO	PAD NAME	COORDINATES X	COORDINATES Y	PAD NO	PAD NAME	COORDINATES X	COORDINATES Y
351	Y158	-137.5	377	386	Y123	-2062.5	377
352	Y157	-192.5	377	387	Y122	-2117.5	377
353	Y156	-247.5	377	388	Y121	-2172.5	377
354	Y155	-302.5	377	389	Y120	-2227.5	377
355	Y154	-357.5	377	390	Y119	-2282.5	377
356	Y153	-412.5	377	391	Y118	-2337.5	377
357	Y152	-467.5	377	392	Y117	-2392.5	377
358	Y151	-522.5	377	393	Y116	-2447.5	377
359	Y150	-577.5	377	394	Y115	-2502.5	377
360	Y149	-632.5	377	395	Y114	-2557.5	377
361	Y148	-687.5	377	396	Y113	-2612.5	377
362	Y147	-742.5	377	397	Y112	-2667.5	377
363	Y146	-797.5	377	398	Y111	-2722.5	377
364	Y145	-852.5	377	399	Y110	-2777.5	377
365	Y144	-907.5	377	400	Y109	-2832.5	377
366	Y143	-962.5	377	401	Y108	-2887.5	377
367	Y142	-1017.5	377	402	Y107	-2942.5	377
368	Y141	-1072.5	377	403	Y106	-2997.5	377
369	Y140	-1127.5	377	404	Y105	-3052.5	377
370	Y139	-1182.5	377	405	Y104	-3107.5	377
371	Y138	-1237.5	377	406	Y103	-3162.5	377
372	Y137	-1292.5	377	407	Y102	-3217.5	377
373	Y136	-1347.5	377	408	Y101	-3272.5	377
374	Y135	-1402.5	377	409	Y100	-3327.5	377
375	Y134	-1457.5	377	410	Y99	-3382.5	377
376	Y133	-1512.5	377	411	Y98	-3437.5	377
377	Y132	-1567.5	377	412	Y97	-3492.5	377
378	Y131	-1622.5	377	413	Y96	-3547.5	377
379	Y130	-1677.5	377	414	Y95	-3602.5	377
380	Y129	-1732.5	377	415	Y94	-3657.5	377
381	Y128	-1787.5	377	416	Y93	-3712.5	377
382	Y127	-1842.5	377	417	Y92	-3767.5	377
383	Y126	-1897.5	377	418	Y91	-3822.5	377
384	Y125	-1952.5	377	419	Y90	-3877.5	377
385	Y124	-2007.5	377	420	Y89	-3932.5	377

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Table 2 : Pad Center Coordinates (Continued)

Unit : um

PAD NO	PAD NAME	COORDINATES X	COORDINATES Y	PAD NO	PAD NAME	COORDINATES X	COORDINATES Y
421	Y88	-3987.5	377	456	Y53	-5912.5	377
422	Y87	-4042.5	377	457	Y52	-5967.5	377
423	Y86	-4097.5	377	458	Y51	-6022.5	377
424	Y85	-4152.5	377	459	Y50	-6077.5	377
425	Y84	-4207.5	377	460	Y49	-6132.5	377
426	Y83	-4262.5	377	461	Y48	-6187.5	377
427	Y82	-4317.5	377	462	Y47	-6242.5	377
428	Y81	-4372.5	377	463	Y46	-6297.5	377
429	Y80	-4427.5	377	464	Y45	-6352.5	377
430	Y79	-4482.5	377	465	Y44	-6407.5	377
431	Y78	-4537.5	377	466	Y43	-6462.5	377
432	Y77	-4592.5	377	467	Y42	-6517.5	377
433	Y76	-4647.5	377	468	Y41	-6572.5	377
434	Y75	-4702.5	377	469	Y40	-6627.5	377
435	Y74	-4757.5	377	470	Y39	-6682.5	377
436	Y73	-4812.5	377	471	Y38	-6737.5	377
437	Y72	-4867.5	377	472	Y37	-6792.5	377
438	Y71	-4922.5	377	473	Y36	-6847.5	377
439	Y70	-4977.5	377	474	Y35	-6902.5	377
440	Y69	-5032.5	377	475	Y34	-6957.5	377
441	Y68	-5087.5	377	476	Y33	-7012.5	377
442	Y67	-5142.5	377	477	Y32	-7067.5	377
443	Y66	-5197.5	377	478	Y31	-7122.5	377
444	Y65	-5252.5	377	479	Y30	-7177.5	377
445	Y64	-5307.5	377	480	Y29	-7232.5	377
446	Y63	-5362.5	377	481	Y28	-7287.5	377
447	Y62	-5417.5	377	482	Y27	-7342.5	377
448	Y61	-5472.5	377	483	Y26	-7397.5	377
449	Y60	-5527.5	377	484	Y25	-7452.5	377
450	Y59	-5582.5	377	485	Y24	-7507.5	377
451	Y58	-5637.5	377	486	Y23	-7562.5	377
452	Y57	-5692.5	377	487	Y22	-7617.5	377
453	Y56	-5747.5	377	488	Y21	-7672.5	377
454	Y55	-5802.5	377	489	Y20	-7727.5	377
455	Y54	-5857.5	377	490	Y19	-7782.5	377

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Table 2 : Pad Center Coordinates (Continued)

Unit : um

PAD NO	PAD NAME	COORDINATES X	COORDINATES Y	PAD NO	PAD NAME	COORDINATES X	COORDINATES Y
491	Y18	-7837.5	377	502	Y9	-8430.5	163.65
492	Y17	-7892.5	377	503	Y8	-8430.5	108.65
493	Y16	-7947.5	377	504	Y7	-8430.5	53.65
494	Y15	-8002.5	377	505	Y6	-8430.5	-1.35
495	Y14	-8057.5	377	506	Y5	-8430.5	-56.35
496	Y13	-8112.5	377	507	Y4	-8430.5	-111.35
497	Y12	-8167.5	377	508	Y3	-8430.5	-166.35
498	Y11	-8222.5	377	509	Y2	-8430.5	-221.35
499	Y10	-8277.5	377	510	Y1	-8430.5	-276.35
500	DUMMY	-8343.5	377	511	DUMMY	-8430.5	-346
501	DUMMY	-8430.5	227.65				

※ Big PAD is highlighted

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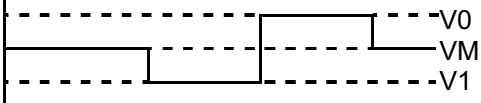
Pin Functions

<table>
<tr><th>Class</th><th>Symbol</th><th>Pin Name</th><th>I / O</th><th>Functions</th></tr>
<tr><td rowspan="2">Power supply</td><td>Vcc
GND1
GND2</td><td>Vcc
GND</td><td>-</td><td>Vcc-GND: Power supply for logic.</td></tr>
<tr><td>V0L, R
VML, R
V1L, R</td><td>V0L, R
VML, R
V1L, R</td><td>Input</td><td>Liquid crystal drive level power supply
  </td></tr>
<tr><td rowspan="9">Control signal</td><td>CL1</td><td>Clock 1</td><td>Input</td><td>Latch signal of display data: A liquid crystal drive signal corresponding to display data is output at the fall of CL1.</td></tr>
<tr><td>CL2</td><td>Clock 2</td><td>Input</td><td>Capture signal of display data: Display data is captured at the fall of CL2.</td></tr>
<tr><td>M</td><td>M</td><td>Input</td><td>A.C. signal of liquid crystal drive output</td></tr>
<tr><td>D0 to D7</td><td>DATA 0
to
DATA 7</td><td>Input</td><td>
<table>
<tr><th>Display data t</th><th>liquid crystal drive output</th><th>Liquid crystal display</th></tr>
<tr><td>1</td><td>(Vcc level) Selected level</td><td>ON</td></tr>
<tr><td>0</td><td>(GND level) Not-selected level</td><td>OFF</td></tr>
</table>
</td></tr>
<tr><td>SHL</td><td>Shift Left</td><td>Input</td><td>Control signal for inverting the order of data output (see the page 6)</td></tr>
<tr><td>/EIO1</td><td>Enable IO1</td><td>I / O</td><td>
<table>
<tr><th>SHL</th><th>/EIO1</th><th>/EIO2</th></tr>
<tr><td>GND</td><td>Enable input</td><td>Enable output</td></tr>
<tr><td>Vcc</td><td>Enable output</td><td>Enable input</td></tr>
</table>
</td></tr>
<tr><td>/EIO2</td><td>Enable IO2</td><td>I / O</td><td>Enable input: The enable input of the first IC is connected to the GND and another is connected to the enable input of the second IC.
Enable output: Connected to the enable input of the second IC at cascade output.</td></tr>
<tr><td>/DISP</td><td>Display off</td><td>Input</td><td>Grounding /DISP sets liquid crystal drive output Y1-Y320 to the VM level.</td></tr>
<tr><td>BS</td><td>Bus select</td><td>Input</td><td>Switches the number of input bits for the display data.
Vcc 8-bit input mode
GND 4-bit input mode (Captures data from D0-D3. At this time, connect D4-D7 to the GND.)</td></tr>
<tr><td>MODE</td><td>MODE</td><td>Input</td><td>Switches the number of input bits for the display data.
Vcc 320 output mode
GND 240 output mode (Y41-Y280 are valid output. The other 80 pins output the not-selected level signals synchronized every time, release these pins.)</td></tr>
</table>

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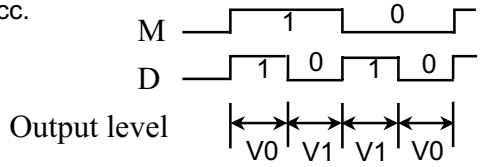
Pin Functions (cont)

Class	Symbol	Pin Name	I / O	Functions
Liquid crystal drive output	Y1 to Y320	Y1 to Y320	Output	Liquid crystal drive output: Selects and outputs level V0 or V1 according to the combination of the M signal and display data when /DISP is connected to Vcc. 

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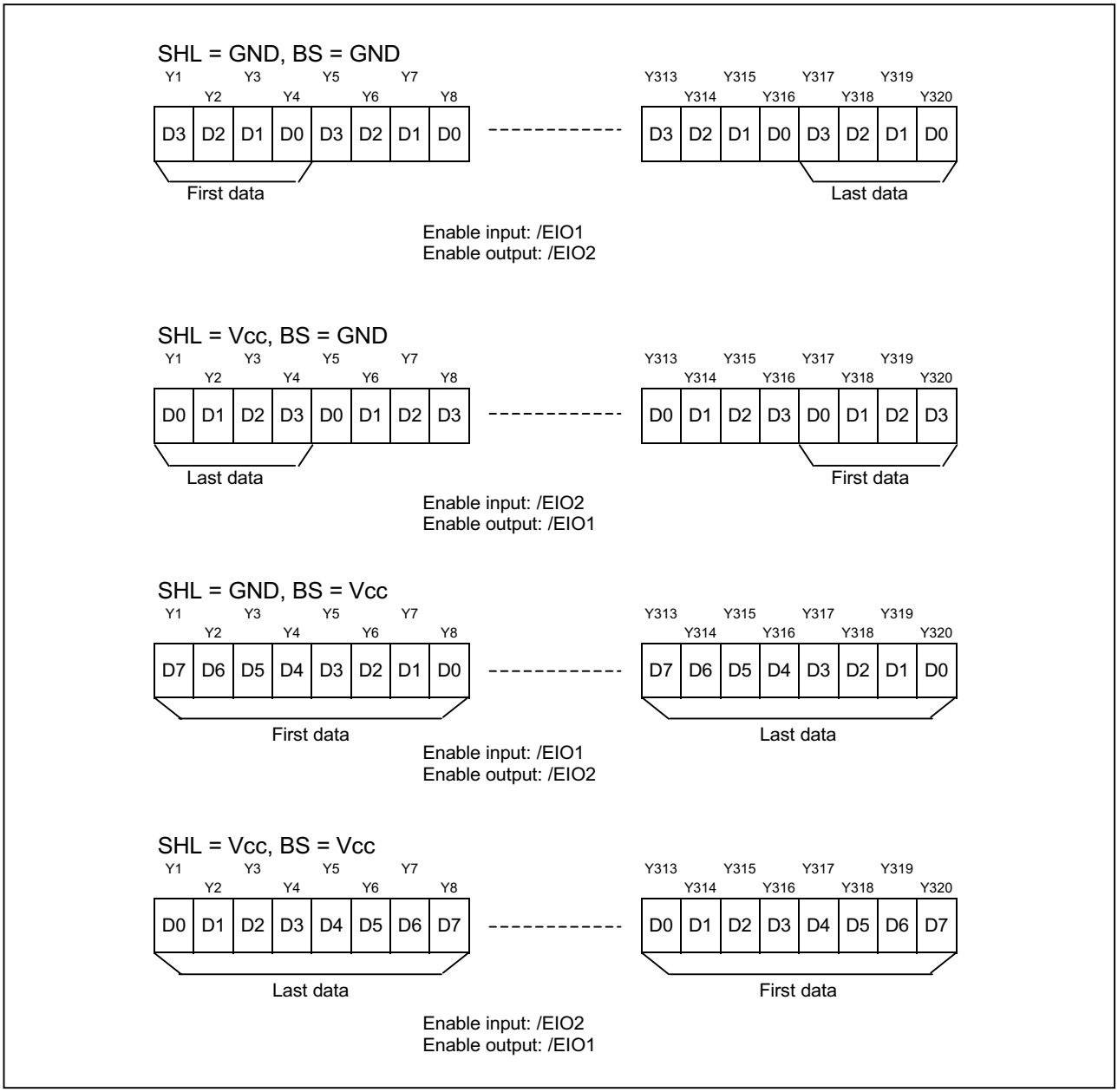
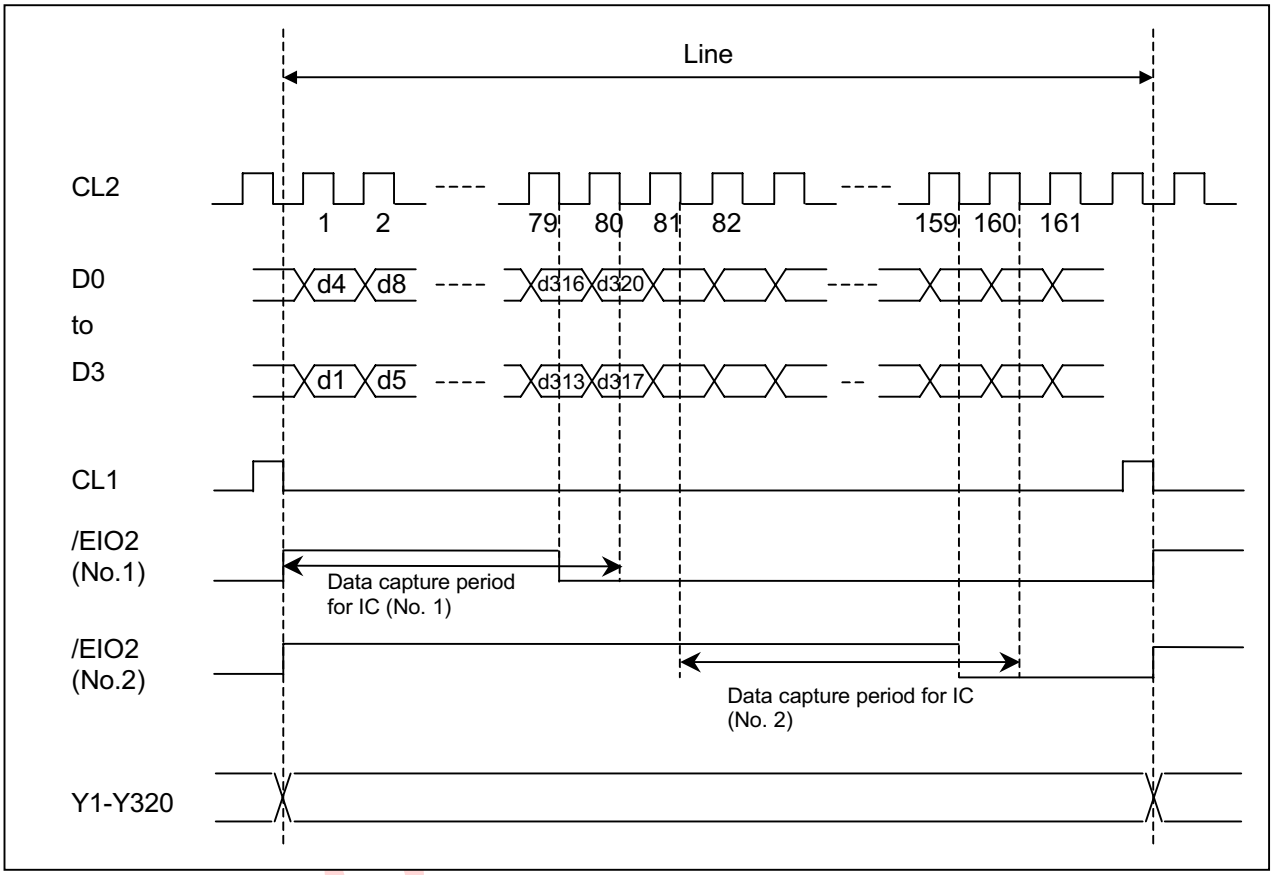
Rearranging Output Data (SHL)

The order for the output of captured data is inverted crosswise according to the SHL signal. At this time, the input/output pin of the enable signal can be switched.



Operation Timing

(1) 4-bit capture mode (1 line, 640 dots)



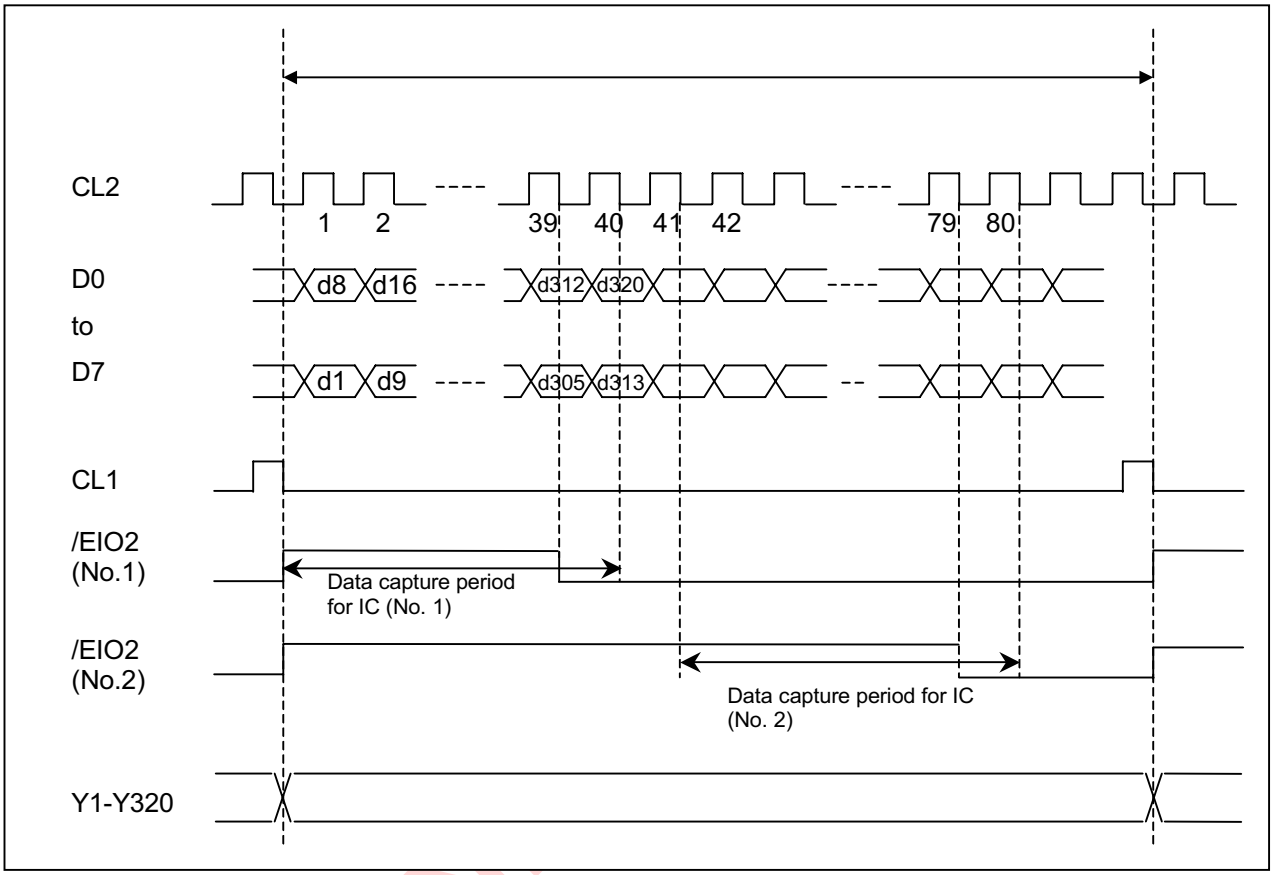
BS = GND (4-bit capture mode)

During the data standby state when the data capture operation enable signal is low (SHL = GND: /EIO1), the next data capture clock (CL2) cancels the standby state. The 4-bit data is captured at the fall of CL2. when 316 bits are captured, the enable signal becomes the GND level (SHL = GND: /EIO2). When 320 bits are captured, the operation automatically stops (the standby state is entered). The second IC is then activated when pin /EIO2 is connected to pin /EIO1 of the second IC.

Data output changes at the fall of CL1.

During SHL = GND, captured data d1 and d320 are output to Y1 and Y320, respectively. During SHL = Vcc, data d1 and d320 are output to Y320 and Y1, respectively.

(2) 8-bit capture mode (1 line, 640 dots)



BS = Vcc (8-bit capture mode)

The 8-bit display data is captured at the fall of CL2. Other basic operations are the same as those of the 4-bit capture mode.

Application Example

Application Example

Figure 1 shows an application example of 320 x 3(color) x 240 dot Quarter VGA Size STN color panel. This panel consist on IST3032 x 1 piece and IST3033 x 3 pieces.
IST3032 generate M signal and DOC signal. M signal pin is connected M signal pin of IST3033 and DOC signal pin is connected DISP signal pin of IST3033
IST3032 is able to generates minus voltage by external capacitor, CO.
VEO pin is connected VEE pin VL pin.

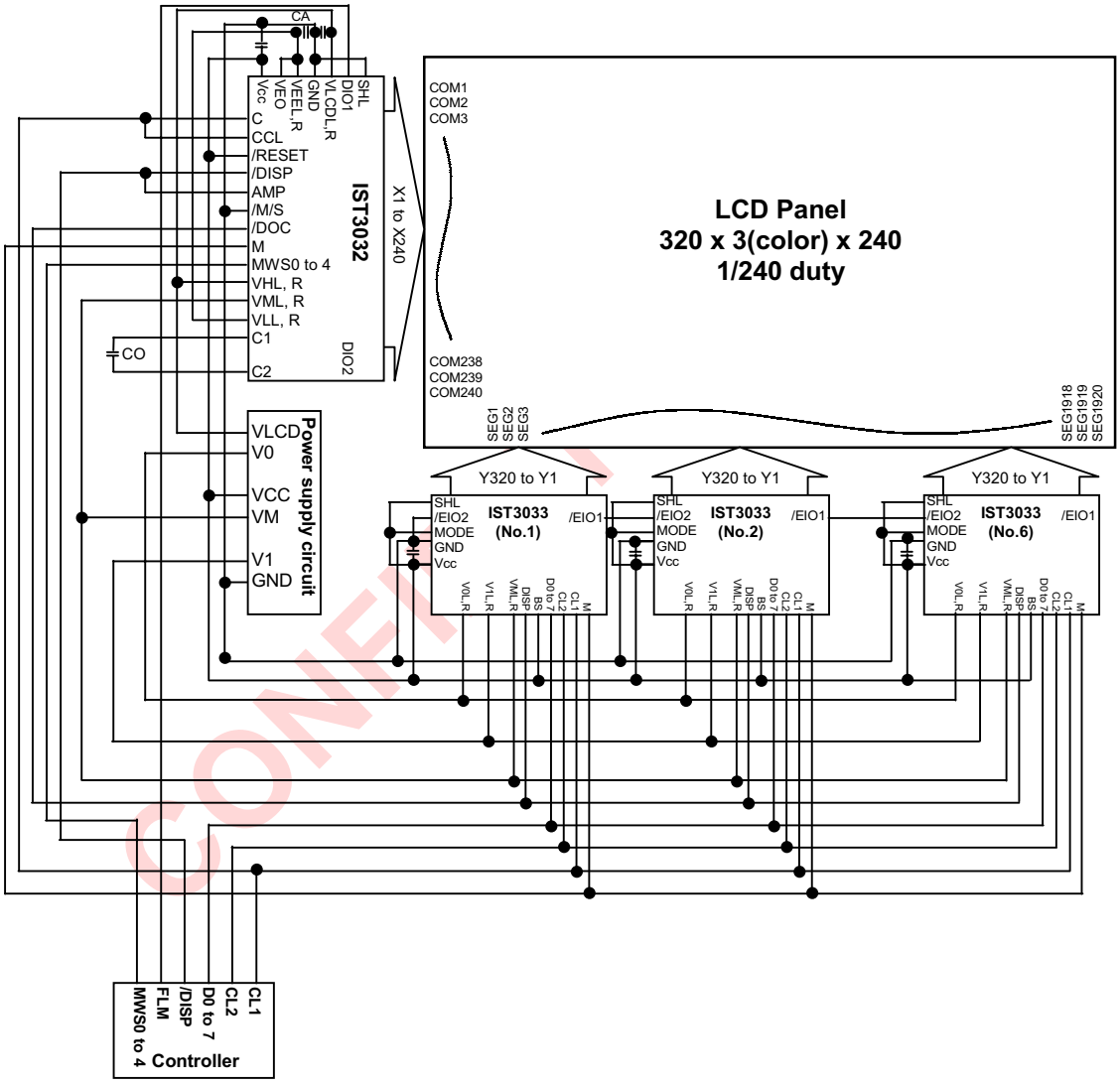


Figure 1 Application Example

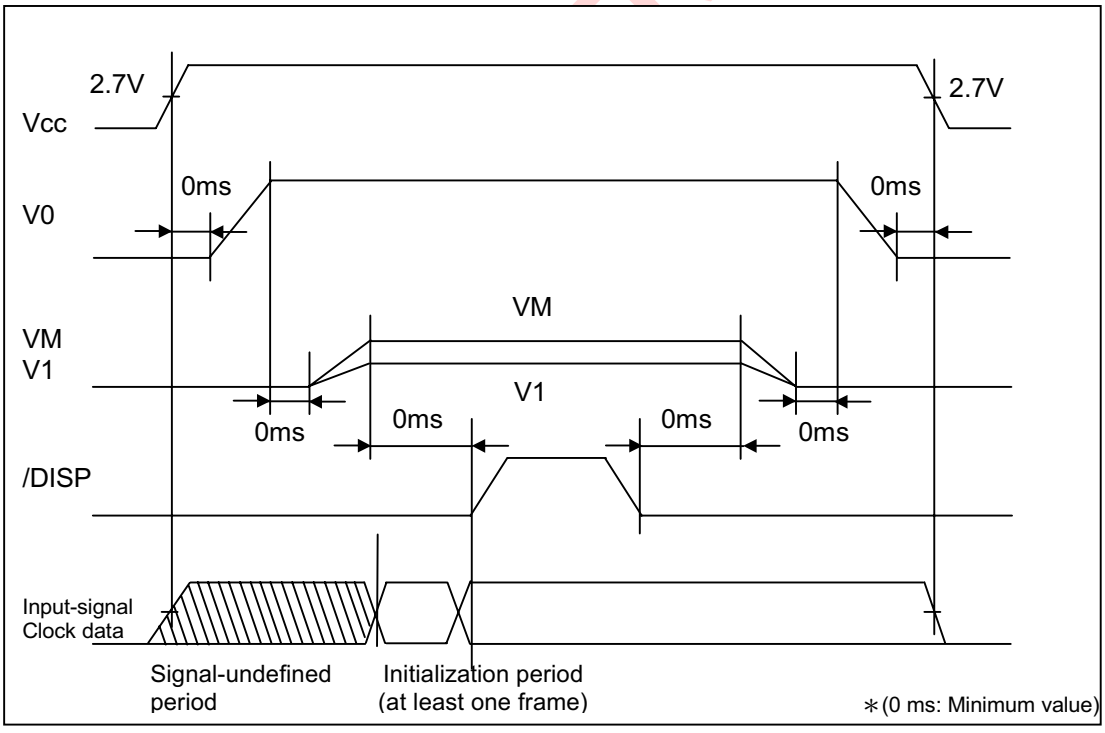
Note:

1. When designing the board, connect a capacitor near the IC to stabilize power supply. Use two capacitors of about 0.1 µF for each IC, between Vcc and GND, V0 and GND, VLCD and GND, and VEE and GND.
2. In addition, for the power supply circuit, connect a capacitor of several µF or several tens of µF between the drive power supply and level power supply in the period between when the liquid-crystal drive power supply is turned on and when it is turned off.
3. when using external capacitor, CO to generate VEE, connect a capacitor of several µF or several tens of µF between the VEE and GND.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	-0.3 to +7.0	V	1,4
Power supply voltage for LCD drive circuits	V0	-0.3 to +7.0	V	1,4
Input voltage 1	VT1	-0.3 to V_{cc} +0.3	V	1,2
Input voltage 2	VT2	-0.3 to V0 +0.3	V	1,3,4
Operating temperature	T_{opr}	-30 to +75	℃	
Storage temperature	T_{stg}	-55 to +110	℃	

Notes: 1. Potential from the GND
2. Applied to pins SHL, /EIO1, /EIO2, /DISP, D0 to D7, CL1, CL2, M, BS, and MODE.
3. Applied to VML, VMR, V1L, and VMR.
   Operating the LSI in excess of the absolute maximum rating will result in permanent damage. Use the LSI observing electrical characteristic conditions in normal operation. Exceeding the conditions will cause malfunctions or will affect LSI reliability.
4. Conform to the following turn-on/off sequence of the power and signals. Otherwise, the LSI will malfunction or will be permanently damaged. In addition, LSI reliability will be affected.



4.1 Turning on the power

1) Turn on the power in the order of GND- V_{CC}, GND-V0, and VM/V1. Then, ground the /DISP pin.
2) The LCD forcibly outputs the VM level by the DISPOFF function.
3) Even if an input signal is disturbed immediately after V_{CC} is applied, the DISPOFF function has priority.
4) Input the specific signal to initialize registers in the driver. The initialization period must be at least one frame.
5) The preparation of normal display is completed. Input the V_{CC} level to the /DISP pin to cancel the DISPOFF function. At this time, the level of pins V0, VM, and V1 must rise to the specific potential.

4.2 Turning off the power

The procedure is basically the reverse for turning on the power.

1) Ground the /DISP pin.
2) Turn off the liquid crystal power in the order of VM/V1 and GND-V0.
3) Ground V_{CC} and an input signal.

At this time, the level of pins V0, VM, and V1 must fall to 0 V. Since the DISPOFF function stops when V_{CC} falls to 0 V, the LCD may output a level other than VM. Therefore, a display failure may occur when the power is turned off or on.

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Electrical Characteristics

DC Characteristics 1 (V_{CC} = 2.5 to 4.5V, V0-GND = 2.6 to 4.5V, Ta = -30 to +75℃)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	VIH	CL1, CL2, SHL, M, /EIO1, /EIO2, MODE, /DISP, D0 to D7, BS	0.8xV_{CC}	-	V_{CC}	V		
Input low voltage	VIL		0	-	0.2xV_{CC}	V		
Output high voltage	VOH	/EIO1, /EIO2	V_{CC} –0.4	-	-	V	I_{OH}=-0.4mA	
Output low voltage	VOL	/EIO1, /EIO2	-	-	0.4	V	I_{OL}=0.4mA	
Vi-Yj on resistance	R_{ON}	Y1 to Y320, V0L, R	-	0.7	2.0	KΩ	I_{ON}=150μA	1
		Y1 to Y320, VML, R	-	2.0	3.0	KΩ		
		Y1 to Y320, V1L, R	-	0.7	2.0	KΩ		
Input leakage current 1	I_{IL1}	CL1, CL2, SHL, M, /EIO1, /EIO2, MODE, /DISP, D0 to D7, BS	-5.0		5.0	μA	VIN=V_{CC} to GND	
Input leakage current 2	I_{IL2}	VML,R, V1L, R	-25		25	μA	VIN=V0 to GND	
Current consumption 1	I_{CC}	V_{CC}	-	150	300	μA	V_{CC}=3.3V V0=2.7V f_{CL2}=3.5MHz f_{CL1}=19.2KHz f_M=1.5KHz	2
Current consumption 2	IV0	V0L, R	-	60	200	μA		
Current consumption 3	I_{ST}	V_{CC}	-	50	100	μA		2,3

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DC Characteristics 2 (V_{CC} = 4.5 to 5.5V, V0-GND = 2.6 to 4.5V, Ta = -30 to +75℃)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	VIH	CL1, CL2, SHL, M, /EIO1, /EIO2, MODE, /DISP, D0 to D7, BS	0.8xV_{CC}	-	V_{CC}	V		
Input low voltage	VIL		0	-	0.2xV_{CC}	V		
Output high voltage	VOH	/EIO1, /EIO2	V_{CC} –0.4	-	-	V	I_{OH}=-0.4mA	
Output low voltage	VOL	/EIO1, /EIO2	-	-	0.4	V	I_{OL}=0.4mA	
Vi-Yj on resistance	R_{ON}	Y1 to Y320, V0L, R	-	0.7	2.0	KΩ	I_{ON}=150μA	1
		Y1 to Y320, VML, R	-	2.0	3.0	KΩ		
		Y1 to Y320, V1L, R	-	0.7	2.0	KΩ		
Input leakage current 1	I_{IL1}	CL1, CL2, SHL, M, /EIO1, /EIO2, MODE, /DISP, D0 to D7, BS	-5.0		5.0	μA	VIN=V_{CC} to GND	
Input leakage current 2	I_{IL2}	VML, R, V1L, R	-25		25	μA	VIN=V0 to GND	
Current consumption 1	I_{CC}	V_{CC}	-	230	450	μA	V_{CC}=5.0V V0=2.7V f_{CL2}=3.5MHz f_{CL1}=19.2KHz f_M=1.5KHz	2
Current consumption 2	IV0	V0L, R	-	60	200	μA		
Current consumption 3	I_{ST}	V_{CC}	-	80	150	μA		2,3

Notes: 1. Resistance between pins Y and V when a load current flows to one of the pins from Y1 to Y320.
The following conditions are defined:
V0-GND = 4.5 V
VM = (V0 + V1)/2
V1 = GND + 1.0

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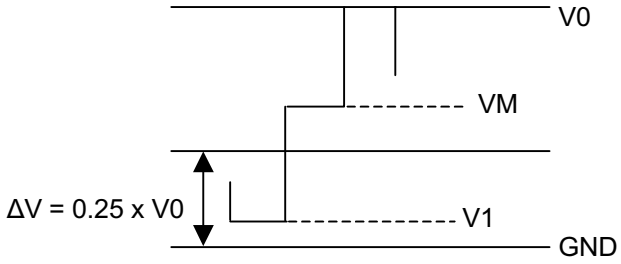
The voltage range of the liquid crystal drive level power supply is described. A voltage around the GND is applied to pin V1, and an intermediate voltage of about V0 and V1 is applied to pin VM. Use the V1 in the range of ΔV = 0.25 x V0, in which the impedance Ron of driver output is stable.



Relationship between the driver output waveform and each level voltage

2. A current flowing in the input or output section is excluded. If an input signal is at an intermediate level for the CMOS, a through-current flows in the input circuit and power supply current increases. Therefore, VIH must be at the V_{CC} level and VIL must be at the GND level.
3. Current at standby
4. The voltage of each signal is shown below.

Segment voltage	Segment waveform		Common waveform		Common voltage
V0 (4.5 V) V_{CC} (3.3 V) VM (2.75V) V1 (1.0 V) GND(0.0V)					VH (22.75V) V_{CC} (3.3 V) VM (2.75V) GND(0.0V) VL(-17.25V)
	Normal display period	Display-off period	Normal display period	Display-off period	

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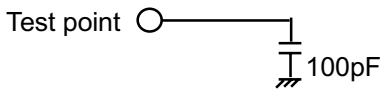
AC Characteristics 1 (V_{CC} = 2.5 to 4.5V, V0-GND = 2.6 to 4.5V, Ta = -30 to +75℃)

Item	Symbol	Pins	Min	Max	Unit
Clock cycle time	t_{CYC}	CL2	152	-	ns
Clock high pulse width 1	t_{CWH2}	CL2	65	-	ns
Clock low pulse width 1	t_{CWL2}	CL2	65	-	ns
Clock high pulse width 2	t_{CWH1}	CL1	65	-	ns
Clock setup time	t_{SCL}	CL1, CL2	80	-	ns
Clock hold time	t_{HCL}	CL1, CL2	80	-	ns
Clock rise time	t_r	CL1, CL2	-	30	ns
Clock fall time	t_f	CL1, CL2	-	30	ns
Data setup time	t_{DS}	D0 to D7, CL2	50	-	ns
Data hold time	t_{DH}	D0 to D7, CL2	50	-	ns
M setup time	t_{MS}	M, CL1	20	-	ns
M hold time	t_{MH}	M, CL1	20	-	ns
Output delay time	t_{pd1}	CL1, Y1 to Y320	-	1000	ns

AC Characteristics 2 (V_{CC} = 4.5 to 5.5V, V0-GND = 2.6 to 4.5V, Ta = -30 to +75℃)

Item	Symbol	Pins	Min	Max	Unit
Clock cycle time	t_{CYC}	CL2	125	-	ns
Clock high pulse width 1	t_{CWH2}	CL2	45	-	ns
Clock low pulse width 1	t_{CWL2}	CL2	45	-	ns
Clock high pulse width 2	t_{CWH1}	CL1	45	-	ns
Clock setup time	t_{SCL}	CL1, CL2	80	-	ns
Clock hold time	t_{HCL}	CL1, CL2	80	-	ns
Clock rise time	t_r	CL1, CL2	-	20	ns
Clock fall time	t_f	CL1, CL2	-	20	ns
Data setup time	t_{DS}	D0 to D7, CL2	20	-	ns
Data hold time	t_{DH}	D0 to D7, CL2	20	-	ns
M setup time	t_{MS}	M, CL1	20	-	ns
M hold time	t_{MH}	M, CL1	20	-	ns
Output delay time	t_{pd1}	CL1, Y1 to Y320	-	1000	ns

Notes: 1. A load must be 10pF or less for EI/O connection between drivers.
2. For output delay time, connect the load circuit shown below.



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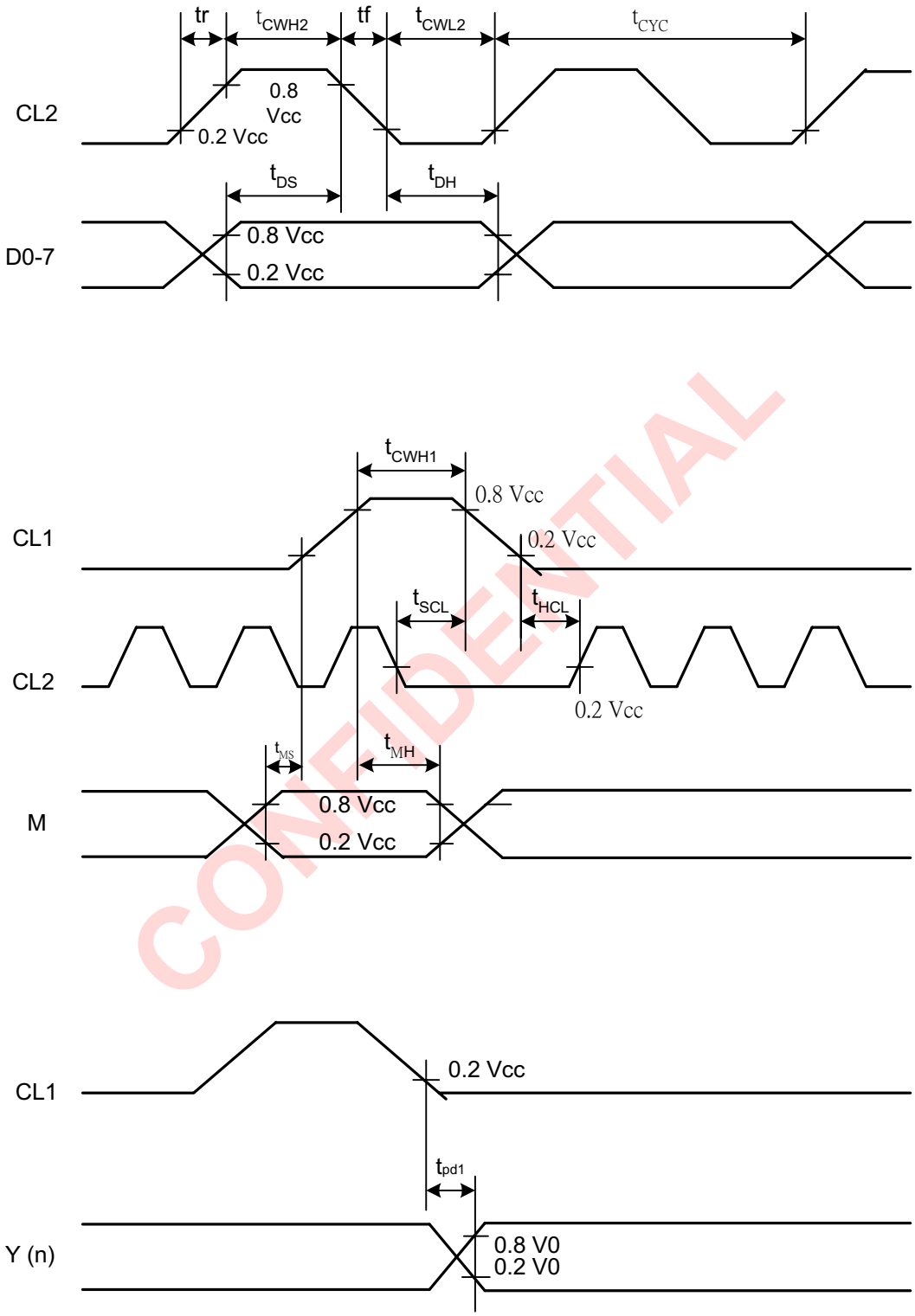

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