



S6B3301

Rev. 1.20

MOBILE DISPLAY DRIVER IC

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Samsung Electronics Co., Ltd.
San #24 Nongseo-Dong, Giheung-Gu,
Yongin-City, Gyeonggi-Do, Korea
446-711

<http://www.samsung.com/Products/Semiconductor/DisplayDriverIC>

IMPORTANT NOTICE!!

Precautions against Light

The conductivity of a semiconductor is strongly influenced by eletro-magnetic radiation such as visible light, infrared light, ultraviolet light, or gamma radiation. When light is absorbed, electron-hole pairs are generated raising the conductivity of the material, eventually altering the electrical characteristics of the IC. Therefore, if the packages that expose IC's to external light sources, such as COB, COG, TCP, and COF, are used, effective means to shield the IC from the light coming in all directions – top, bottom, and the sides – must be devised. Full observation of the following precautions is strongly recommended.

1. Make sure that the IC and substrate (board or glass) are protected from a stray light.
2. Always test and inspect products under the environment with no of light penetration.

Revision History

Ver.	Date	History
0.00	2006-11-02	Original
0.10	2006-11-15	Add PAD configuration and coordinates
0.20	2006-11-22	<ol style="list-style-type: none"> 1. Modify "table1. S6B3301 PAD dimensions" (Page 12) 2. Modify "Figure3. COG Align Key coordination" (Page 13) 3. Modify " DC CHARATERISTIC(3) " (Page 73) 4. Modify "P_MTP voltage tolerance " (Page 85) 5. Modify "Figure22. Figure23, Table28" (Page 86~88)
0.30	2007-01-28	<ol style="list-style-type: none"> 1. Modify instruction name from Test Key Command to Preliminary instruction 2. Delete VDD description (Page 10, 68) 3. Add TEST[2:0], C21P, C31M PAD in Pin description (Page 23) 4. Add Frame Frequency instruction (Page 36, 53, 57) 5. Delete "DC-DC Select and power supply for V1 Op-Amp" 6. Modify "9.8 Standby Mode ON" → SEG, VRP states (Page 41)
0.31	2007-02-02	Modify "Figure22. Application Circuit"
0.32	2007-03-06	Modify "PIN CONFIGRATION" (Page 14)
0.33	2007-03-21	Modify "Frame Frequency Set " (Page 53)
0.40	2007-04-04	<ol style="list-style-type: none"> 1. Modify "Instruction Description " (Page 36, 52, 57) → Add "Booster Boosting Ratio Set (70h)" Command 2. Modify "DC CHARACTERISTICS(1) " (Page 69~71) → Add V1,VCC,VEE Output Graph as VIN1 sweep 3. Modify "DC CHARACTERISTICS(3)" (Page 73) → Modify VRP Condition to " Isource=20uA" → Modify VRN Condition to " Isink=20uA" 4. Modify "System Application Diagram" (Page 86) → Add a Capacitor at VOUT45,VIN45 → Insert a Capacitor 'C2' as Item "VOUT45-GND" (Page 88)
0.50	2007-06-27	<ol style="list-style-type: none"> 1. Modify "figure3. COG Align Key Coordinate" (Page 13) 2. Add VSS3 description (Page 20) 3. Modify "Partial Display Start/End Line Set" (Page 50) → Delete the words, '+2'. 4. Modify "Booster Boosting Set" (Page 52) → Modify the range of boosting set (Delete x3 and comment 'Don't Use') 5. Modify "table 22. instruction parameter" (Page 57) → Modify initial value of 7FH instruction to '40h' 6. Modify "DC CHARACTERISTICS(1)" → Delete the 'VIN2' item. (Page 69) → Modify the note *2. (Page 69) → Modify the boosting graph. (Page 70~71) 7. Modify "P_MTP voltage tolerance" (Page 85) → Modify the P_MTP supply voltage from '20V' to '18V'
1.00	2007-08-01	<ol style="list-style-type: none"> 1. Modify TBD → Modify "Low Power Consumption" TBD value to 900μA Typ. (Page 10) → Modify "Oscillator Frequency Tolerance" TBD value. (Page 69) → Modify "Current Consumption" item's condition, typ, max column TBD value and Modify fFR value. (Page 72)

		<p>2. Modify "10.1 Power on sequence" (Page 59) -> Modify the wait time from 120ms to 200ms after standby mode off.</p> <p>3. Modify "10.5 Wake up sequence" (Page 63) -> Modify the wait time from 180ms to 300ms after standby mode off.</p> <p>4. Modify "DC CHARACTERISTICS(1)" (Page 69) -> Modify "Oscillator Frequency Tolerance" 's condition. -> Delete "Oscillator Frequency Range" item and note.</p> <p>5. Modify "Table 28. External component" (Page 88) -> Modify the C2,C3,C4,C5,C6 capacitors value from "1.0 to 2.2μF" to "1.0μF".</p>
1.10	2007-11-26	<p>1. Modify "Load current condition" (Page 74) -> Correct the wrong typing, "Load current condition" of " VRP-VM - VM-VRN ".</p> <p>2. Modify "13.4 MTP Erase sequence", "13.5 MTP Write sequence" (Page 83,84) -> Correct the wrong typing, "P_MTP supply voltage" from 20V to 18V.</p>
1.20	2008-03-28	<p>1. Modify "Table.2 PAD Center Coordinates" (Page 15) -> Correct the wrong typing of "DB<13>" pin number from "2" to "69".</p>

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1. INTRODUCTION

S6B3301 is a mid-display-size-compatible driver for liquid crystal dot matrix gray-scale graphic systems. With on-chip RC oscillator circuit, the display-timing signal is generated without being sent from MPU. Also, it is capable of using 8bit/16bit data bus alternatively and operating with 68/80-series MPU in asynchronous. Due to the LCD driving signal (132 RGB X 132 output) corresponding to the display data and the internal bit-map display RAM of 132 ×132 ×16-bit, S6B3301 is capable of operating max. 132 RGB x 132 dot LCD panels in low-power consumption. Being the segment RGB 3-output, one pixel is 16-bit data and S6B3301 can max display 65,536 color.

2. FEATURES

- **Driver Output**
 - 132 RGB x 132
- **Gray Scale Function**
 - 65,536 color display of R: 32 gray scale, G: 64 gray scale, B: 32 gray scale
 - 4,096 color display of R: 16 gray scale, G: 16 gray scale, B: 16 gray scale
- **On-chip Display Data RAM**
 - Capacity: 132 x 16 x 132 = 278.784k bits
- **Display Mode**
 - Normal display mode : Entire duty displaying
 - Partial display mode : Partial duty displaying
 - Standby mode : Internal display clocks off
- **MPU (Microprocessor) Interface**
 - 8-bit/16 bit parallel bi-directional interface with 6800-series or 8080-series
 - 3/4 Pin SPI (only write operation)
- **On-chip Low Power Analog Circuit**
 - On-chip RC oscillator (Internal cap. & resistor), external clock available
 - Voltage converter / Voltage regulator / Voltage follower
 - On-chip electronic contrast control
- **Operating Voltage Range**
 - VDD3 = 1.65 to 3.0 [V]
 - VIN1: 2.4 to 3.0 [V], VIN1R: 2.4 to 3.0 [V]
 - Display operating voltage(V1): 2.8 to 4.0 [V]
- **Low Power Consumption**
 - 900 μ A Typ. (Refer to DC CHARACTERISTICS (2))
- **Package Type**
 - COG (Output Pad Pitch Min. 24, 30 μ m)

3. BLOCK DIAGRAM

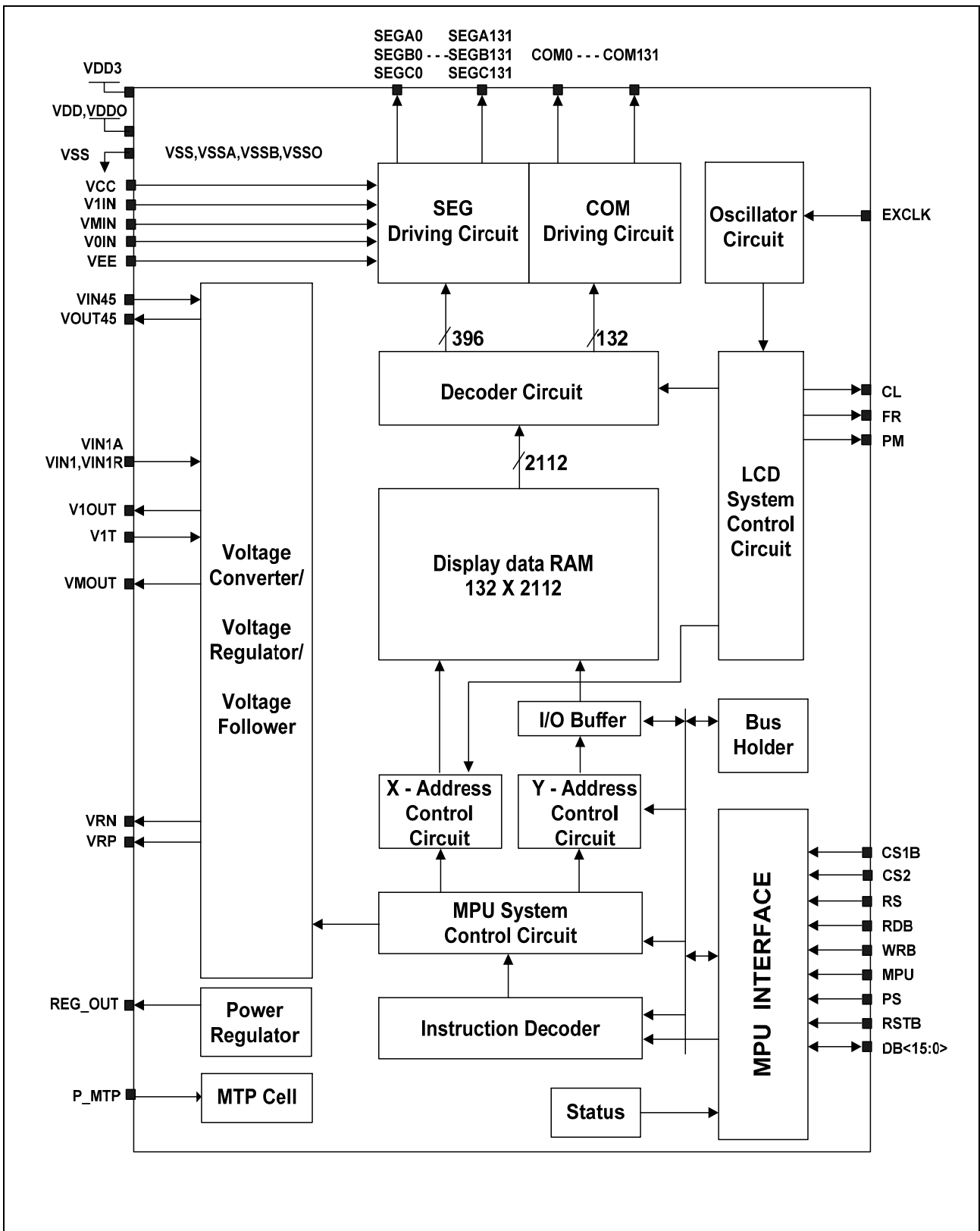


Figure 1. Block Diagram

4. PAD CONFIGURATION

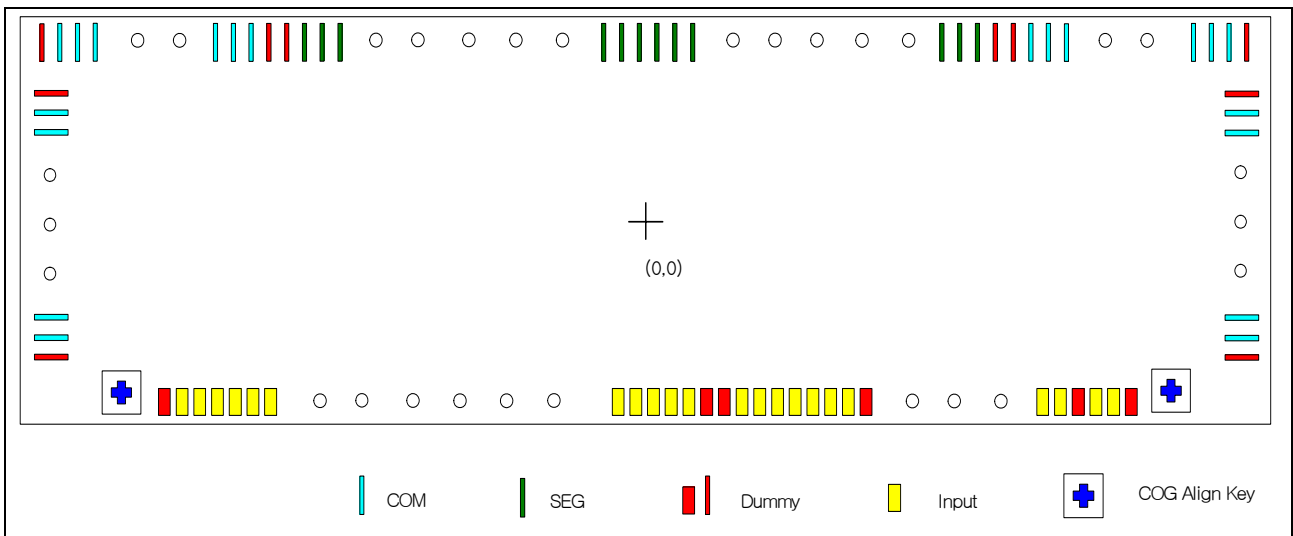


Figure 2. S6B3301 Chip Pad Configuration

Table 1. S6B3301 Pad Dimensions

ITEM	PAD NO.	SIZE		UNIT
		X	Y	
CHIP SIZE (with S/L 80 μm)	-	12240	780	μm
PAD PITCH	1 ~ 43, 47 ~ 55, 72 ~ 156	60		
	43 ~ 44, 46 ~ 47, 55 ~ 56, 71 ~ 72	80		
	44 ~ 46, 56 ~ 71	100		
	157 ~ 173, 680 ~ 696	30		
	174 ~ 679	24		
BUMPED PAD TOP SIZE	1 ~ 43, 47 ~ 55, 72 ~ 156	40±2	40±2	
	44 ~ 46, 56 ~ 71	80±2	40±2	
	157 ~ 173, 680 ~ 696	77±2	17±2	
	174 ~ 679	13±2	100±2	
BUMPED PAD HEIGHT	All pad	15±3		

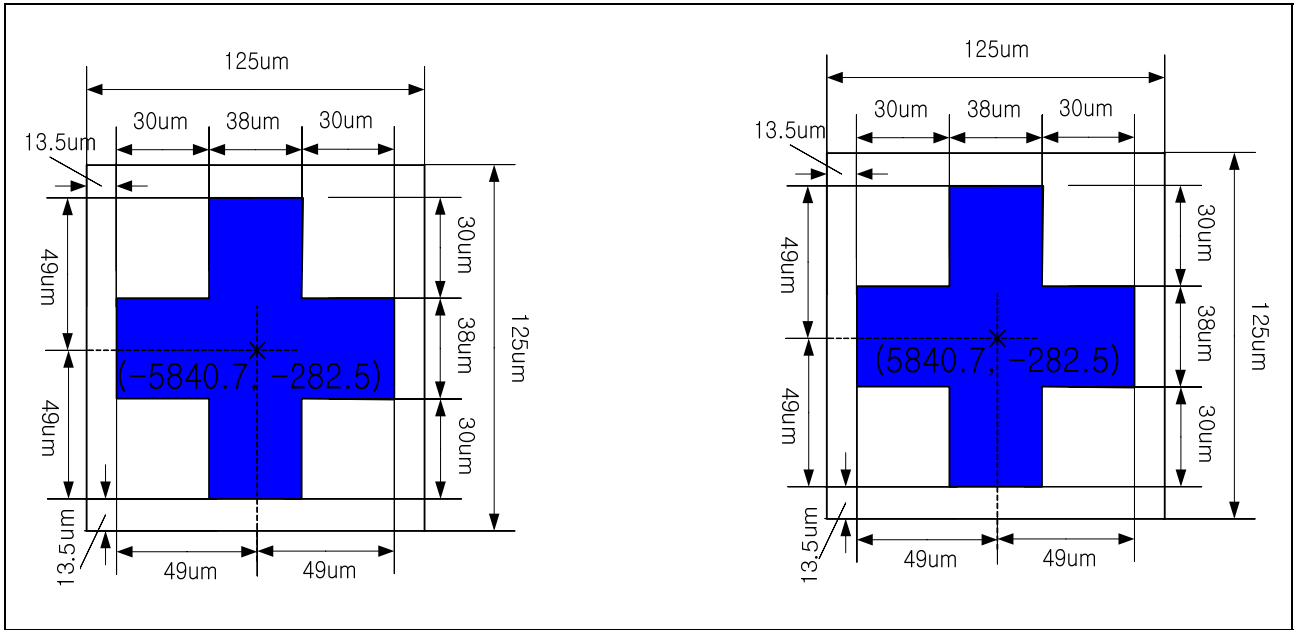


Figure 3. COG Align Key Coordinate

* NOTE : When designing COG pattern, ITO pattern must be prohibited on BUMP, COG Align Keys, DUMMY pads, TEST pads. If ITO pattern is used for routing over these areas, it can be happened pattern-short through bumped pattern on these areas.

6. PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
1	DUMMY<1>	-5,030.0	-323.0	51	RDB	-1,910.0	-323.0	101	VSSB	1,730.0	-323.0
2	P_MTP	-4,970.0	-323.0	52	VDD3	-1,850.0	-323.0	102	VSSB	1,790.0	-323.0
3	P_MTP	-4,910.0	-323.0	53	TEST<2>	-1,790.0	-323.0	103	VSSB	1,850.0	-323.0
4	VOIN	-4,850.0	-323.0	54	TEST<1>	-1,730.0	-323.0	104	VSSB	1,910.0	-323.0
5	VOIN	-4,790.0	-323.0	55	TEST<0>	-1,670.0	-323.0	105	VSSB	1,970.0	-323.0
6	RTEST	-4,730.0	-323.0	56	DB<0>	-1,590.0	-323.0	106	VSSB	2,030.0	-323.0
7	VSS3	-4,670.0	-323.0	57	DB<1>	-1,490.0	-323.0	107	VSSB	2,090.0	-323.0
8	REG_OUT	-4,610.0	-323.0	58	DB<2>	-1,390.0	-323.0	108	VIN1R	2,150.0	-323.0
9	REG_OUT	-4,550.0	-323.0	59	DB<3>	-1,290.0	-323.0	109	VIN1R	2,210.0	-323.0
10	VDDO	-4,490.0	-323.0	60	DB<4>	-1,190.0	-323.0	110	VIN1R	2,270.0	-323.0
11	VDDO	-4,430.0	-323.0	61	DB<5>	-1,090.0	-323.0	111	VIN1R	2,330.0	-323.0
12	VDD	-4,370.0	-323.0	62	DB<6>	-990.0	-323.0	112	VIN1A	2,390.0	-323.0
13	VDD	-4,310.0	-323.0	63	DB<7>	-890.0	-323.0	113	VIN1A	2,450.0	-323.0
14	VDD	-4,250.0	-323.0	64	DB<8>	-790.0	-323.0	114	VIN1A	2,510.0	-323.0
15	VDD	-4,190.0	-323.0	65	DB<9>	-690.0	-323.0	115	VIN1A	2,570.0	-323.0
16	VDD	-4,130.0	-323.0	66	DB<10>	-590.0	-323.0	116	VIN1A	2,630.0	-323.0
17	VDD	-4,070.0	-323.0	67	DB<11>	-490.0	-323.0	117	VIN1A	2,690.0	-323.0
18	VDD3	-4,010.0	-323.0	68	DB<12>	-390.0	-323.0	118	VIN1	2,750.0	-323.0
19	VDD3	-3,950.0	-323.0	69	DB<13>	-290.0	-323.0	119	VIN1	2,810.0	-323.0
20	VDD3	-3,890.0	-323.0	70	DB<14>	-190.0	-323.0	120	VIN1	2,870.0	-323.0
21	VDD3	-3,830.0	-323.0	71	DB<15>	-90.0	-323.0	121	VIN1	2,930.0	-323.0
22	VDD3	-3,770.0	-323.0	72	VSS3	-10.0	-323.0	122	VIN1	2,990.0	-323.0
23	VDD3	-3,710.0	-323.0	73	PS	50.0	-323.0	123	VIN1	3,050.0	-323.0
24	FUSE_EN	-3,650.0	-323.0	74	VDD3	110.0	-323.0	124	VIN1	3,110.0	-323.0
25	V1IN	-3,590.0	-323.0	75	MPU	170.0	-323.0	125	VIN1	3,170.0	-323.0
26	V1IN	-3,530.0	-323.0	76	VSS3	230.0	-323.0	126	VIN1	3,230.0	-323.0
27	V1IN	-3,470.0	-323.0	77	CS2	290.0	-323.0	127	VIN1	3,290.0	-323.0
28	V1IN	-3,410.0	-323.0	78	VDD3	350.0	-323.0	128	VIN1	3,350.0	-323.0
29	V1IN	-3,350.0	-323.0	79	CS1B	410.0	-323.0	129	VIN1	3,410.0	-323.0
30	V1IN	-3,290.0	-323.0	80	VSSO	470.0	-323.0	130	VIN45	3,470.0	-323.0
31	V1OUT	-3,230.0	-323.0	81	VSSO	530.0	-323.0	131	VIN45	3,530.0	-323.0
32	V1OUT	-3,170.0	-323.0	82	VSS	590.0	-323.0	132	VOUT45	3,590.0	-323.0
33	V1T	-3,110.0	-323.0	83	VSS	650.0	-323.0	133	VOUT45	3,650.0	-323.0
34	VMOUT	-3,050.0	-323.0	84	VSS	710.0	-323.0	134	C21P	3,710.0	-323.0
35	VMOUT	-2,990.0	-323.0	85	VSS	770.0	-323.0	135	C31M	3,770.0	-323.0
36	VMIN	-2,930.0	-323.0	86	VSS	830.0	-323.0	136	DUMMY<2>	3,830.0	-323.0
37	VMIN	-2,870.0	-323.0	87	VSS	890.0	-323.0	137	DUMMY<3>	3,890.0	-323.0
38	MODE<1>	-2,810.0	-323.0	88	VSS	950.0	-323.0	138	VRN	3,950.0	-323.0
39	MODE<0>	-2,750.0	-323.0	89	VSSA	1,010.0	-323.0	139	VRN	4,010.0	-323.0
40	EXCLK	-2,690.0	-323.0	90	VSSA	1,070.0	-323.0	140	VRN	4,070.0	-323.0
41	VDD3	-2,630.0	-323.0	91	VSSA	1,130.0	-323.0	141	VEE	4,130.0	-323.0
42	ZIGZAG_MODE	-2,570.0	-323.0	92	VSSA	1,190.0	-323.0	142	VEE	4,190.0	-323.0
43	VSS3	-2,510.0	-323.0	93	VSSA	1,250.0	-323.0	143	VEE	4,250.0	-323.0
44	CL	-2,430.0	-323.0	94	VSSA	1,310.0	-323.0	144	VEE	4,310.0	-323.0
45	PM	-2,330.0	-323.0	95	VSSA	1,370.0	-323.0	145	DUMMY<4>	4,370.0	-323.0
46	FR	-2,230.0	-323.0	96	VSSB	1,430.0	-323.0	146	VCC	4,430.0	-323.0
47	RSTB	-2,150.0	-323.0	97	VSSB	1,490.0	-323.0	147	VCC	4,490.0	-323.0
48	RS	-2,090.0	-323.0	98	VSSB	1,550.0	-323.0	148	VCC	4,550.0	-323.0
49	VSS3	-2,030.0	-323.0	99	VSSB	1,610.0	-323.0	149	VCC	4,610.0	-323.0
50	WRB	-1,970.0	-323.0	100	VSSB	1,670.0	-323.0	150	VRP	4,670.0	-323.0

Table 3. Pad Center Coordinates (Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
151	VRP	4,730.0	-323.0	201	COM<41>	5,412.0	293.0	251	SEGB<7>	4,212.0	293.0
152	VRP	4,790.0	-323.0	202	COM<42>	5,388.0	293.0	252	SEGA<7>	4,188.0	293.0
153	DUMMY<5>	4,850.0	-323.0	203	COM<43>	5,364.0	293.0	253	SEGC<8>	4,164.0	293.0
154	VOIN	4,910.0	-323.0	204	COM<44>	5,340.0	293.0	254	SEGB<8>	4,140.0	293.0
155	VOIN	4,970.0	-323.0	205	COM<45>	5,316.0	293.0	255	SEGA<8>	4,116.0	293.0
156	DUMMY<6>	5,030.0	-323.0	206	COM<46>	5,292.0	293.0	256	SEGC<9>	4,092.0	293.0
157	DUMMY<7>	6,034.5	-330.0	207	COM<47>	5,268.0	293.0	257	SEGB<9>	4,068.0	293.0
158	COM<0>	6,034.5	-300.0	208	COM<48>	5,244.0	293.0	258	SEGA<9>	4,044.0	293.0
159	COM<1>	6,034.5	-270.0	209	COM<49>	5,220.0	293.0	259	SEGC<10>	4,020.0	293.0
160	COM<2>	6,034.5	-240.0	210	COM<50>	5,196.0	293.0	260	SEGB<10>	3,996.0	293.0
161	COM<3>	6,034.5	-210.0	211	COM<51>	5,172.0	293.0	261	SEGA<10>	3,972.0	293.0
162	COM<4>	6,034.5	-180.0	212	COM<52>	5,148.0	293.0	262	SEGC<11>	3,948.0	293.0
163	COM<5>	6,034.5	-150.0	213	COM<53>	5,124.0	293.0	263	SEGB<11>	3,924.0	293.0
164	COM<6>	6,034.5	-120.0	214	COM<54>	5,100.0	293.0	264	SEGA<11>	3,900.0	293.0
165	COM<7>	6,034.5	-90.0	215	COM<55>	5,076.0	293.0	265	SEGC<12>	3,876.0	293.0
166	COM<8>	6,034.5	-60.0	216	COM<56>	5,052.0	293.0	266	SEGB<12>	3,852.0	293.0
167	COM<9>	6,034.5	-30.0	217	COM<57>	5,028.0	293.0	267	SEGA<12>	3,828.0	293.0
168	COM<10>	6,034.5	0.0	218	COM<58>	5,004.0	293.0	268	SEGC<13>	3,804.0	293.0
169	COM<11>	6,034.5	30.0	219	COM<59>	4,980.0	293.0	269	SEGB<13>	3,780.0	293.0
170	COM<12>	6,034.5	60.0	220	COM<60>	4,956.0	293.0	270	SEGA<13>	3,756.0	293.0
171	COM<13>	6,034.5	90.0	221	COM<61>	4,932.0	293.0	271	SEGC<14>	3,732.0	293.0
172	COM<14>	6,034.5	120.0	222	COM<62>	4,908.0	293.0	272	SEGB<14>	3,708.0	293.0
173	DUMMY<8>	6,034.5	150.0	223	COM<63>	4,884.0	293.0	273	SEGA<14>	3,684.0	293.0
174	DUMMY<9>	6,060.0	293.0	224	COM<64>	4,860.0	293.0	274	SEGC<15>	3,660.0	293.0
175	COM<15>	6,036.0	293.0	225	COM<65>	4,836.0	293.0	275	SEGB<15>	3,636.0	293.0
176	COM<16>	6,012.0	293.0	226	DUMMY<10>	4,812.0	293.0	276	SEGA<15>	3,612.0	293.0
177	COM<17>	5,988.0	293.0	227	DUMMY<11>	4,788.0	293.0	277	SEGC<16>	3,588.0	293.0
178	COM<18>	5,964.0	293.0	228	DUMMY<12>	4,764.0	293.0	278	SEGB<16>	3,564.0	293.0
179	COM<19>	5,940.0	293.0	229	SEGC<0>	4,740.0	293.0	279	SEGA<16>	3,540.0	293.0
180	COM<20>	5,916.0	293.0	230	SEGB<0>	4,716.0	293.0	280	SEGC<17>	3,516.0	293.0
181	COM<21>	5,892.0	293.0	231	SEGA<0>	4,692.0	293.0	281	SEGB<17>	3,492.0	293.0
182	COM<22>	5,868.0	293.0	232	SEGC<1>	4,668.0	293.0	282	SEGA<17>	3,468.0	293.0
183	COM<23>	5,844.0	293.0	233	SEGB<1>	4,644.0	293.0	283	SEGC<18>	3,444.0	293.0
184	COM<24>	5,820.0	293.0	234	SEGA<1>	4,620.0	293.0	284	SEGB<18>	3,420.0	293.0
185	COM<25>	5,796.0	293.0	235	SEGC<2>	4,596.0	293.0	285	SEGA<18>	3,396.0	293.0
186	COM<26>	5,772.0	293.0	236	SEGB<2>	4,572.0	293.0	286	SEGC<19>	3,372.0	293.0
187	COM<27>	5,748.0	293.0	237	SEGA<2>	4,548.0	293.0	287	SEGB<19>	3,348.0	293.0
188	COM<28>	5,724.0	293.0	238	SEGC<3>	4,524.0	293.0	288	SEGA<19>	3,324.0	293.0
189	COM<29>	5,700.0	293.0	239	SEGB<3>	4,500.0	293.0	289	SEGC<20>	3,300.0	293.0
190	COM<30>	5,676.0	293.0	240	SEGA<3>	4,476.0	293.0	290	SEGB<20>	3,276.0	293.0
191	COM<31>	5,652.0	293.0	241	SEGC<4>	4,452.0	293.0	291	SEGA<20>	3,252.0	293.0
192	COM<32>	5,628.0	293.0	242	SEGB<4>	4,428.0	293.0	292	SEGC<21>	3,228.0	293.0
193	COM<33>	5,604.0	293.0	243	SEGA<4>	4,404.0	293.0	293	SEGB<21>	3,204.0	293.0
194	COM<34>	5,580.0	293.0	244	SEGC<5>	4,380.0	293.0	294	SEGA<21>	3,180.0	293.0
195	COM<35>	5,556.0	293.0	245	SEGB<5>	4,356.0	293.0	295	SEGC<22>	3,156.0	293.0
196	COM<36>	5,532.0	293.0	246	SEGA<5>	4,332.0	293.0	296	SEGB<22>	3,132.0	293.0
197	COM<37>	5,508.0	293.0	247	SEGC<6>	4,308.0	293.0	297	SEGA<22>	3,108.0	293.0
198	COM<38>	5,484.0	293.0	248	SEGB<6>	4,284.0	293.0	298	SEGC<23>	3,084.0	293.0
199	COM<39>	5,460.0	293.0	249	SEGA<6>	4,260.0	293.0	299	SEGB<23>	3,060.0	293.0
200	COM<40>	5,436.0	293.0	250	SEGC<7>	4,236.0	293.0	300	SEGA<23>	3,036.0	293.0

Table 4. Pad Center Coordinates (Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
301	SEGC<24>	3,012.0	293.0	351	SEGA<40>	1,812.0	293.0	401	SEGB<57>	612.0	293.0
302	SEGB<24>	2,988.0	293.0	352	SEGC<41>	1,788.0	293.0	402	SEGA<57>	588.0	293.0
303	SEGA<24>	2,964.0	293.0	353	SEGB<41>	1,764.0	293.0	403	SEGC<58>	564.0	293.0
304	SEGC<25>	2,940.0	293.0	354	SEGA<41>	1,740.0	293.0	404	SEGB<58>	540.0	293.0
305	SEGB<25>	2,916.0	293.0	355	SEGC<42>	1,716.0	293.0	405	SEGA<58>	516.0	293.0
306	SEGA<25>	2,892.0	293.0	356	SEGB<42>	1,692.0	293.0	406	SEGC<59>	492.0	293.0
307	SEGC<26>	2,868.0	293.0	357	SEGA<42>	1,668.0	293.0	407	SEGB<59>	468.0	293.0
308	SEGB<26>	2,844.0	293.0	358	SEGC<43>	1,644.0	293.0	408	SEGA<59>	444.0	293.0
309	SEGA<26>	2,820.0	293.0	359	SEGB<43>	1,620.0	293.0	409	SEGC<60>	420.0	293.0
310	SEGC<27>	2,796.0	293.0	360	SEGA<43>	1,596.0	293.0	410	SEGB<60>	396.0	293.0
311	SEGB<27>	2,772.0	293.0	361	SEGC<44>	1,572.0	293.0	411	SEGA<60>	372.0	293.0
312	SEGA<27>	2,748.0	293.0	362	SEGB<44>	1,548.0	293.0	412	SEGC<61>	348.0	293.0
313	SEGC<28>	2,724.0	293.0	363	SEGA<44>	1,524.0	293.0	413	SEGB<61>	324.0	293.0
314	SEGB<28>	2,700.0	293.0	364	SEGC<45>	1,500.0	293.0	414	SEGA<61>	300.0	293.0
315	SEGA<28>	2,676.0	293.0	365	SEGB<45>	1,476.0	293.0	415	SEGC<62>	276.0	293.0
316	SEGC<29>	2,652.0	293.0	366	SEGA<45>	1,452.0	293.0	416	SEGB<62>	252.0	293.0
317	SEGB<29>	2,628.0	293.0	367	SEGC<46>	1,428.0	293.0	417	SEGA<62>	228.0	293.0
318	SEGA<29>	2,604.0	293.0	368	SEGB<46>	1,404.0	293.0	418	SEGC<63>	204.0	293.0
319	SEGC<30>	2,580.0	293.0	369	SEGA<46>	1,380.0	293.0	419	SEGB<63>	180.0	293.0
320	SEGB<30>	2,556.0	293.0	370	SEGC<47>	1,356.0	293.0	420	SEGA<63>	156.0	293.0
321	SEGA<30>	2,532.0	293.0	371	SEGB<47>	1,332.0	293.0	421	SEGC<64>	132.0	293.0
322	SEGC<31>	2,508.0	293.0	372	SEGA<47>	1,308.0	293.0	422	SEGB<64>	108.0	293.0
323	SEGB<31>	2,484.0	293.0	373	SEGC<48>	1,284.0	293.0	423	SEGA<64>	84.0	293.0
324	SEGA<31>	2,460.0	293.0	374	SEGB<48>	1,260.0	293.0	424	SEGC<65>	60.0	293.0
325	SEGC<32>	2,436.0	293.0	375	SEGA<48>	1,236.0	293.0	425	SEGB<65>	36.0	293.0
326	SEGB<32>	2,412.0	293.0	376	SEGC<49>	1,212.0	293.0	426	SEGA<65>	12.0	293.0
327	SEGA<32>	2,388.0	293.0	377	SEGB<49>	1,188.0	293.0	427	SEGC<66>	-12.0	293.0
328	SEGC<33>	2,364.0	293.0	378	SEGA<49>	1,164.0	293.0	428	SEGB<66>	-36.0	293.0
329	SEGB<33>	2,340.0	293.0	379	SEGC<50>	1,140.0	293.0	429	SEGA<66>	-60.0	293.0
330	SEGA<33>	2,316.0	293.0	380	SEGB<50>	1,116.0	293.0	430	SEGC<67>	-84.0	293.0
331	SEGC<34>	2,292.0	293.0	381	SEGA<50>	1,092.0	293.0	431	SEGB<67>	-108.0	293.0
332	SEGB<34>	2,268.0	293.0	382	SEGC<51>	1,068.0	293.0	432	SEGA<67>	-132.0	293.0
333	SEGA<34>	2,244.0	293.0	383	SEGB<51>	1,044.0	293.0	433	SEGC<68>	-156.0	293.0
334	SEGC<35>	2,220.0	293.0	384	SEGA<51>	1,020.0	293.0	434	SEGB<68>	-180.0	293.0
335	SEGB<35>	2,196.0	293.0	385	SEGC<52>	996.0	293.0	435	SEGA<68>	-204.0	293.0
336	SEGA<35>	2,172.0	293.0	386	SEGB<52>	972.0	293.0	436	SEGC<69>	-228.0	293.0
337	SEGC<36>	2,148.0	293.0	387	SEGA<52>	948.0	293.0	437	SEGB<69>	-252.0	293.0
338	SEGB<36>	2,124.0	293.0	388	SEGC<53>	924.0	293.0	438	SEGA<69>	-276.0	293.0
339	SEGA<36>	2,100.0	293.0	389	SEGB<53>	900.0	293.0	439	SEGC<70>	-300.0	293.0
340	SEGC<37>	2,076.0	293.0	390	SEGA<53>	876.0	293.0	440	SEGB<70>	-324.0	293.0
341	SEGB<37>	2,052.0	293.0	391	SEGC<54>	852.0	293.0	441	SEGA<70>	-348.0	293.0
342	SEGA<37>	2,028.0	293.0	392	SEGB<54>	828.0	293.0	442	SEGC<71>	-372.0	293.0
343	SEGC<38>	2,004.0	293.0	393	SEGA<54>	804.0	293.0	443	SEGB<71>	-396.0	293.0
344	SEGB<38>	1,980.0	293.0	394	SEGC<55>	780.0	293.0	444	SEGA<71>	-420.0	293.0
345	SEGA<38>	1,956.0	293.0	395	SEGB<55>	756.0	293.0	445	SEGC<72>	-444.0	293.0
346	SEGC<39>	1,932.0	293.0	396	SEGA<55>	732.0	293.0	446	SEGB<72>	-468.0	293.0
347	SEGB<39>	1,908.0	293.0	397	SEGC<56>	708.0	293.0	447	SEGA<72>	-492.0	293.0
348	SEGA<39>	1,884.0	293.0	398	SEGB<56>	684.0	293.0	448	SEGC<73>	-516.0	293.0
349	SEGC<40>	1,860.0	293.0	399	SEGA<56>	660.0	293.0	449	SEGB<73>	-540.0	293.0
350	SEGB<40>	1,836.0	293.0	400	SEGC<57>	636.0	293.0	450	SEGA<73>	-564.0	293.0

Table 5. Pad Center Coordinates (Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
451	SEGC<74>	-588.0	293.0	501	SEGA<90>	-1,788.0	293.0	551	SEGB<107>	-2,988.0	293.0
452	SEGB<74>	-612.0	293.0	502	SEGC<91>	-1,812.0	293.0	552	SEGA<107>	-3,012.0	293.0
453	SEGA<74>	-636.0	293.0	503	SEGB<91>	-1,836.0	293.0	553	SEGC<108>	-3,036.0	293.0
454	SEGC<75>	-660.0	293.0	504	SEGA<91>	-1,860.0	293.0	554	SEGB<108>	-3,060.0	293.0
455	SEGB<75>	-684.0	293.0	505	SEGC<92>	-1,884.0	293.0	555	SEGA<108>	-3,084.0	293.0
456	SEGA<75>	-708.0	293.0	506	SEGB<92>	-1,908.0	293.0	556	SEGC<109>	-3,108.0	293.0
457	SEGC<76>	-732.0	293.0	507	SEGA<92>	-1,932.0	293.0	557	SEGB<109>	-3,132.0	293.0
458	SEGB<76>	-756.0	293.0	508	SEGC<93>	-1,956.0	293.0	558	SEGA<109>	-3,156.0	293.0
459	SEGA<76>	-780.0	293.0	509	SEGB<93>	-1,980.0	293.0	559	SEGC<110>	-3,180.0	293.0
460	SEGC<77>	-804.0	293.0	510	SEGA<93>	-2,004.0	293.0	560	SEGB<110>	-3,204.0	293.0
461	SEGB<77>	-828.0	293.0	511	SEGC<94>	-2,028.0	293.0	561	SEGA<110>	-3,228.0	293.0
462	SEGA<77>	-852.0	293.0	512	SEGB<94>	-2,052.0	293.0	562	SEGC<111>	-3,252.0	293.0
463	SEGC<78>	-876.0	293.0	513	SEGA<94>	-2,076.0	293.0	563	SEGB<111>	-3,276.0	293.0
464	SEGB<78>	-900.0	293.0	514	SEGC<95>	-2,100.0	293.0	564	SEGA<111>	-3,300.0	293.0
465	SEGA<78>	-924.0	293.0	515	SEGB<95>	-2,124.0	293.0	565	SEGC<112>	-3,324.0	293.0
466	SEGC<79>	-948.0	293.0	516	SEGA<95>	-2,148.0	293.0	566	SEGB<112>	-3,348.0	293.0
467	SEGB<79>	-972.0	293.0	517	SEGC<96>	-2,172.0	293.0	567	SEGA<112>	-3,372.0	293.0
468	SEGA<79>	-996.0	293.0	518	SEGB<96>	-2,196.0	293.0	568	SEGC<113>	-3,396.0	293.0
469	SEGC<80>	-1,020.0	293.0	519	SEGA<96>	-2,220.0	293.0	569	SEGB<113>	-3,420.0	293.0
470	SEGB<80>	-1,044.0	293.0	520	SEGC<97>	-2,244.0	293.0	570	SEGA<113>	-3,444.0	293.0
471	SEGA<80>	-1,068.0	293.0	521	SEGB<97>	-2,268.0	293.0	571	SEGC<114>	-3,468.0	293.0
472	SEGC<81>	-1,092.0	293.0	522	SEGA<97>	-2,292.0	293.0	572	SEGB<114>	-3,492.0	293.0
473	SEGB<81>	-1,116.0	293.0	523	SEGC<98>	-2,316.0	293.0	573	SEGA<114>	-3,516.0	293.0
474	SEGA<81>	-1,140.0	293.0	524	SEGB<98>	-2,340.0	293.0	574	SEGC<115>	-3,540.0	293.0
475	SEGC<82>	-1,164.0	293.0	525	SEGA<98>	-2,364.0	293.0	575	SEGB<115>	-3,564.0	293.0
476	SEGB<82>	-1,188.0	293.0	526	SEGC<99>	-2,388.0	293.0	576	SEGA<115>	-3,588.0	293.0
477	SEGA<82>	-1,212.0	293.0	527	SEGB<99>	-2,412.0	293.0	577	SEGC<116>	-3,612.0	293.0
478	SEGC<83>	-1,236.0	293.0	528	SEGA<99>	-2,436.0	293.0	578	SEGB<116>	-3,636.0	293.0
479	SEGB<83>	-1,260.0	293.0	529	SEGC<100>	-2,460.0	293.0	579	SEGA<116>	-3,660.0	293.0
480	SEGA<83>	-1,284.0	293.0	530	SEGB<100>	-2,484.0	293.0	580	SEGC<117>	-3,684.0	293.0
481	SEGC<84>	-1,308.0	293.0	531	SEGA<100>	-2,508.0	293.0	581	SEGB<117>	-3,708.0	293.0
482	SEGB<84>	-1,332.0	293.0	532	SEGC<101>	-2,532.0	293.0	582	SEGA<117>	-3,732.0	293.0
483	SEGA<84>	-1,356.0	293.0	533	SEGB<101>	-2,556.0	293.0	583	SEGC<118>	-3,756.0	293.0
484	SEGC<85>	-1,380.0	293.0	534	SEGA<101>	-2,580.0	293.0	584	SEGB<118>	-3,780.0	293.0
485	SEGB<85>	-1,404.0	293.0	535	SEGC<102>	-2,604.0	293.0	585	SEGA<118>	-3,804.0	293.0
486	SEGA<85>	-1,428.0	293.0	536	SEGB<102>	-2,628.0	293.0	586	SEGC<119>	-3,828.0	293.0
487	SEGC<86>	-1,452.0	293.0	537	SEGA<102>	-2,652.0	293.0	587	SEGB<119>	-3,852.0	293.0
488	SEGB<86>	-1,476.0	293.0	538	SEGC<103>	-2,676.0	293.0	588	SEGA<119>	-3,876.0	293.0
489	SEGA<86>	-1,500.0	293.0	539	SEGB<103>	-2,700.0	293.0	589	SEGC<120>	-3,900.0	293.0
490	SEGC<87>	-1,524.0	293.0	540	SEGA<103>	-2,724.0	293.0	590	SEGB<120>	-3,924.0	293.0
491	SEGB<87>	-1,548.0	293.0	541	SEGC<104>	-2,748.0	293.0	591	SEGA<120>	-3,948.0	293.0
492	SEGA<87>	-1,572.0	293.0	542	SEGB<104>	-2,772.0	293.0	592	SEGC<121>	-3,972.0	293.0
493	SEGC<88>	-1,596.0	293.0	543	SEGA<104>	-2,796.0	293.0	593	SEGB<121>	-3,996.0	293.0
494	SEGB<88>	-1,620.0	293.0	544	SEGC<105>	-2,820.0	293.0	594	SEGA<121>	-4,020.0	293.0
495	SEGA<88>	-1,644.0	293.0	545	SEGB<105>	-2,844.0	293.0	595	SEGC<122>	-4,044.0	293.0
496	SEGC<89>	-1,668.0	293.0	546	SEGA<105>	-2,868.0	293.0	596	SEGB<122>	-4,068.0	293.0
497	SEGB<89>	-1,692.0	293.0	547	SEGC<106>	-2,892.0	293.0	597	SEGA<122>	-4,092.0	293.0
498	SEGA<89>	-1,716.0	293.0	548	SEGB<106>	-2,916.0	293.0	598	SEGC<123>	-4,116.0	293.0
499	SEGC<90>	-1,740.0	293.0	549	SEGA<106>	-2,940.0	293.0	599	SEGB<123>	-4,140.0	293.0
500	SEGB<90>	-1,764.0	293.0	550	SEGC<107>	-2,964.0	293.0	600	SEGA<123>	-4,164.0	293.0

Table 6. Pad Center Coordinates

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
601	SEGB<124>	-4,188.0	293.0	651	COM<108>	-5,388.0	293.0	0	0	0.0	0.0
602	SEGB<124>	-4,212.0	293.0	652	COM<107>	-5,412.0	293.0	0	0	0.0	0.0
603	SEGA<124>	-4,236.0	293.0	653	COM<106>	-5,436.0	293.0	0	0	0.0	0.0
604	SEGB<125>	-4,260.0	293.0	654	COM<105>	-5,460.0	293.0	0	0	0.0	0.0
605	SEGB<125>	-4,284.0	293.0	655	COM<104>	-5,484.0	293.0	0	0	0.0	0.0
606	SEGA<125>	-4,308.0	293.0	656	COM<103>	-5,508.0	293.0	0	0	0.0	0.0
607	SEGB<126>	-4,332.0	293.0	657	COM<102>	-5,532.0	293.0	0	0	0.0	0.0
608	SEGB<126>	-4,356.0	293.0	658	COM<101>	-5,556.0	293.0	0	0	0.0	0.0
609	SEGA<126>	-4,380.0	293.0	659	COM<100>	-5,580.0	293.0	0	0	0.0	0.0
610	SEGC<127>	-4,404.0	293.0	660	COM<99>	-5,604.0	293.0	0	0	0.0	0.0
611	SEGB<127>	-4,428.0	293.0	661	COM<98>	-5,628.0	293.0	0	0	0.0	0.0
612	SEGA<127>	-4,452.0	293.0	662	COM<97>	-5,652.0	293.0	0	0	0.0	0.0
613	SEGC<128>	-4,476.0	293.0	663	COM<96>	-5,676.0	293.0	0	0	0.0	0.0
614	SEGB<128>	-4,500.0	293.0	664	COM<95>	-5,700.0	293.0	0	0	0.0	0.0
615	SEGA<128>	-4,524.0	293.0	665	COM<94>	-5,724.0	293.0	0	0	0.0	0.0
616	SEGC<129>	-4,548.0	293.0	666	COM<93>	-5,748.0	293.0	0	0	0.0	0.0
617	SEGB<129>	-4,572.0	293.0	667	COM<92>	-5,772.0	293.0	0	0	0.0	0.0
618	SEGA<129>	-4,596.0	293.0	668	COM<91>	-5,796.0	293.0	0	0	0.0	0.0
619	SEGC<130>	-4,620.0	293.0	669	COM<90>	-5,820.0	293.0	0	0	0.0	0.0
620	SEGB<130>	-4,644.0	293.0	670	COM<89>	-5,844.0	293.0	0	0	0.0	0.0
621	SEGA<130>	-4,668.0	293.0	671	COM<88>	-5,868.0	293.0	0	0	0.0	0.0
622	SEGC<131>	-4,692.0	293.0	672	COM<87>	-5,892.0	293.0	0	0	0.0	0.0
623	SEGB<131>	-4,716.0	293.0	673	COM<86>	-5,916.0	293.0	0	0	0.0	0.0
624	SEGA<131>	-4,740.0	293.0	674	COM<85>	-5,940.0	293.0	0	0	0.0	0.0
625	DUMMY<13>	-4,764.0	293.0	675	COM<84>	-5,964.0	293.0	0	0	0.0	0.0
626	DUMMY<14>	-4,788.0	293.0	676	COM<83>	-5,988.0	293.0	0	0	0.0	0.0
627	DUMMY<15>	-4,812.0	293.0	677	COM<82>	-6,012.0	293.0	0	0	0.0	0.0
628	COM<131>	-4,836.0	293.0	678	COM<81>	-6,036.0	293.0	0	0	0.0	0.0
629	COM<130>	-4,860.0	293.0	679	DUMMY<16>	-6,060.0	293.0	0	0	0.0	0.0
630	COM<129>	-4,884.0	293.0	680	DUMMY<17>	-6,034.5	150.0	0	0	0.0	0.0
631	COM<128>	-4,908.0	293.0	681	COM<80>	-6,034.5	120.0	0	0	0.0	0.0
632	COM<127>	-4,932.0	293.0	682	COM<79>	-6,034.5	90.0	0	0	0.0	0.0
633	COM<126>	-4,956.0	293.0	683	COM<78>	-6,034.5	60.0	0	0	0.0	0.0
634	COM<125>	-4,980.0	293.0	684	COM<77>	-6,034.5	30.0	0	0	0.0	0.0
635	COM<124>	-5,004.0	293.0	685	COM<76>	-6,034.5	0.0	0	0	0.0	0.0
636	COM<123>	-5,028.0	293.0	686	COM<75>	-6,034.5	-30.0	0	0	0.0	0.0
637	COM<122>	-5,052.0	293.0	687	COM<74>	-6,034.5	-60.0	0	0	0.0	0.0
638	COM<121>	-5,076.0	293.0	688	COM<73>	-6,034.5	-90.0	0	0	0.0	0.0
639	COM<120>	-5,100.0	293.0	689	COM<72>	-6,034.5	-120.0	0	0	0.0	0.0
640	COM<119>	-5,124.0	293.0	690	COM<71>	-6,034.5	-150.0	0	0	0.0	0.0
641	COM<118>	-5,148.0	293.0	691	COM<70>	-6,034.5	-180.0	0	0	0.0	0.0
642	COM<117>	-5,172.0	293.0	692	COM<69>	-6,034.5	-210.0	0	0	0.0	0.0
643	COM<116>	-5,196.0	293.0	693	COM<68>	-6,034.5	-240.0	0	0	0.0	0.0
644	COM<115>	-5,220.0	293.0	694	COM<67>	-6,034.5	-270.0	0	0	0.0	0.0
645	COM<114>	-5,244.0	293.0	695	COM<66>	-6,034.5	-300.0	0	0	0.0	0.0
646	COM<113>	-5,268.0	293.0	696	DUMMY<18>	-6,034.5	-330.0	0	0	0.0	0.0
647	COM<112>	-5,292.0	293.0	0	0	0.0	0.0	0	0	0.0	0.0
648	COM<111>	-5,316.0	293.0	0	0	0.0	0.0	0	0	0.0	0.0
649	COM<110>	-5,340.0	293.0	0	0	0.0	0.0	0	0	0.0	0.0
650	COM<109>	-5,364.0	293.0	0	0	0.0	0.0	0	0	0.0	0.0

7. PIN DESCRIPTION

Table 7. Power Supply Pins

Name	I/O	Description
VDD3	Supply	I/O power supply.
VIN1R	Supply	Internal regulator power supply This pin is connected to VIN1.
VDD	Supply	Regulated power supply input pin for internal digital and DDRAM block. This pin is connected to REG_OUT outside the chip with stabilization capacitor.
VDDO	Supply	Oscillator Power Supply. Connect to VDD
VSS, VSSO VSSA, VSSB	GND	Ground
VSS3	GND	I/O Ground (This pin is connected to VSS inside the chip and is the assistance pin for adjacent pins.)
V1IN	I	LCD segment high selected driving voltage input pin
V1OUT	O	LCD segment high selected driving voltage output pin
VMIN	I	LCD common non-selected driving voltage input pin
VMOUT	O	LCD common non-selected driving voltage output pin
V0IN	I	LCD segment low selected driving voltage input pin
VCC	I	LCD common high selected driving voltage input pin
VRP	O	LCD common high selected driving voltage output pin
VEE	I	LCD common low selected driving voltage input pin The relationship between VCC, V1, VM, V0 and VEE: $VCC > V1 > VM > V0(=VSS) > VEE$ ($V1 - VM = VM - V0$, $VCC - VM = VM - VEE$)
VRN	O	LCD common low selected driving voltage output pin
VIN1, VIN1A	I	Power supply for 1'st booster circuit and VM amp
VOUT45	O	1'st booster output pin
VIN45	I	Power supply for V1 amp. Recommend to connect this pin to VOUT45
V1T	I	V1 voltage adjustment pin. It is valid only when the external temperature compensation circuit is used. Otherwise, the ITO pattern is recommended not to be made for this pin. Note : V1T is recommended to connect the external Cap. with GND if much noise is injected into this pin.

Table 8. MPU Interface Pins

Name	I/O	Description				
RSTB	I	Reset input pin. When RSTB is "L", initialization is executed.				
PS MPU	I	MPU interface select pin				
		PS	MPU	Description		
		H	L	8080-parallel interface		
		H	H	6800-parallel interface		
		L	L	3 pin SPI (Write only)		
		L	H	4 pin SPI (Write only)		
NOTE: In serial mode, WRB and RDB must be fixed to either VDD3 or VSS3.						
CS1B CS2	I	Chip select input pin. Data / instruction I/O is enabled only when CS1B is "L" and CS2 is "H". When chip select is non-active, DB0 to DB15 are high impedance.				
RS	I	Display Data / Instruction select input pin – RS = "H": DB0 to DB15 are display data – RS = "L": DB0 to DB7 are instruction data * When this pin is not used according to mode, these pins must be tied to VSS3. (In the case of 3Pin Serial I/F mode)				
WRB (R/W)	I	Read / Write execution control pin				
		PS	MPU	MPU Type	WRB	Description
		H	H	6800-series	R/W	Read / Write control input pin – R/W = "H": read – R/W = "L": write
H	L	8080-series	WRB	Write enable clock input pin The data on DB0 to DB15 are latched at the rising edge of the WRB signal.		
RDB (E)	I	Read / Write execution control pin				
		PS	MPU	MPU Type	RDB	Description
		H	H	6800-series	E	Read / Write control input pin – R/W = "H": When E is "H", DB0 to DB15 are in an output status. – R/W = "L": The data on DB0 to DB15 are latched at the falling edge of the E signal.
H	L	8080-series	RDB	Read enable clock input pin When RDB is "L", DB0 to DB15 are in an output status.		
DB[15:8] DB[7]/SDI DB[6]/SCL DB[5:0]	I/O	–DB[15:0]: 16-bit bi-directional data bus. –SDI: Serial data input pin. The data is latched at the rising edge of SCL. –SCL: Serial clock input pin. * When these pins are not used according to mode, these pins must be connected to VSS3.				

Table 9. Oscillator and Power Regulator Pins

Name	I/O	Description
EXCLK	I	External clock input pin When an external input is used, it is input to this pin. But the internal oscillator is used, this pin is connected to VDD3 or VSS3.
REG_OUT	O	Internal voltage regulator output pin This pin is connected to VDD, VDDO, VDDM outside the chip with stabilization capacitor.

Table 10. Timing signal Pins for monitoring

Name	I/O	Description
CL	O	Shift clock output pin
PM	O	Field delimiter output pin
FR	O	Liquid crystal alternating current output pin

Table 11. LCD driver output pins

Name	I/O	Description
SEGA0 to 131	O	LCD driving segment outputs (Red or Blue)
SEGB0 to 131	O	LCD driving segment outputs (Green)
SEGC0 to 131	O	LCD driving segment outputs (Blue or Red)
COM0 to 131	O	LCD common outputs

Table 12. MTP pins

Name	I/O	Description
P_MTP	I	Power of writing MTP cell (When this pin is not used, this pin must be floating)

Table 13. Test pins

Name	I/O	Description
TEST[2:0]	I	Don't use these pins. IC maker's test pins These pins must be tied to VDD3.
FUSE_EN	I	Don't use this pin. IC maker's test pin This pin must be tied to VDD3.
MODE[1:0]	I	Don't use these pins. IC maker's test pins These pins must be tied to VDD3.
ZIGZAG_MODE	I	COM group scan mode select pin. – ZIGZAG_MODE = H : COM group scanning operates in zigzag. In this mode, ZIGZAG_MODE pin is tied to VDD3. – ZIGZAG_MODE = L : COM group scanning operates in sequence. In this mode, ZIGZAG_MODE pin is tied to VSS3.
RTEST	I	Don't use this pin. IC maker's test pin This pin must be tied to VSS3.
C21P	O	Don't use this pin. IC maker's test pin This pin must be floating.
C31M	O	Don't use this pin. IC maker's test pin This pin must be floating.
DUMMY	–	This pin must be floating.

8. FUNCTIONAL DESCRIPTION

8.1. MPU Interface

8.1.1. Chip Select Input

There are CS1B and CS2 pins for chip selection. The S6B3301 can interface with an MPU only when CS1B is “L” and CS2 is “H”. When these pins are set to any other combination, RS, RDB, and WRB inputs are disabled and DB0 to DB15 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

8.1.2. Parallel/Serial Interface

The S6B3301 has four types of interface with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in Table 8.

Table 14. Parallel/Serial Interface–Mode.

PS	MPU	CS1B	CS2	MPU bus type
H	L	CS1B	CS2	8080–Series MPU
	H			6800–Series MPU
L	L	CS1B	CS2	3–Pin SPI
	H			4–Pin SPI

8.1.3. Parallel Interface (PS=“H”)

The 8–bit/16–bit bi–directional data bus is used in parallel interface. The type of MPU is selected by MPU and the mode of data–bus is controlled by 16B register as shown in below. In accessing internal registers (RS = “L”), only DB[7:0] are valid. When 16B is high, DB[15:8] are high impedance.

Table 15. MPU Selection for Parallel Interface

MPU	16B	CS1B	CS2	RDB	WRB	Data Bus	MPU bus type
L	L	CS1B	CS2	RDB	WRB	DB[15:0]	8080–series MPU
	H					DB[7:0]	
H	L	CS1B	CS2	E	R/W	DB[15:0]	6800–series MPU
	H					DB[7:0]	

Table 16. Parallel Data Transfer

RS	6800-series		8080-series		Description
	E	R/W	RDB	WRB	
H	H	H	L	H	Read display data
H	H	L	H	L	Write display data
L	H	H	L	H	Read out internal status register
L	H	L	H	L	Write instruction data

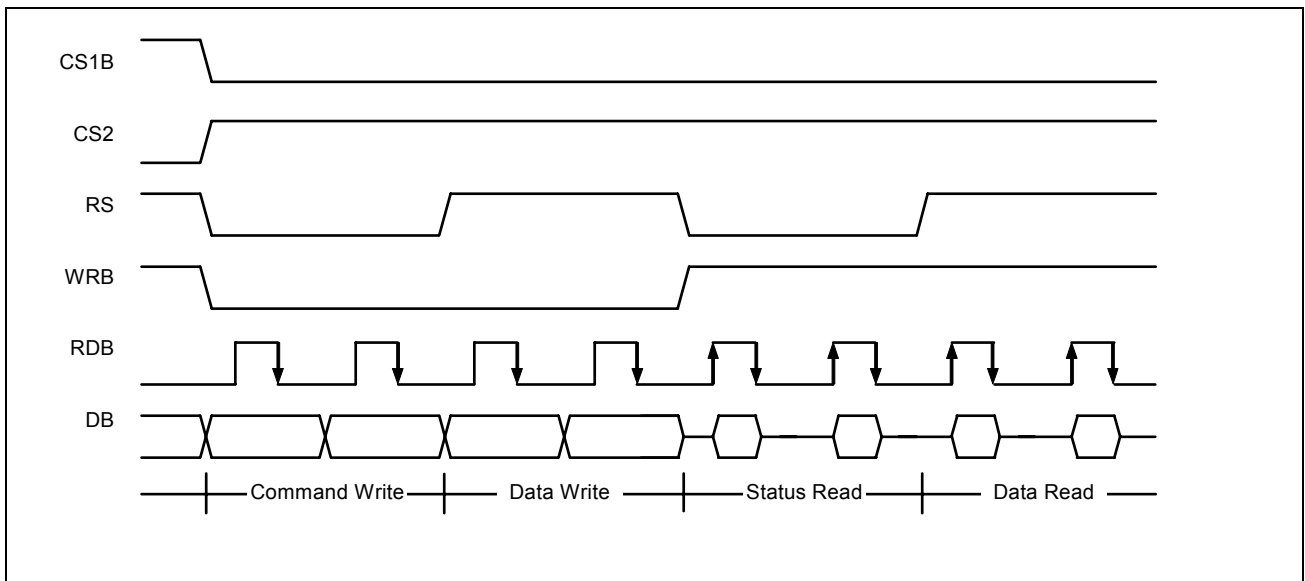


Figure 5. 6800-Series MPU Interface protocol (MPU="H")

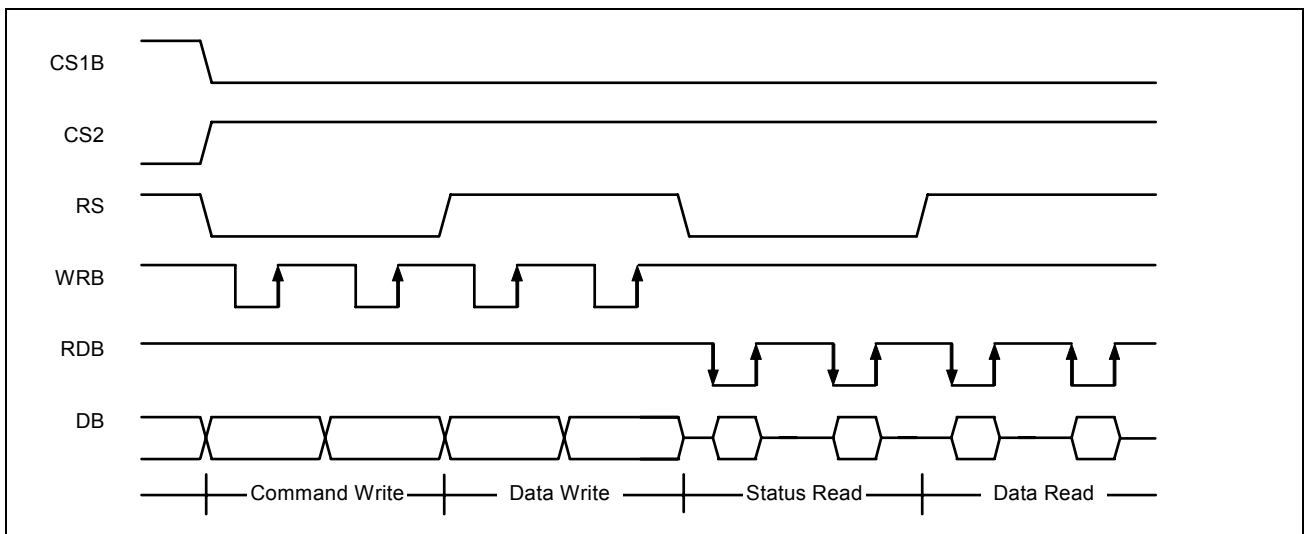


Figure 6. 8080-Series MPU Interface Protocol (MPU="L")

8.1.4. Serial Interface (PS="L")

Communication with the MPU occurs via a clock-synchronized serial peripheral interface when PS is low. When using the serial interface, read operations are not allowed. When the chip select inputs are valid (CS1B = "L" & CS2 = "H"), the serial data is sent most significant bit first on the rising edge of a serial clock going into DB6 and processed as 8 bit parallel data on the eighth clock. Since the clock signal is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended. And Invalid, the internal shift register and the counter are reset. The serial interface type is selected by setting PS as shown in Table14.

Table 17. MPU Selection for Serial Interface

PS	MPU	CS1B	CS2	RS	Serial Data	Serial Clock	SPI Mode
L	L	CS1B	CS2	By S/W	DB[7]	DB[6]	3-Pin
	H	CS1B	CS2	D/I			4-Pin

8.1.5. 3-Pin SPI Interface (PS = "L" & MPU = "L")

In 3-Pin SPI Interface mode, the first bit of serial 9 bits is used to indicate whether serial data input is display or instruction data instead of D/I pin. The serial data format consists of D/I (1bit) and DATA (8bits). For details, refer the Figure 7.

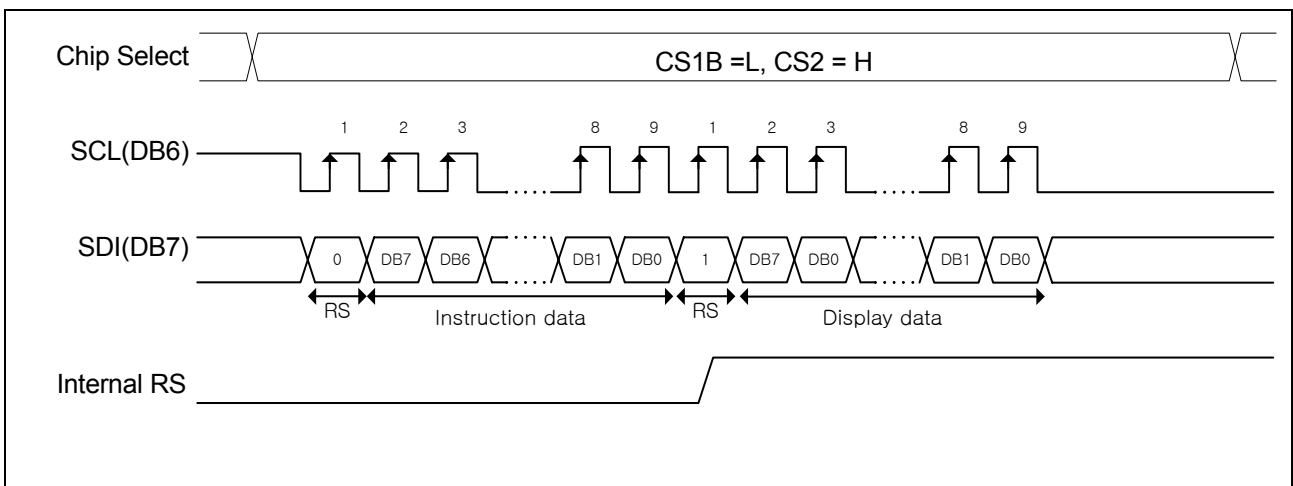


Figure 7. 3-Pin SPI Timing (RS is not used)

8.1.6. 4-Pin Serial Interface (PS="L" & MPU="H")

In 4-pin SPI interface mode, RS pin is used for indicating whether serial data input is display or instruction data. Data is display data when RS is high and instruction data when RS is low. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. For details, refer the Figure 8.

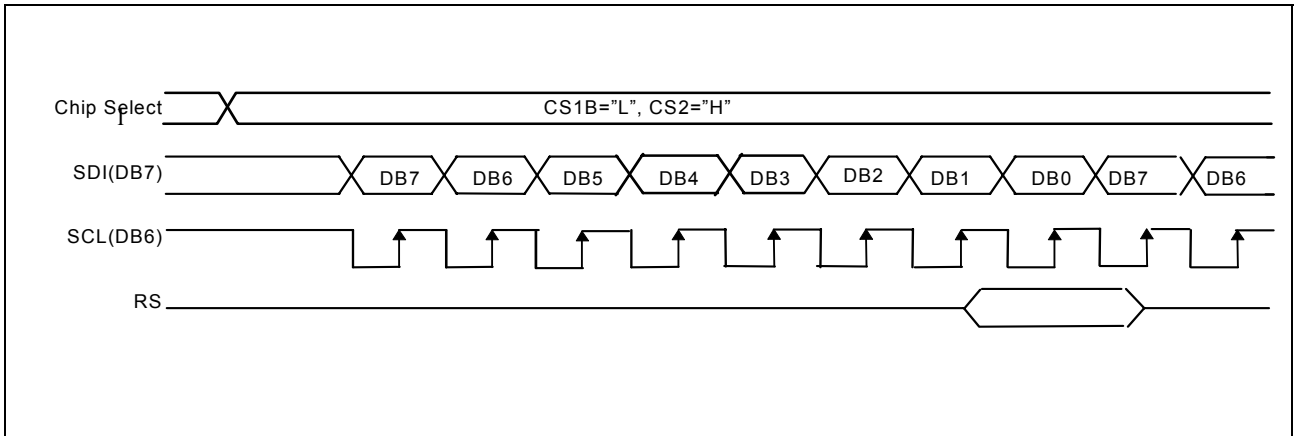


Figure 8. 4-Pin Serial Interface Timing

8.2. DISPLAY DATA RAM

The on-chip display data RAM of S6B3301 is a static RAM that is stored the data for the display. It is a 2,112 x 132 structure. It is controlled by 2 addresses, X and Y. And, RAM area selection and automatic address count up functions are accomplished by the internal instructions.

8.2.1. DDRAM Address Area Selection

A part of DDRAM address area of S6B3301 can be accessed by X and Y address area settings. After setting RAM area, the addresses become the start address.

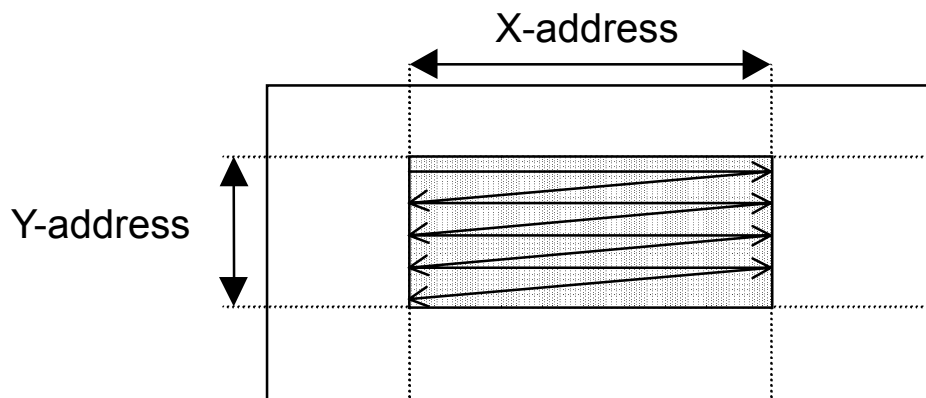


Figure 9. DDRAM Address Area

Table 18. Y address Control

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	0	0	0	1	0
P1	Y start address set(Initial Status = 00H)							
P2	Y end address set(Initial Status = 83H)							

Table 19. X address Control

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	0	0	0	1	1
P1	X start address set (Initial status = 00H)							
P2	X end address set (Initial status = 83H)							

8.2.2. RAM Addressing Count up

By selecting the X address and Y address area by the internal instructions, the address counts up from its start address to end address after data access operation. When one address is equal to the end address, it returns to the start address. At this time, the other address is increased by 1.

8.2.3. X address count mode (X address = 00h to 83h, Y address = 00h to 83h)

		X-address									
		00h	01h	02h	03h	04h	05h	06h	07h	08h	83h
Y-address	00h	1	2	3	4	5	6	7	8	9	132
	01h	133									264
	02h	265									396
	03h	397									528
	83h	17293									

Figure 10. X address count mode

8.2.4. Y address count mode (X address =00h to 83h, Y address = 00h to 83h)

		X-address									
		00h	01h	02h	03h	04h	05h	06h	07h	08h	83h
Y-address	00h	1	133	265	397	529	661	793	925	1057	17293
	01h	2									
	02h	3									
	03h	4									
	83h	132	264	396	528	660	792	924	1056	1188	17424

Figure 11. Y address count mode

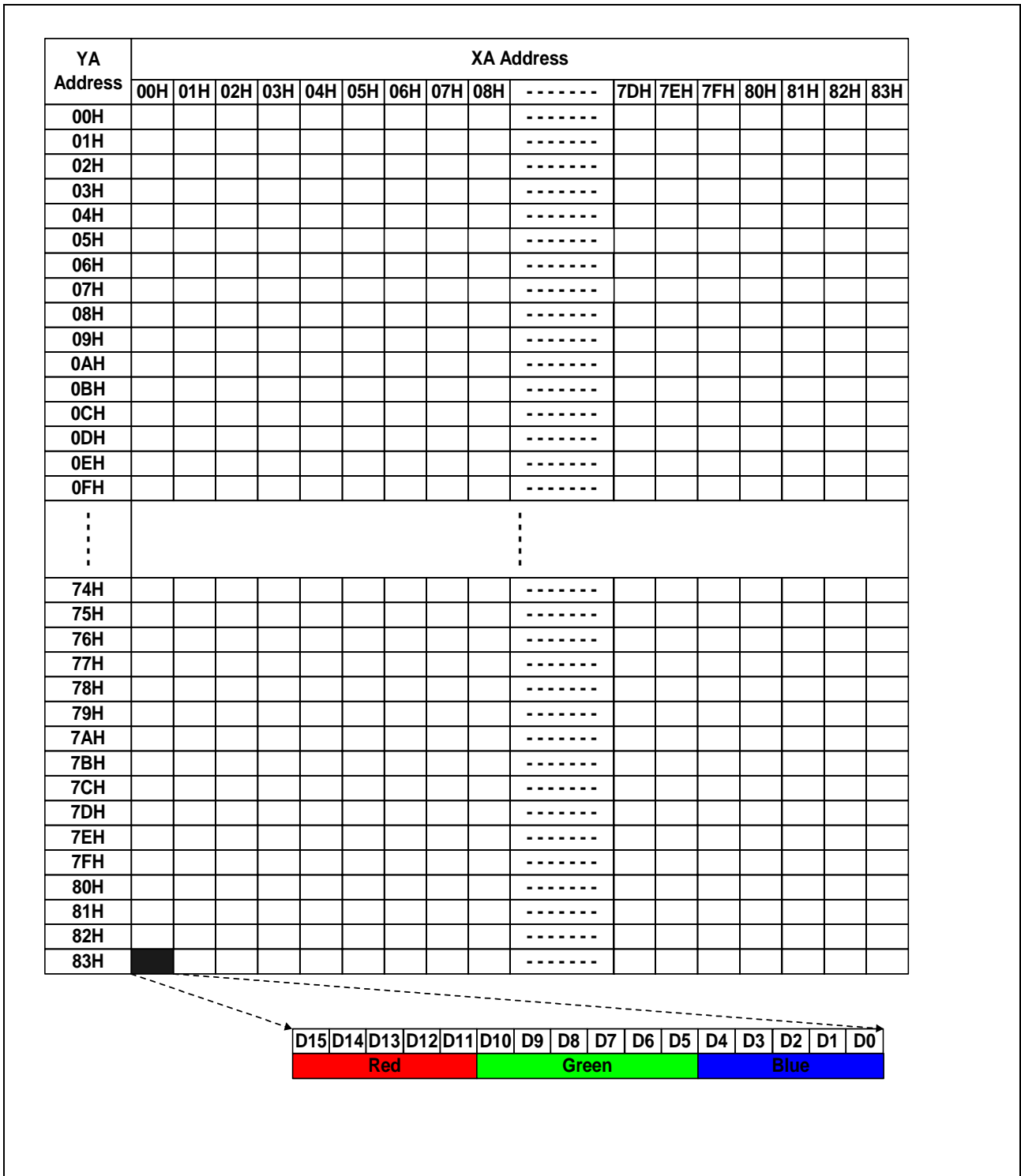


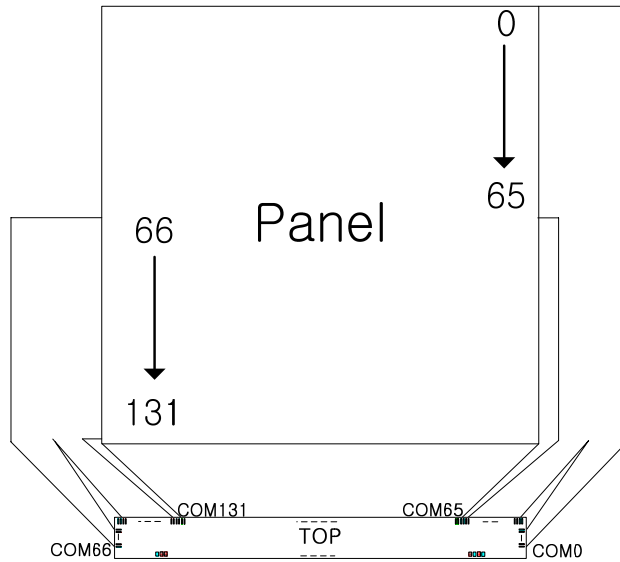
Figure 12. Display Data RAM Map

8.2.5. COM Group Scan Mode

There is ZIGZAG_MODE pin for COM group scan mode selection.

ZIGZAG_MODE=0

COM group scanning operates in sequence.



ZIGZAG_MODE=1

COM group scanning operates in zigzag.

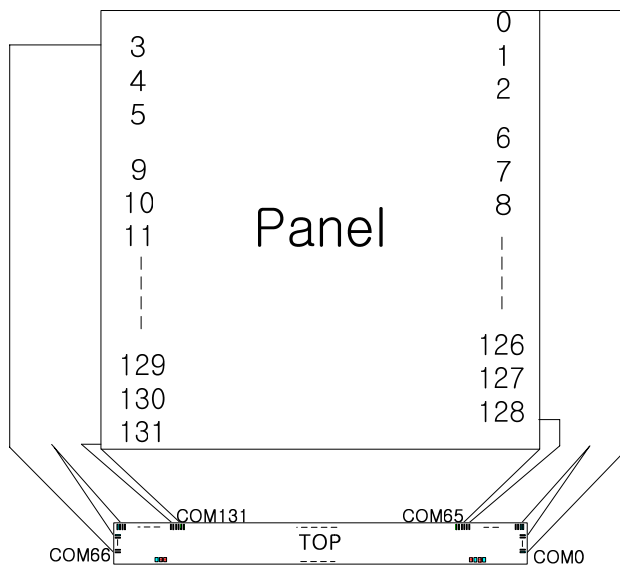


Figure 13. The relationship between COM outputs and Panel

8.2.6. The relationship between COM outputs and display line of panel (CDIR=0)

Display Line Number	Common Number ZIGZAG_ MODE=0	Common Number ZIGZAG_ MODE=1	Display Line Number	Common Number ZIGZAG_ MODE=0	Common Number ZIGZAG_ MODE=1	Display Line Number	Common Number ZIGZAG_ MODE=0	Common Number ZIGZAG_ MODE=1
Line Number0	COM0	COM0	Line Number45	COM45	COM87	Line Number90	COM90	COM45
Line Number1	COM1	COM1	Line Number46	COM46	COM88	Line Number91	COM91	COM46
Line Number2	COM2	COM2	Line Number47	COM47	COM89	Line Number92	COM92	COM47
Line Number3	COM3	COM66	Line Number48	COM48	COM24	Line Number93	COM93	COM111
Line Number4	COM4	COM67	Line Number49	COM49	COM25	Line Number94	COM94	COM112
Line Number5	COM5	COM68	Line Number50	COM50	COM26	Line Number95	COM95	COM113
Line Number6	COM6	COM3	Line Number51	COM51	COM90	Line Number96	COM96	COM48
Line Number7	COM7	COM4	Line Number52	COM52	COM91	Line Number97	COM97	COM49
Line Number8	COM8	COM5	Line Number53	COM53	COM92	Line Number98	COM98	COM50
Line Number9	COM9	COM69	Line Number54	COM54	COM27	Line Number99	COM99	COM114
Line Number10	COM10	COM70	Line Number55	COM55	COM28	Line Number100	COM100	COM115
Line Number11	COM11	COM71	Line Number56	COM56	COM29	Line Number101	COM101	COM116
Line Number12	COM12	COM6	Line Number57	COM57	COM93	Line Number102	COM102	COM51
Line Number13	COM13	COM7	Line Number58	COM58	COM94	Line Number103	COM103	COM52
Line Number14	COM14	COM8	Line Number59	COM59	COM95	Line Number104	COM104	COM53
Line Number15	COM15	COM72	Line Number60	COM60	COM30	Line Number105	COM105	COM117
Line Number16	COM16	COM73	Line Number61	COM61	COM31	Line Number106	COM106	COM118
Line Number17	COM17	COM74	Line Number62	COM62	COM32	Line Number107	COM107	COM119
Line Number18	COM18	COM9	Line Number63	COM63	COM96	Line Number108	COM108	COM54
Line Number19	COM19	COM10	Line Number64	COM64	COM97	Line Number109	COM109	COM55
Line Number20	COM20	COM11	Line Number65	COM65	COM98	Line Number110	COM110	COM56
Line Number21	COM21	COM75	Line Number66	COM66	COM33	Line Number111	COM111	COM120
Line Number22	COM22	COM76	Line Number67	COM67	COM34	Line Number112	COM112	COM121
Line Number23	COM23	COM77	Line Number68	COM68	COM35	Line Number113	COM113	COM122
Line Number24	COM24	COM12	Line Number69	COM69	COM99	Line Number114	COM114	COM57
Line Number25	COM25	COM13	Line Number70	COM70	COM100	Line Number115	COM115	COM58
Line Number26	COM26	COM14	Line Number71	COM71	COM101	Line Number116	COM116	COM59
Line Number27	COM27	COM78	Line Number72	COM72	COM36	Line Number117	COM117	COM123
Line Number28	COM28	COM79	Line Number73	COM73	COM37	Line Number118	COM118	COM124
Line Number29	COM29	COM80	Line Number74	COM74	COM38	Line Number119	COM119	COM125
Line Number30	COM30	COM15	Line Number75	COM75	COM102	Line Number120	COM120	COM60
Line Number31	COM31	COM16	Line Number76	COM76	COM103	Line Number121	COM121	COM61
Line Number32	COM32	COM17	Line Number77	COM77	COM104	Line Number122	COM122	COM62
Line Number33	COM33	COM81	Line Number78	COM78	COM39	Line Number123	COM123	COM126
Line Number34	COM34	COM82	Line Number79	COM79	COM40	Line Number124	COM124	COM127
Line Number35	COM35	COM83	Line Number80	COM80	COM41	Line Number125	COM125	COM128
Line Number36	COM36	COM18	Line Number81	COM81	COM105	Line Number126	COM126	COM63
Line Number37	COM37	COM19	Line Number82	COM82	COM106	Line Number127	COM127	COM64
Line Number38	COM38	COM20	Line Number83	COM83	COM107	Line Number128	COM128	COM65
Line Number39	COM39	COM84	Line Number84	COM84	COM42	Line Number129	COM129	COM129
Line Number40	COM40	COM85	Line Number85	COM85	COM43	Line Number130	COM130	COM130
Line Number41	COM41	COM86	Line Number86	COM86	COM44	Line Number131	COM131	COM131
Line Number42	COM42	COM21	Line Number87	COM87	COM108			
Line Number43	COM43	COM22	Line Number88	COM88	COM109			
Line Number44	COM44	COM23	Line Number89	COM89	COM110			

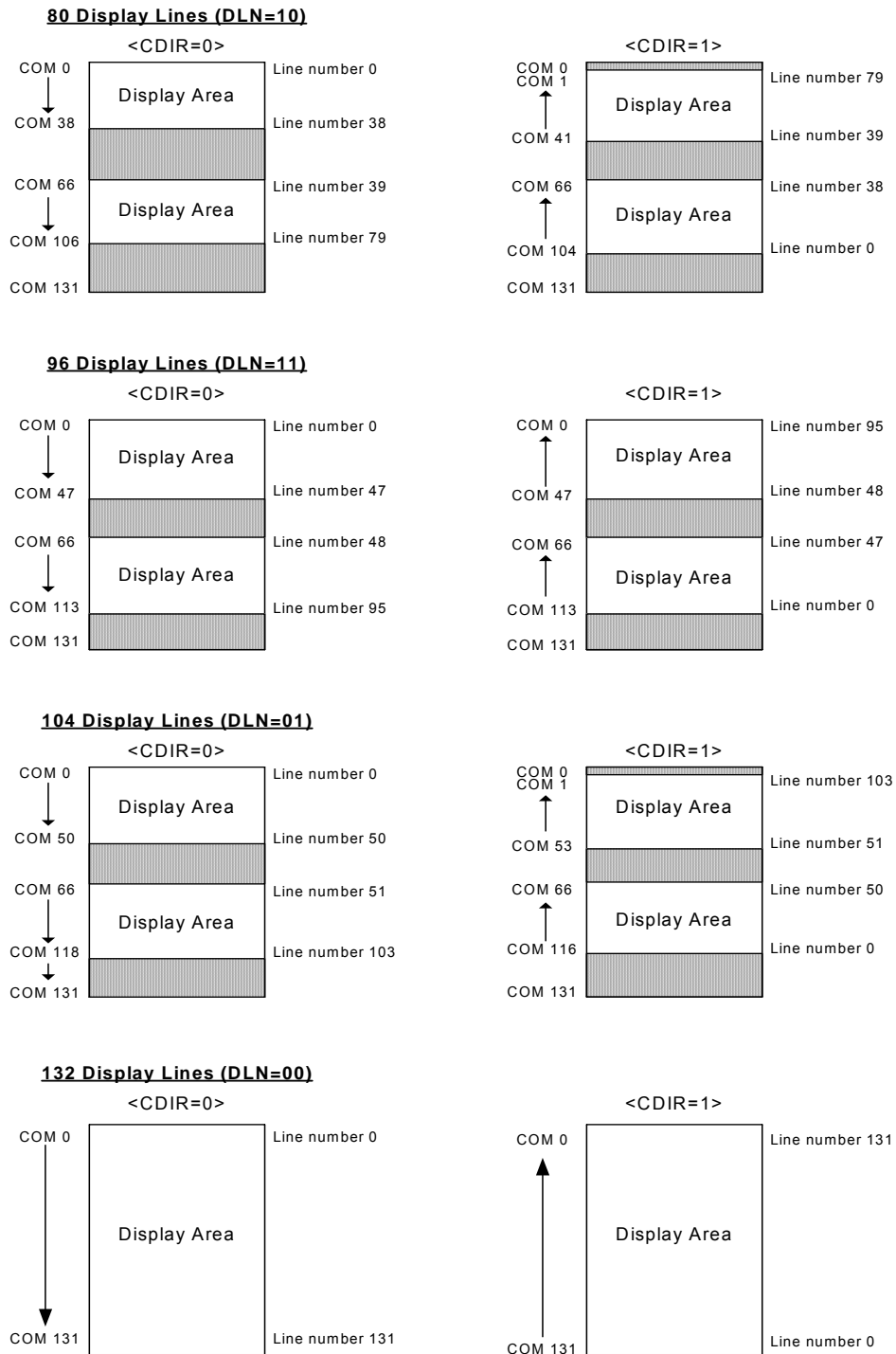
8.3. Display Direction

8.3.1. CDIR

The CDIR flag of Driver Output Mode Set Instruction selects the direction of common driver scanning.

(ZIGZAG_MODE=0)

COM group scanning operates in sequence.

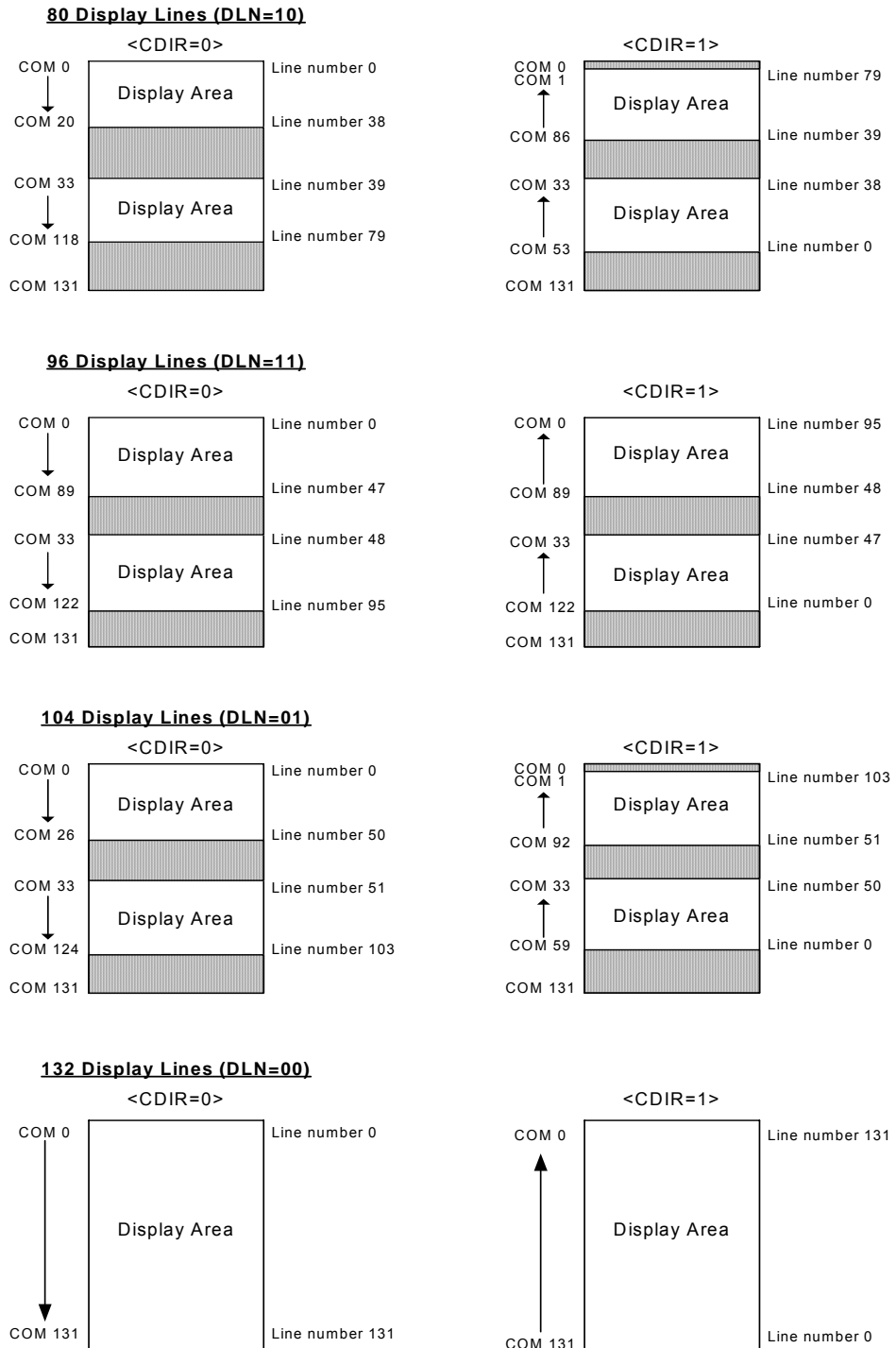


8.3.2. CDIR

The CDIR flag of Driver Output Mode Set Instruction selects the direction of common driver scanning.

(ZIGZAG_MODE=1)

COM group scanning operates in zigzag



8.3.3. SWP

The SWP flag of Driver Output Mode Set instruction selects the swapping of segment display.

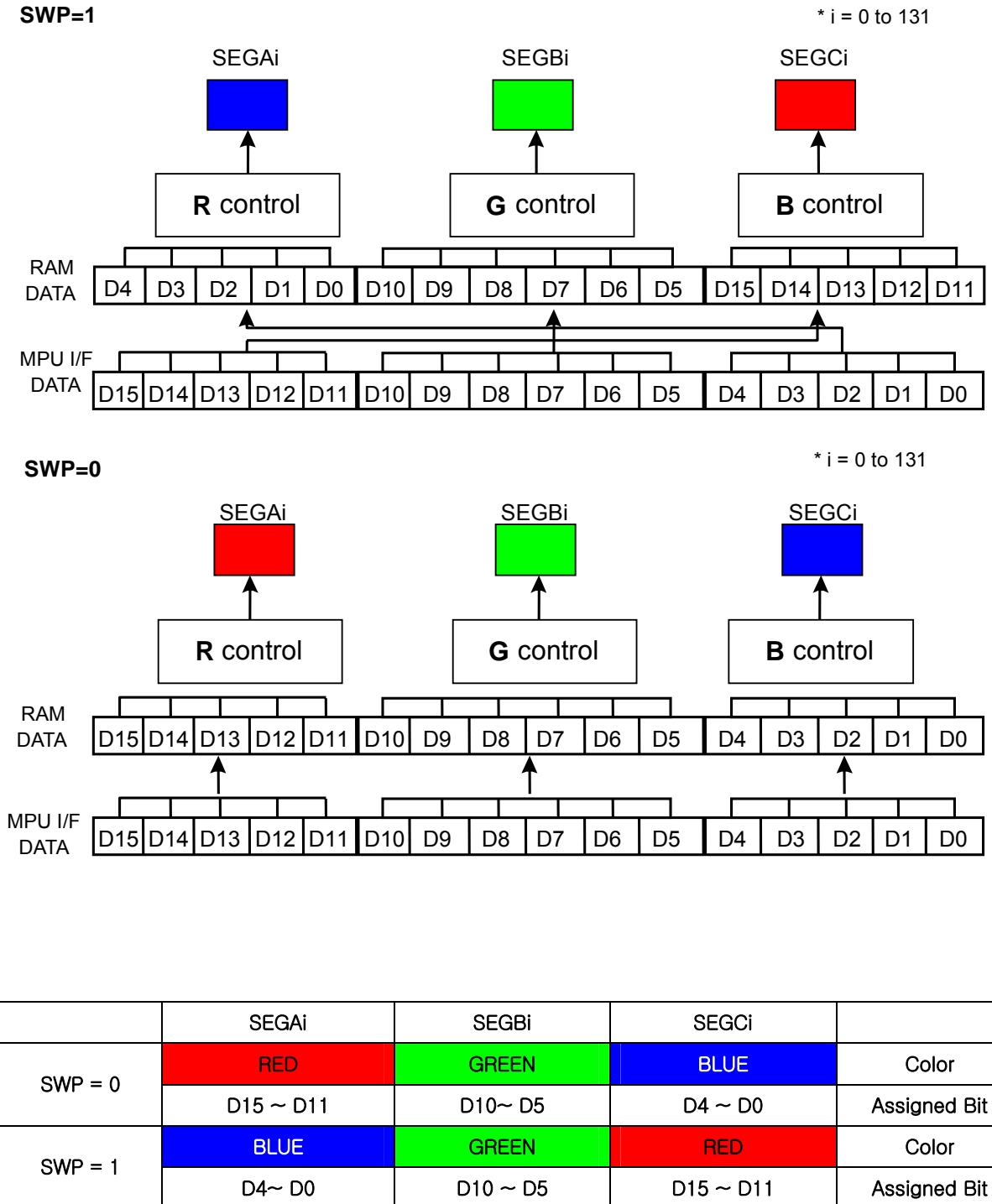


Figure 14. The relationship between SEG outputs and RGB color

9. INSTRUCTION DESCRIPTION

Table 20. Instruction Table

Instruction Name	RS	WRB	RDB	DB15 ~ DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.	Parameter
Non Operation	0	0	1	*	0	0	0	0	0	0	0	0	00	
Oscillation Mode Set	0	0	1	*	0	0	0	0	0	0	1	0	02	1Byte
Driver Output Mode Set	0	0	1	*	0	0	0	1	0	0	0	0	10	1Byte
Monitor Signal Control	0	0	1	*	0	0	0	1	1	0	0	0	18	1Byte
Temperature Compensation Set	0	0	1	*	0	0	1	0	1	0	0	0	28	1Byte
Contrast Control	0	0	1	*	0	0	1	0	1	0	1	0	2A	1Byte
Standby Mode OFF	0	0	1	*	0	0	1	0	1	1	0	0	2C	-
Standby Mode ON	0	0	1	*	0	0	1	0	1	1	0	1	2D	-
Addressing Mode Set	0	0	1	*	0	0	1	1	0	0	0	0	30	1Byte
ROW Vector Mode Set	0	0	1	*	0	0	1	1	0	0	1	0	32	1Byte
N-block Inversion Set	0	0	1	*	0	0	1	1	0	1	0	0	34	1Byte
Driving Mode Set	0	0	1	*	0	0	1	1	0	1	1	0	36	1Byte
Entry Mode Set	0	0	1	*	0	1	0	0	0	0	0	0	40	1Byte
Row address Area Set	0	0	1	*	0	1	0	0	0	0	1	0	42	2Byte
Column address Area Set	0	0	1	*	0	1	0	0	0	0	1	1	43	2Byte
RAM skip Area Set	0	0	1	*	0	1	0	0	0	1	0	1	45	1Byte
Display OFF	0	0	1	*	0	1	0	1	0	0	0	0	50	-
Display ON	0	0	1	*	0	1	0	1	0	0	0	1	51	-
Specified Display Pattern Set	0	0	1	*	0	1	0	1	0	0	1	1	53	1Byte
Partial Display Mode Set	0	0	1	*	0	1	0	1	0	1	0	1	55	1Byte
Partial Display Start Line Set	0	0	1	*	0	1	0	1	0	1	1	0	56	1Byte
Partial Display End Line Set	0	0	1	*	0	1	0	1	0	1	1	1	57	1Byte
Booster Boosting Ratio Set	0	0	1	*	0	1	1	1	0	0	0	0	70	1Byte
Frame Frequency Set	0	0	1	*	0	1	1	1	1	1	1	1	7F	1Byte
Preliminary Instruction	0	0	1	*	1	0	0	0	1	1	0	0	8C	1Byte
MTP Load	0	0	1	*	1	1	1	0	0	1	0	1	E5	-
MTP Read Mode	0	0	1	*	1	1	1	0	0	1	1	0	E6	1Byte
MTP Initial Disable	0	0	1	*	1	1	1	0	1	0	0	0	E8	-
MTP Initial Enable	0	0	1	*	1	1	1	0	1	0	0	1	E9	-
MTP Select Mode Off	0	0	1	*	1	1	1	0	1	0	1	0	EA	-
MTP Select Mode On	0	0	1	*	1	1	1	0	1	0	1	1	EB	-
Offset Volume Set	0	0	1	*	1	1	1	0	1	1	0	1	ED	1Byte
MTP Write Disable	0	0	1	*	1	1	1	0	1	1	1	0	EE	-
MTP Write Enable	0	0	1	*	1	1	1	0	1	1	1	1	EF	-
Display Data Write	1	0	1		Display Data Write							-	-	
Display Data Read	1	1	0		Display Data Read							-	-	
Status Read	0	1	0	0	Status Data Read							-	-	

*: Don't care

Parameter: The number of parameter bytes that follows instruction data.

9.1. Non Operation (00H)

This instruction is Non operation.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	0	0

9.2. Oscillation Mode Set (02H)

Setting internal function mode.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1	0
			0	0	0	0	0	0	0	EXT

EXT: External clock selecting

EXT = 0: Internal clock mode (Initial status)

EXT = 1: External clock mode

9.3. Driver Output Mode Set (10H)

This instruction sets the display duty and direction.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	0	0	0	0
			0	0	DLN		MY	MX	SWP	CDIR

DLN: Display Line Number selecting (DLN = 00 initial status)

DB5	DB4	Display Duty
0	0	1/132
0	1	1/104
1	0	1/80
1	1	1/96

MY: Selection Row Address Count.

MY = 0 : Row address increment (Initial status)

MY = 1 : Row address decrement

MX: Selection Column Address Count.

MX = 0 : Column address increment (Initial status)

MX = 1 : Column address decrement

SWP: Swap segment output SEGAI and SEGCi

This bit is for swapping the output of segment driver.

SWP = 0 (Initial status)

CDIR: Common Direction

This bit is for controlling the direction of common driver.

CDIR = 0 (Initial status)

9.4. Monitor Signal Control (18H)

This instruction configures the output enable and timing of monitor signal

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	1	0	0	0
			0	0	0	0	0	PM	CL	FR

PM: Enable to transfer field delimiter signal to output pin by active high
 PM = 0 (Initial status)

CL: Enable to transfer shift signal to output pin by active high
 CL = 0 (Initial status)

FR: Enable to transfer liquid crystal alternating signal to output pin by active high
 FR = 0 (Initial status)

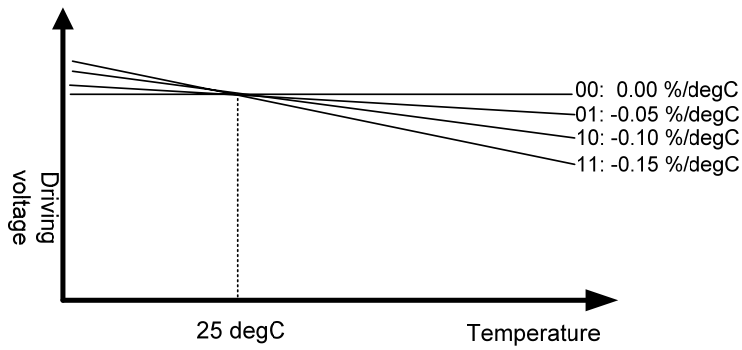
9.5. Temperature Compensation Set (28H)

This Instruction sets up the driving voltage slope for temperature compensation.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	0	0	0
			0	0	0	0	0	0	TCS	

TCS: Temperature compensation slope set (TCS = 00 initial status)

TCS[1:0]	Temp. Coefficient	Note
00	0.00%/°C	(Initial status)
01	-0.05%/°C	
10	-0.10%/°C	
11	-0.15%/°C	



9.6. Contrast Control (2AH)

This instruction updates the contrast control value in normal display mode and partial display mode.

RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	0	1	0
Contrast control value (0 to 127)										

The relation between V1 voltage (typ.) and Contrast set value (00h initial status)

Contrast(HEX)	V1 [V]	Contrast(HEX)	V1 [V]	Contrast(HEX)	V1 [V]	Contrast(HEX)	V1 [V]
00h	2.800	20h	3.102	40h	3.405	60h	3.707
01h	2.809	21h	3.112	41h	3.414	61h	3.717
02h	2.819	22h	3.121	42h	3.424	62h	3.726
03h	2.828	23h	3.131	43h	3.433	63h	3.735
04h	2.838	24h	3.140	44h	3.443	64h	3.745
05h	2.847	25h	3.150	45h	3.452	65h	3.754
06h	2.857	26h	3.159	46h	3.461	66h	3.764
07h	2.866	27h	3.169	47h	3.471	67h	3.773
08h	2.876	28h	3.178	48h	3.480	68h	3.783
09h	2.885	29h	3.187	49h	3.490	69h	3.792
0Ah	2.894	2Ah	3.197	4Ah	3.499	6Ah	3.802
0Bh	2.904	2Bh	3.206	4Bh	3.509	6Bh	3.811
0Ch	2.913	2Ch	3.216	4Ch	3.518	6Ch	3.820
0Dh	2.923	2Dh	3.225	4Dh	3.528	6Dh	3.830
0Eh	2.932	2Eh	3.235	4Eh	3.537	6Eh	3.839
0Fh	2.942	2Fh	3.244	4Fh	3.546	6Fh	3.849
10h	2.951	30h	3.254	50h	3.556	70h	3.858
11h	2.961	31h	3.263	51h	3.565	71h	3.868
12h	2.970	32h	3.272	52h	3.575	72h	3.877
13h	2.980	33h	3.282	53h	3.584	73h	3.887
14h	2.989	34h	3.291	54h	3.594	74h	3.896
15h	2.998	35h	3.301	55h	3.603	75h	3.906
16h	3.008	36h	3.310	56h	3.613	76h	3.915
17h	3.017	37h	3.320	57h	3.622	77h	3.924
18h	3.027	38h	3.329	58h	3.631	78h	3.934
19h	3.036	39h	3.339	59h	3.641	79h	3.943
1Ah	3.046	3Ah	3.348	5Ah	3.650	7Ah	3.953
1Bh	3.055	3Bh	3.357	5Bh	3.660	7Bh	3.962
1Ch	3.065	3Ch	3.367	5Ch	3.669	7Ch	3.972
1Dh	3.074	3Dh	3.376	5Dh	3.679	7Dh	3.981
1Eh	3.083	3Eh	3.386	5Eh	3.688	7Eh	3.991
1Fh	3.093	3Fh	3.395	5Fh	3.698	7Fh	4.000

9.7. Standby Mode OFF (2CH)

This instruction releases the standby mode.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	1	0	0

The internal statuses during standby off are as following:

All commons output: VRP or -VR or VM

All segments output: VSS or V1

All Analog power is generated automatically. (OSC. , Amp. , Booster(1'st, 2'nd, 3'rd))

Displaying clocks (FR, PM, CL): In operation

Function and Pin condition at standby OFF

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	ON (Operate)
COM outputs	VRP or VM or VRN
SEG outputs	V1 or VSS

9.8. Standby Mode ON (2DH)

This instruction enters the standby mode to reduce the power consumption to the static power consumption value (Initial status). The following instructions, standby off and display on, cause returning to the normal operation status.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	1	0	1

The internal statuses during standby on are as following:

All common and segment output: VSS

All analog power circuit : OFF (OSC. , Amp. , Booster(1'st,2'nd,3'rd))

Displaying clocks (FR, PM, CL) are held.

Function and Pin condition at standby ON

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	OFF
COM outputs	VSS
SEG outputs	Floating (discharged)

LCD driving power output condition at Standby ON.

level	Condition
VRP	VIN1
V1	VSS
VM	VSS
VRN	VSS

9.9. Addressing Mode Set (30H)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	0	0	0
			0	0	GSM	DSG	SGF	SGP		SGM

GSM: Gray Scale Mode

- 0 : 65,536 color mode(Initial status)
- 1 : 4,096 color mode (refer to "Display data Write/Read")

DSG : Duty Adjust Setting

- 0 : Dummy subgroup is one subgroup (Initial status)
- 1 : Dummy subgroup is none

SGF : Sub Group Frame Inversion mode setting

- 0: SG Frame inversion OFF (Initial status)
- 1: SG Frame inversion ON

SGM : Sub Group inversion mode setting

- 0: SG inversion OFF (Initial status)
- 1: SG inversion ON

SGP : Sub Group Phase mode setting

- 00 : Same phase in all pixels (Initial status)
- 01 : Different phase by 1pixel-unit
- 10 : Different phase by 2pixel-unit
- 11 : Different phase by 4pixel-unit

9.10. Row Vector Mode Set (32H)

Setting ROW function.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	0	1	0
			0	0	0	0	INC		VEC	

INC: Row Vector Increment Mode. This Parameter set up Row vector increment period (INC = 000 initial status)

DB3	DB2	DB1	Row Vector Increment Period
0	0	0	Every subgroup
0	0	1	Every 2subgroup
0	1	0	Every 4subgroup
0	1	1	Every 8subgroup
1	0	0	Every 16subgroup
1	0	1	Every 16subgroup
1	1	0	Every 16subgroup
1	1	1	Every subframe

VEC: ROW Vector Sequence Mode

- 0: R1->R2->R3->R4 -> R1... (initial status)
- 1: R1->R3->R2->R4 -> R1... ..

9.11. N-block inversion Set (34H)

This instruction set up N block inversion for AC driving.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	1	0	0
			FIM	FIP	0	N-block inversion				

FIM: Forcing Inversion Mode

FIM = 0: Forcing Inversion OFF (Initial status)

FIM = 1: Forcing Inversion ON

FIP: Forcing Inversion Period

FIP = 0: Forcing Inversion Period is one frame (Initial status)

FIP = 1: Forcing Inversion Period is two frames

N-block Inversion : This parameter indicates the basic period of polarity inversion.

The whole period of polarity inversion is decided by FIM, FIP and this parameter.

(N-block Inversion = 00h initial status)

DB7	DB6	DB5	DB4 – DB0	Polarity Inversion Period
x	X	x	0	Every frame
0	X	x	1	Every 1 block
:	:	:	:	:
0	X	x	31	Every 31 blocks
1	0	x	1	Every 1 block and every frame
:	:	:	:	:
1	0	x	31	Every 31 blocks and every frame
1	1	x	1	Every 1 block and every 2 frames
:	:	:	:	:
1	1	x	31	Every 31 blocks and every 2 frames

9.12. Driving Mode Set (36H)

This instruction controls the internal driving mode.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	1	1	0
			0	0	0	0	0	0	0	LFS

LFS: Low frame frequency set for low power consumption.

LFS = 0 : Low frequency set OFF (Initial status)

LFS = 1 : Low frequency set ON

Note: $f_{FR} @ (LFS=1) = f_{FR} @ (LFS=0) / 2$

9.13. Entry Mode Set (40H)

Setting internal function mode.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	0	0
			16B	0	0	0	0	MDI	Y/X	RMW

16B: Selection data bus width.

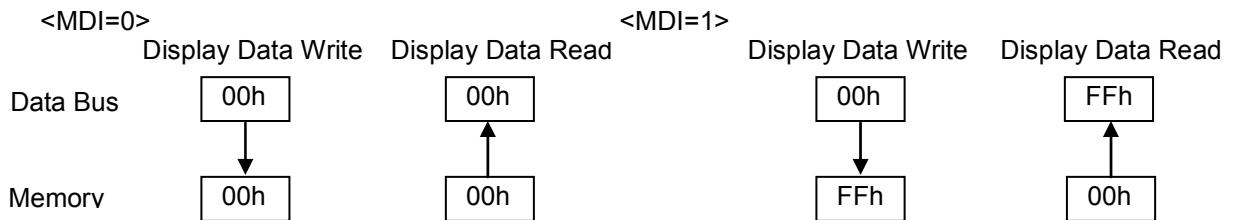
16B = 0 : 16bit data bus (Initial status)

16B = 1 : 8bit data bus

MDI: Memory data inversion setting for low power consumption.

MDI = 0: Memory data inversion OFF (Initial status)

MDI = 1: Memory data inversion ON



Y/X: Selection Address Count.

Y/X = 0 : Column address count first (Initial status)

Y/X = 1 : Row address count first

RMW: Read modify write mode ON/OFF select

RMW = 0 : Read modify write OFF (Initial status)

RMW = 1: Read modify write ON. When this mode is on, X(Y) address of on-chip display RAM is not increment in reading display data but in writing display data.

Table 21. Entry Mode Set Table

Display Data Direction	Entry Mode Set			Stored data into DDRAM	Display Data Direction	Entry Mode Set			Stored data into DDRAM
	Y/X	MX	MY			Y/X	MX	MY	
Normal	0	0	0		X-Y Exchange	1	0	0	
Y-Mirror	0	0	1		X-Y Exchange Y-Mirror	1	0	1	
X-Mirror	0	1	0		X-Y Exchange X-Mirror	1	1	0	
X-Mirror Y-Mirror	0	1	1		X-Y Exchange X-Mirror Y-Mirror	1	1	1	

9.14. Row Address Area Set (42H)

This instruction and parameter set up the Y address areas of the on-chip display data RAM.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	1	0
			Y start address set (Initial Status = 00H)							
			Y end address set (Initial Status = 83H)							

The current Y address of the on-chip display data RAM is the Y start address by setting this instruction. In Y address count mode (Y/X = "H"), the Y address is increased from Y start address to Y end address. When Y address is equal to the Y end address, the X address is increased by 1 and the Y address returns to Y start address. The Y start and Y end addresses must be set as a pair and Y start address must be less than Y end address.

9.15. Column Address Area Set (43H)

This instruction and parameter set up the X address areas of the on-chip display data RAM.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	1	1
			X start address set (Initial Status = 00H)							
			X end address set (Initial Status = 83H)							

The current X address of the on-chip display data RAM is the X start address by setting this instruction. In X address count mode (Y/X = "L"), the X address is increased from X start address to X end address. When X address is equal to the X end address, the Y address is increased by 1 and the X address returns to X start address. The X start and X end address must be set as a pair and X start address must be less than X end address.

9.16. RAM Skip Area Set (45H)

This instruction and parameter set up the X address areas of the on-chip display data RAM.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	0	1
			0	0	0	0	0	0	RSK	

RSK : RAM Skip function ON/OFF set

RSK = 00 : No Skip (initial status)

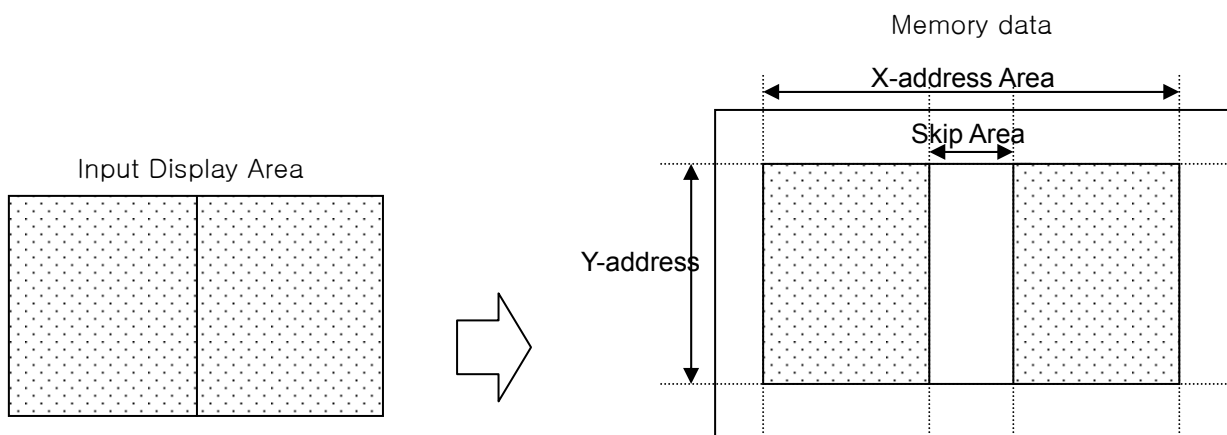
RSK = 01 : X address 34h-4Fh skip(104 RGB)

RSK = 10 : X address 3Ch-47h skip(120 RGB)

RSK = 11 : X address 30h-53h skip(96RGB)

9.16.1. RAM Skip Area Set

RAM Skip Area Set can skip a part of RAM X-address area. After setting RAM skip area, X-address counts skip this area and count. In other words, X address after skip area is changed into X address which added a part for skip area.



9.17. Display OFF (50H)

Turn the display OFF (Initial status).

When display is off, all segment and common output are VSS level.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	0

Function and Pin condition at Display OFF

Function/Pin	Condition
DC/DC booster (1'st, 2'nd, 3'rd)	ON (Operate)
SEG and COM outputs	VSS

9.18. Display ON (51H)

Turn the display ON.

In case of being standby mode, this instruction does not work. This instruction is executed after Standby mode off.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	1

Function and Pin condition at Display ON

Function/Pin	Condition
DC/DC booster (1'st, 2'nd, 3'rd)	ON(Operate)
COM outputs	VRP or VM or VRN
SEG outputs	V1 or VSS

9.19. Specified Display Pattern Set (53H)

This instruction sets the specified display pattern.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	1	1
			0	0	0	0	0	0	SDP	

SDP : Specified Display Pattern set

SDP = 00 : Normal display (Initial status)

SDP = 01 : Reverse display : Display data reversing mode setting without the contents of the display RAM

SDP = 10 : Whole display pattern becomes OFF regardless of the RAM data.

SDP = 11 : Whole display pattern becomes ON regardless of the RAM data.

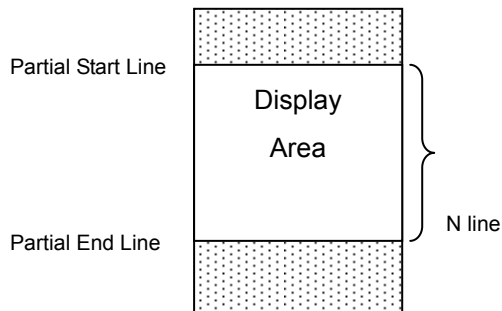
9.20. Partial Display Mode Set (55H)




RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	0	1
			0	0	0	0	0	0	0	PT

PT: Partial Display ON/OFF

PT = 0: Partial display OFF = Normal mode (Initial status)

PT = 1: Partial display ON



-  No display Area : No COM Scanning field COM = VM fixed
-  Except Partial Display Area : COM Timing is existing, but COM = VM fixed
-  Partial Display Area : Real display field

9.20.1. Operation in Partial Display Mode

On scanning except partial display area

- SEG output select V0 or V1 level depend on "FR" value.
- All of COM output is fixed VM level.

On scanning partial display area

- It is equal to be in normal mode

9.21. Partial Display Start Line Set (56H), Partial Display End Line Set (57H)

These 2 instructions set the partial display area and it is possible to display a part.

Partial Display Start Line Set (56H)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1	0
Partial start line (Initial Status = 00H)										

Partial Display End Line Set (57H)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1	1
Partial end line (Initial Status = 00H)										

COM 0	line 0
COM 1	line 1
COM 2	line 2
COM 3	line 3
	:
	:
	:
COM 128	line 128
COM 129	line 129
COM 130	line 130
COM 131	line 131

Parameter set appoints display line number. Parameter Size is able to be in a number of Display lines. Partial end line must be set to bigger number than Partial start line.

9.21.1. Display Data Write/Read

RS	WRB	RDB	DB15 ~ DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	Display RAM write in data								
1	1	0	Display RAM read out data								

9.21.2. GSM = 0 (65,536 Color Mode)

(1) 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1'st cycle	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
2'nd cycle	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

(2) 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	R4	R3	R2	R1	R0	G5	G4	G3
2'nd cycle	G2	G1	G0	B4	B3	B2	B1	B0
3'rd cycle	R4	R3	R2	R1	R0	G5	G4	G3
4'th cycle	G2	G1	G0	B4	B3	B2	B1	B0

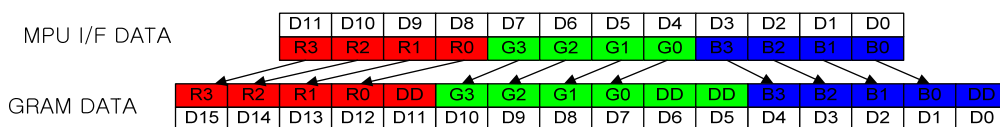
9.21.3. GSM = 1 (4,096 Color Mode)

(1) 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1'st cycle	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0
2'nd cycle	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0

(2) 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	X	X	X	X	R3	R2	R1	R0
2'nd cycle	G3	G2	G1	G0	B3	B2	B1	B0
3'rd cycle	X	X	X	X	R3	R2	R1	R0
4'th cycle	G3	G2	G1	G0	B3	B2	B1	B0



NOTE : In case of MPU I/F DATA are 4'hF, DD bit is "1" and are not 4'hF, DD bit is "0"

9.22. Booster Boosting Set (70H)

This instruction sets the Booster Boosting ratio.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	0	0	0	0
			0	0	NDC[2:0]			DC[2:0]		

NDC[2:0] : Select 3rd Booster Boosting ratio

DB5	DB4	DB3	Boosting ratio (M_3)	Remark
0	0	0	Don't Use	
0	0	1	X-4	
0	1	0	X-5	
0	1	1	X-6	default
1	0	0	Don't Use	
1	0	1	Don't Use	
1	1	0	Don't Use	
1	1	1	Don't Use	

DC[2:0] : Select 2nd Booster Boosting ratio

DB2	DB1	DB0	Boosting ratio (M_2)	Remark
0	0	0	Don't Use	
0	0	1	X 4	
0	1	0	X 5	
0	1	1	X 6	
1	0	0	X 7	default
1	0	1	X 8	
1	1	0	Don't Use	
1	1	1	Don't Use	

The 2nd, 3rd Booster efficiency is changed according to M_2 and M_3 . (See DC CHARACTERISTICS(1).)

9.23. Frame Frequency Set (7FH)

This instruction sets the Frame Frequency.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	1	1	1	1
			0	Frame Frequency (Initial Status = 2H)			0	0	0	0

DB[6]	DB[5]	DB[4]	Frame Frequency[Hz]	Remark
0	0	0	Don't Use	
0	0	1	Don't Use	
0	1	0	198	
0	1	1	148	
1	0	0	119	Default
1	0	1	99	
1	1	0	85	
1	1	1	74	

9.24. Status Read

MTP_RD = 0 : Normal Status Read (Initial status)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	BUSY	Y/X	MPRT	0	PT	STB	REV	DP

This instruction indicates the internal status of the S6B3301.

- DP : (0 : Display OFF Status, 1 : Display ON Status)
- REV : (0 : Display Image Non-Reversing, 1 : Display Image Reversing)
- STB : (0 : Standby Mode OFF Status, 1 : Standby Mode ON Status)
- PT : (0 : Partial Display Mode OFF Status, 1 : Partial Display Mode ON Status)
- MPRT: (0: MTP cell non-protection status, 1: MTP cell protection status)
- Y/X : (0: X-address Count Mode, 1 : Y-address Count Mode)
- BUSY: (0: No Busy, 1: Busy)

MTP_RD = 1: MTP Status Read

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	MPRT	MOV5	MOV4	MOV3	MOV2	MOV1	MOV0

This instruction indicates the MTP cell values of the S6B3301. (Refer to EEPROM CELL STRUCTURE)

9.25. Preliminary Instruction (8CH)

This instruction is used to write / erase MTP cell.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	0	1	1	0	0
			0	0	0	0	1	1	1	1

Parameter default (F0h)

9.26. MTP Load (E5H)

This command is used to load MTP cell.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	1	0	1

This command is valid at standby ON.

9.27. MTP Read Mode (E6H)

This command is used to read MTP cell.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	1	1	0
			0	0	0	0	0	0	0	0

MTP_RD: MTP Read Mode

- MTP_RD = 0: Normal Status Mode (Initial status)
- MTP_RD = 1: MTP Status Mode

9.28. MTP Initial Disable (E8H)

This command is used to turn MTP initial mode off. (Initial status)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	0	0	0

9.29. MTP Initial Enable (E9H)

This command is used to turn MTP initial mode on.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	0	0	1

9.30. MTP Select Mode Off (EAH)

This command is used to turn MTP select mode off.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	0	1	0

9.31. MTP Select Mode On (EBH)

This command is used to turn MTP select mode on. (Initial status)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	0	1	1

9.32. Offset Volume Set (EDH)

This command is used to set offset value x (-32 to +31) to electronic volume by 2s complement.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	1	0	1
			0	0	OV5	OV4	OV3	OV2	OV1	OV0

OV5	OV4	OV3	OV2	OV1	OV0	Offset Volume
0	1	1	1	1	1	31
:	:	:	:	:	:	
0	0	0	0	0	1	1
0	0	0	0	0	0	0
1	1	1	1	1	1	-1
	:	:	:	:	:	:
1	0	0	0	0	0	-32

9.33. MTP Write Disable (EEH)

This command is used to cut off offset value (OV) from EEPROM cells.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	1	1	0

9.34. MTP Write Enable (EFH)

This command is used to write offset value (OV) into EEPROM cells.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	1	1	1

9.35. INSTRUCTION PARAMETER

Table 22. Instruction Parameter

Instruction	Hex	Para	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Oscillation Mode Set	02H	1	0	0	0	0	0	0	EXT	0
			Initial value (00h)							
Driver Output Mode Set	10H	1	0	0	DLN		MY	MX	SWP	CDIR
			Initial value (00h)							
Monitor Signal control	18H	1	0	0	0	0	0	PM	CL	FR
			Initial value (00h)							
Temperature Compensation Set	28H	1	0	0	0	0	0	0	TCS	
			Initial value (00h)							
Contrast Control	2AH	1	0	Contrast control value(0 to 127)						
			Initial value (00h)							
Addressing Mode Set	30H	1	0	0	GSM	DSG	SGF	SGP		SGM
			Initial value (00h)							
ROW Vector Mode Set	32H	1	0	0	0	0	INC			VEC
			Initial value (00h)							
N-block Inversion Set	34H	1	FIM	FIP	0	N-block Inversion				
			Initial value (00h)							
Driving Mode Set	36H	1	0	0	0	0	0	0	0	LFS
			Initial value (00h)							
Entry Mode Set	40H	1	16B	0	0	0	0	MDI	Y/X	RMW
			Initial value (00h)							
Row address Area Set	42H	2	Y Start address set							
			Initial value (00h)							
			Y end address set							
			Initial value (83h)							
RAM Skip Area Set	45H	1	0	0	0	0	0	0	RSK	
			Initial value (00h)							
Column Address Area Set	43H	2	X start address set							
			Initial value (00h)							
			X end address set							
			Initial value (83h)							
Specified Display Pattern Set	53H	1	0	0	0	0	0	0	SDP	
			Initial value (00h)							
Partial Display Mode Set	55H	1	0	0	0	0	0	0	0	PT
			Initial value (00h)							
Partial Display Start Line Set	56H	1	Partial start line							
			Initial value (00h)							
Partial Display End Line Set	57H	1	Partial end line							
			Initial value (00h)							
Booster Boosting Set	70H	1	0	0	NDC[2:0]			DC[2:0]		
			Initial value (1Ch)							
Frame Frequency Set	7FH	1	0	Frame Frequency			0	0	0	0
			Initial value (40h)							
MTP Read Mode	E6H	1	0	0	0	0	0	0	0	MTP_R D
			Initial value (00h)							
Offset Volume Set	EDH	1	0	0	OV5	OV4	OV3	OV2	OV1	OV0
			Initial value (00h)							

Parameter: The number of parameter bytes that follows instruction data.

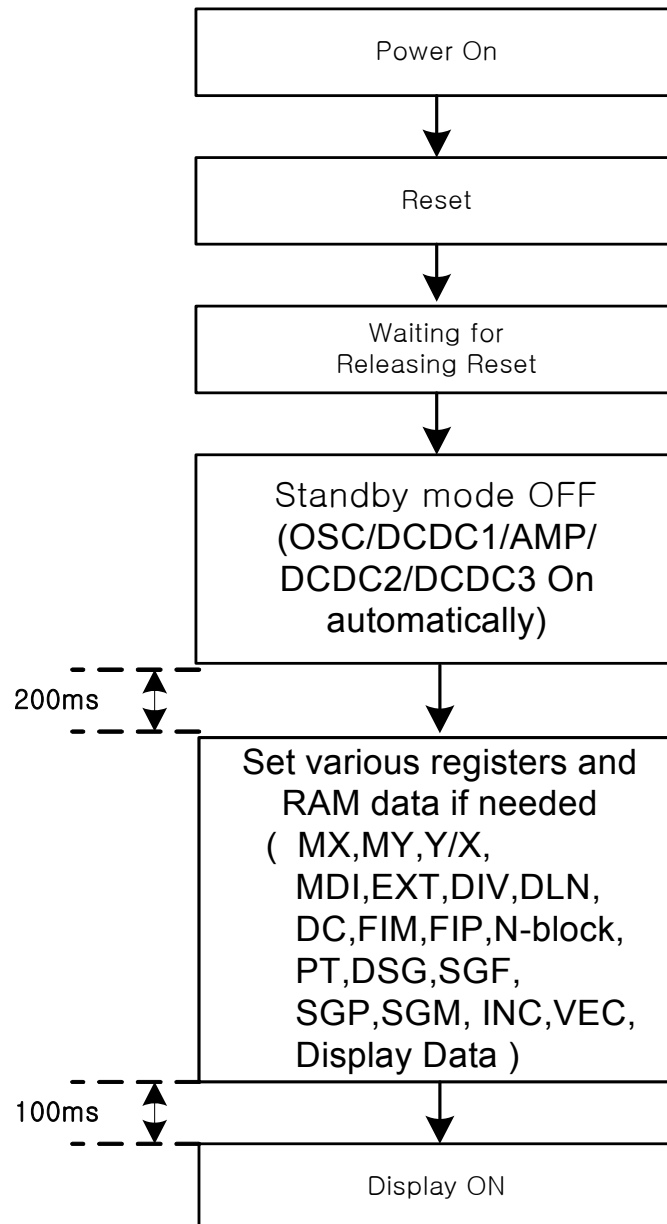
9.36. Reset Operation

When RSTB becomes “L”, following procedure is occurred.

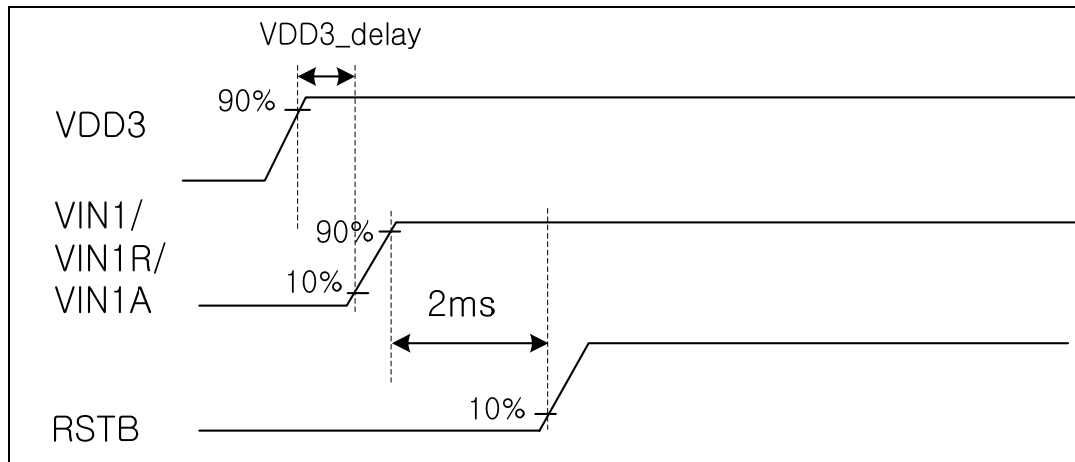
- X start address: 0, X end address: 131
- Y start address: 0, Y end address: 131
- Display OFF
- Read Modify Write Mode OFF
- Function Mode Set
 - EXT = 0: Internal Oscillator Mode
 - LFS = 0: Normal Frequency Mode
 - 16B = 0: Data Bus Width 8bit Mode
 - MDI = 0: Memory Data Inversion OFF
 - MX = 0: Column Address increment
 - MY = 0: Row Address increment
 - Y/X = 0: X-address Count Mode
 - Standby Mode ON
- Duty Set
 - Display Duty : DLN = 00 (132 duty)
- N-block inversion
 - FIM =0: Forcing Inversion OFF
 - N-block inversion = 00H: frame inversion
- Partial Display Mode
 - PT = 0: Partial Display Mode OFF
- Partial Display Area Set
 - Partial start line = 00H
 - Partial end line = 00H
- Addressing Mode Set
 - DSG = 0: Mode 0
 - SGF = 0: SG Frame Inversion OFF
 - SGP = 00: Same phase in all pixel
- Row Vector Mode Set
 - INC =000: Increment every subgroup
 - VEC=0: R1→R2→R3→R4→R1→...

10. POWER ON/OFF SEQUENCE

10.1. Power On Sequence

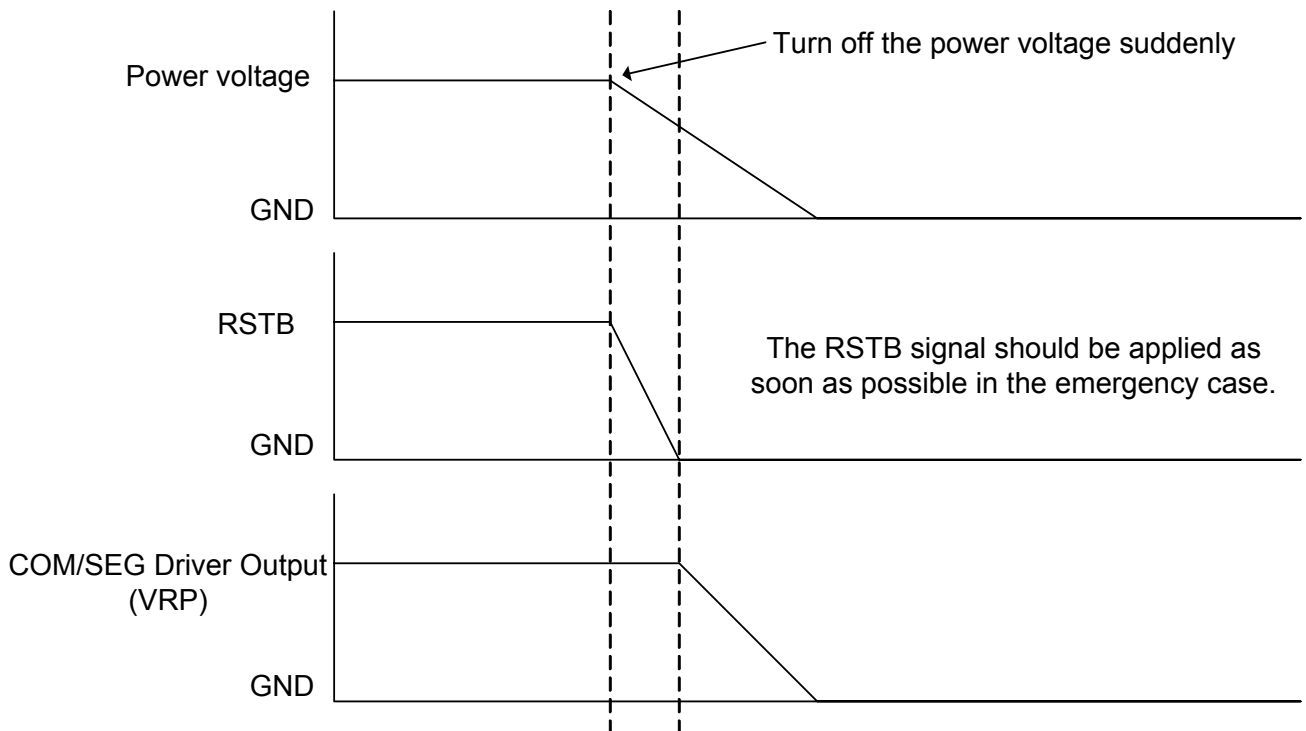
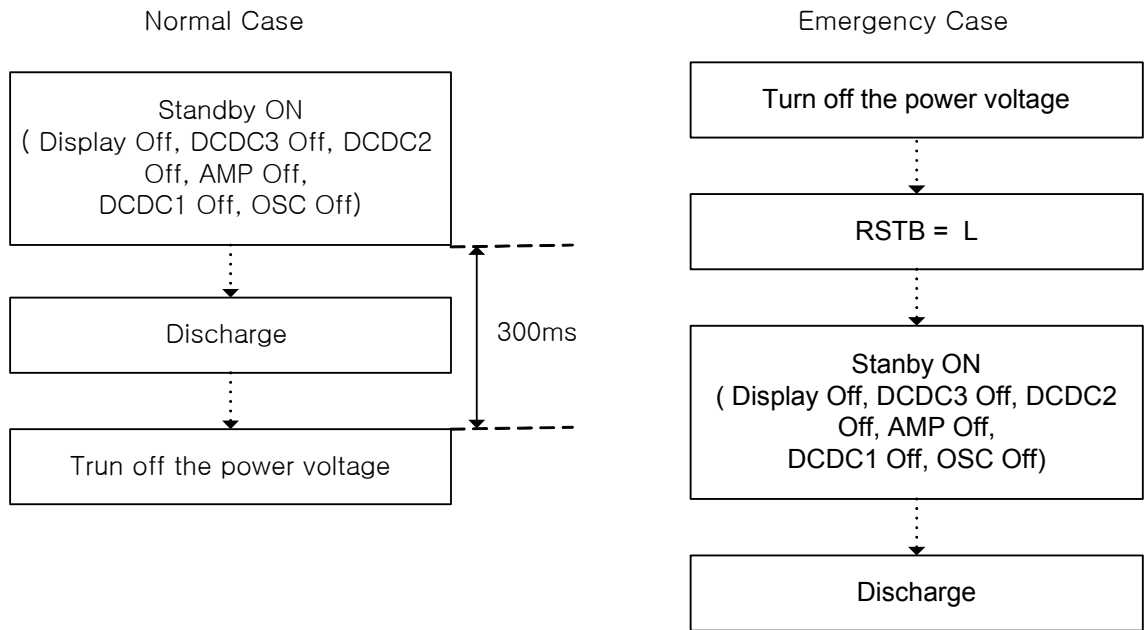


10.2. External Power Input Sequence



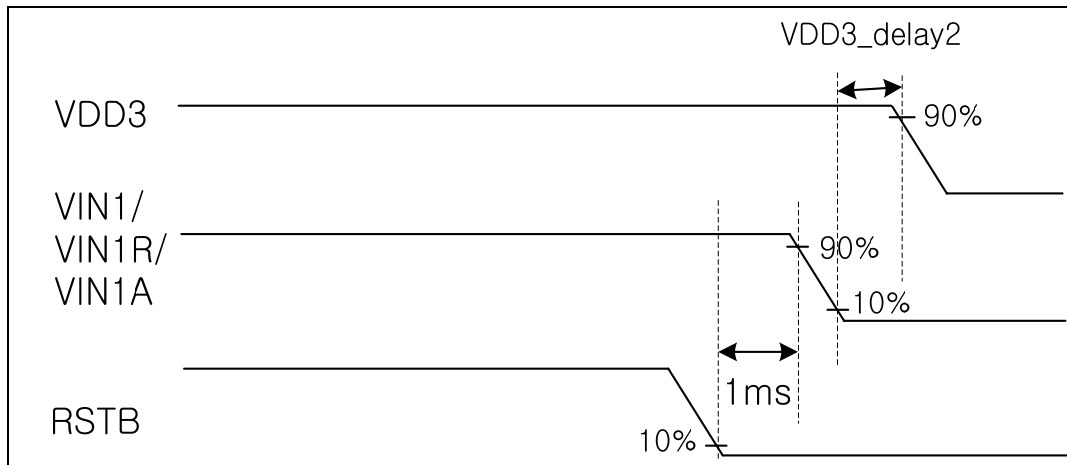
VDD3 must be applied earlier than VIN1/VIN1R/VIN1A or at least applied simultaneously with these signals. When C1 of table24. External component is $1\mu\text{F}$, RSTB must be applied after VIN1/VIN1R/VIN1A have been applied. The applied time gap between VIN1/VIN1R/VIN1A and RSTB is minimum 2ms. As C1 becomes larger, this time gap must be increased. Otherwise function is not guaranteed.

10.3. Power Off Sequence



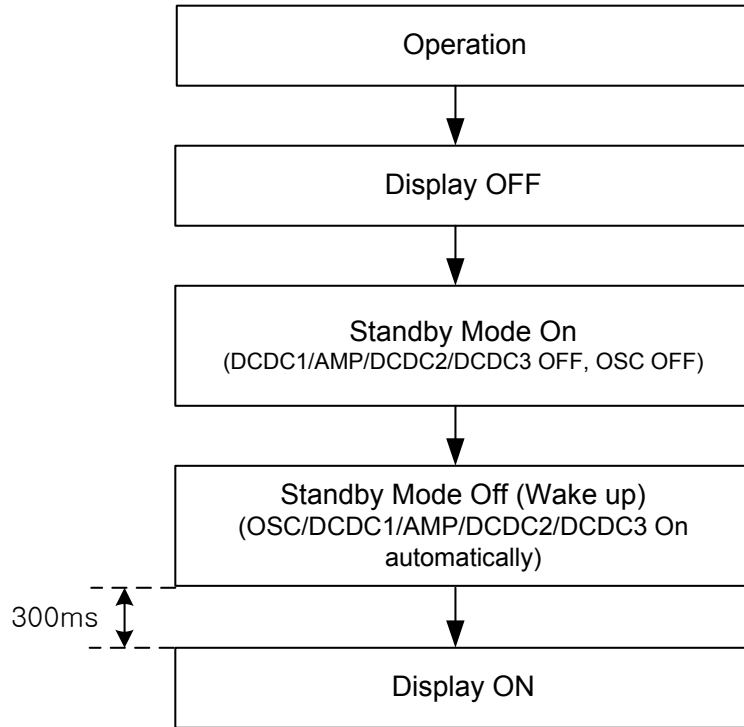
Note: When the signal of the hardware reset comes during the power-off period, COM/SEG output is forcibly lowered to the GND levels.

10.4. External Power Off Sequence



VDD3 must be powered down later than VIN1/VIN1R/VIN1A or at least powered down simultaneously with these signals. VIN1/VIN1R/VIN1A must be powered down after RSTB have been powered down. The time gap of powered down between RSTB and VIN1/VIN1R/VIN1A is minimum 1ms. Otherwise function is not guaranteed.

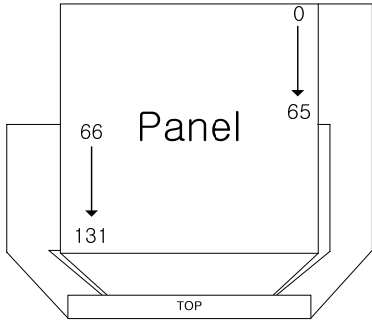
10.5. Wake up Sequence



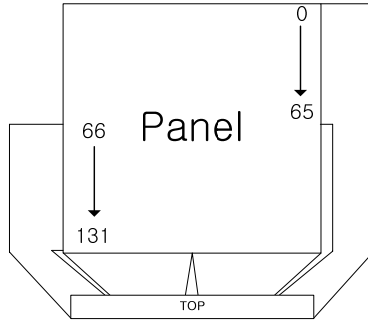
11. DISPLAY APPLICATIONS BETWEEN S6B3301 And PANEL

By combination of DLN, CDIR, RSK bits setting, LCD panel and S6B3301 can be connected in many ways.

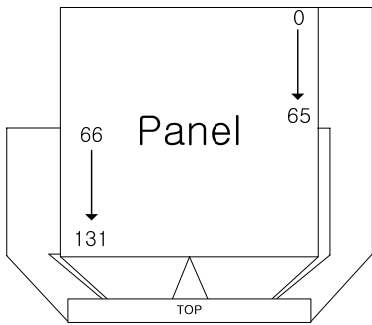
11.1. 132 DUTY DISPLAY (ZIGZAG_MODE=0)



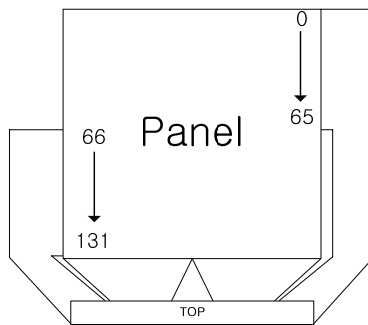
DLN = 00
CDIR = 0
RSK = 00
(132RGB)



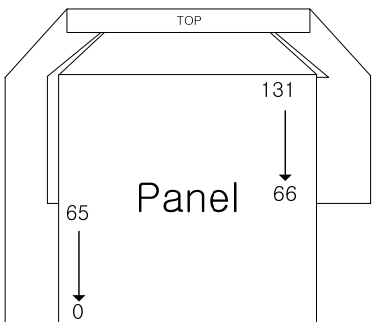
DLN = 00
CDIR = 0
RSK = 10
(120RGB)



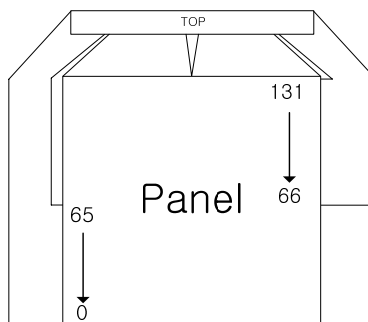
DLN = 00
CDIR = 0
RSK = 01
(104RGB)



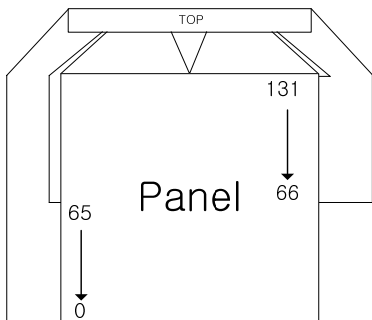
DLN = 00
CDIR = 0
RSK = 11
(96RGB)



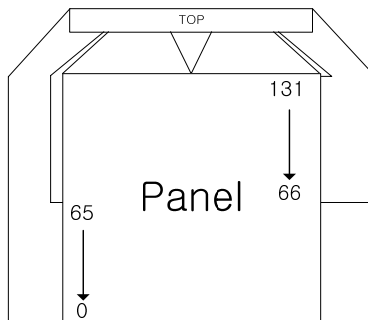
DLN = 00
CDIR = 1
RSK = 00
(132RGB)



DLN = 00
CDIR = 1
RSK = 10
(120RGB)

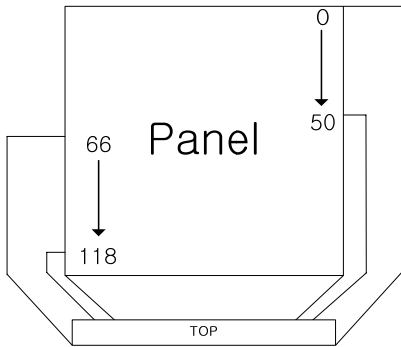


DLN = 00
CDIR = 1
RSK = 01
(104RGB)

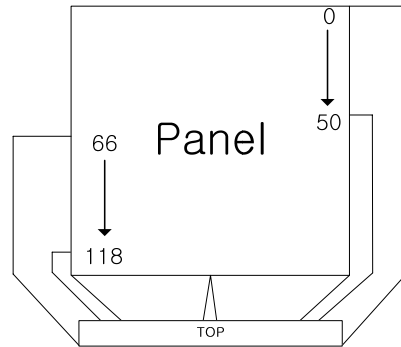


DLN = 00
CDIR = 1
RSK = 11
(96RGB)

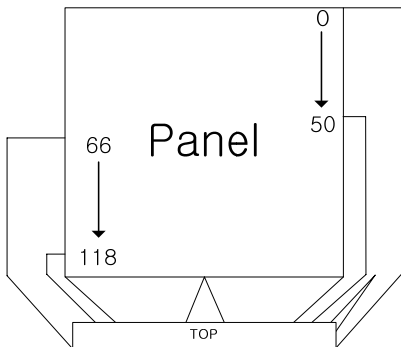
11.2. 104 DUTY DISPLAY (ZIGZAG_MODE=0)



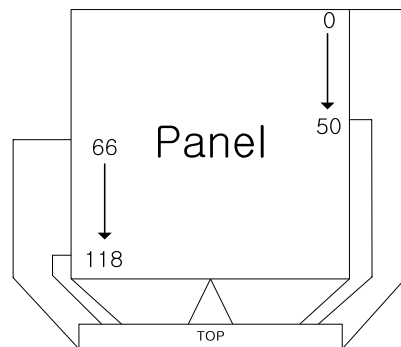
DLN = 01
CDIR = 0
RSK = 00
(132RGB)



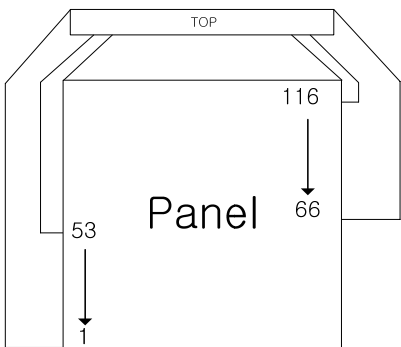
DLN = 01
CDIR = 0
RSK = 10
(120RGB)



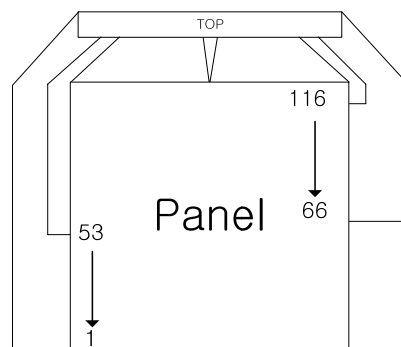
DLN = 01
CDIR = 0
RSK = 01
(104RGB)



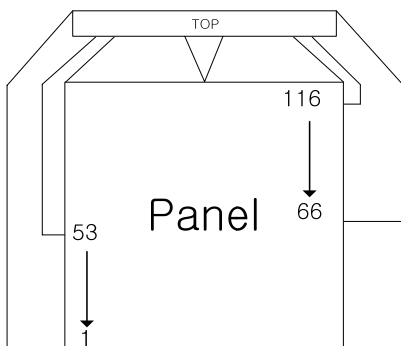
DLN = 01
CDIR = 0
RSK = 11
(96RGB)



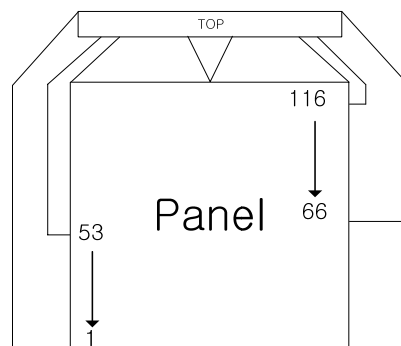
DLN = 01
CDIR = 1
RSK = 00
(132RGB)



DLN = 01
CDIR = 1
RSK = 10
(120RGB)

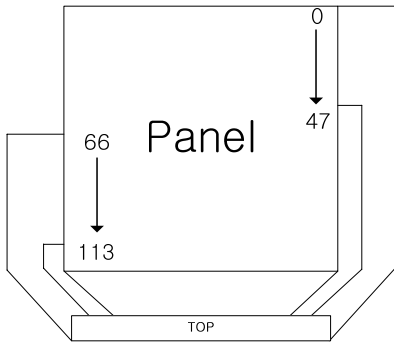


DLN = 01
CDIR = 1
RSK = 01
(104RGB)

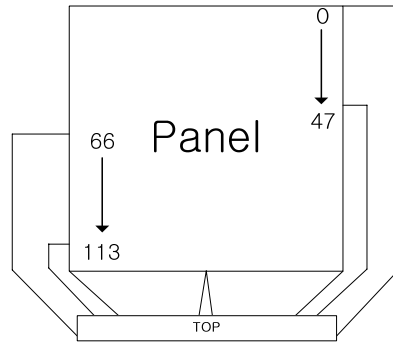


DLN = 01
CDIR = 1
RSK = 11
(96RGB)

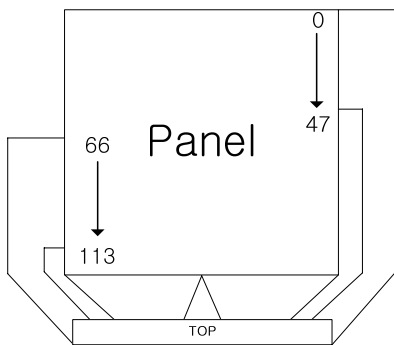
11.3. 96 DUTY DISPLAY (ZIGZAG_MODE=0)



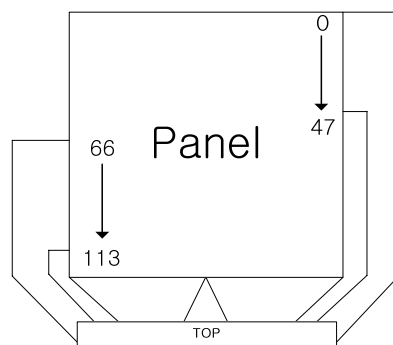
DLN = 11
CDIR = 0
RSK = 00
(132RGB)



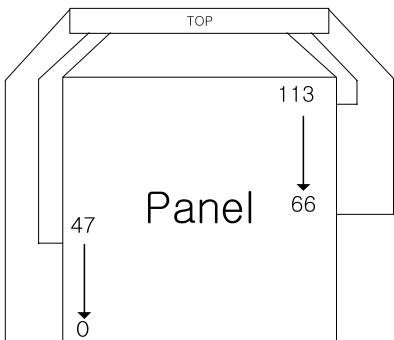
DLN = 11
CDIR = 0
RSK = 10
(120RGB)



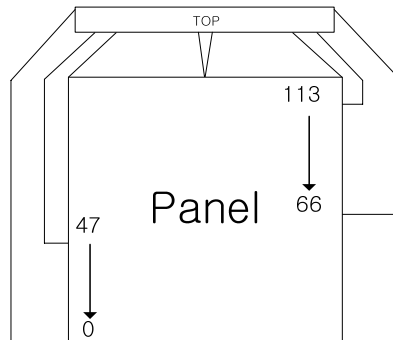
DLN = 11
CDIR = 0
RSK = 01
(104RGB)



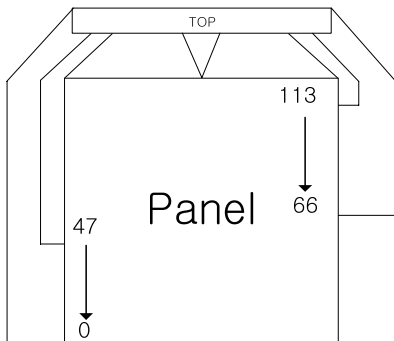
DLN = 11
CDIR = 0
RSK = 11
(96RGB)



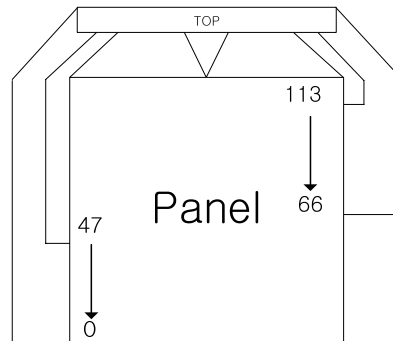
DLN = 11
CDIR = 1
RSK = 00
(132RGB)



DLN = 11
CDIR = 1
RSK = 10
(120RGB)

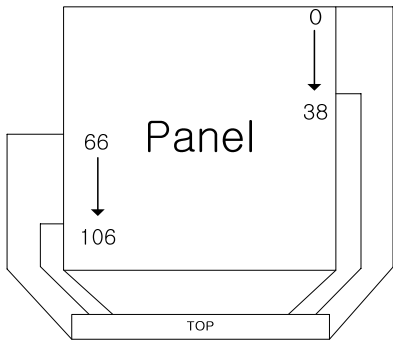


DLN = 11
CDIR = 1
RSK = 01
(104RGB)

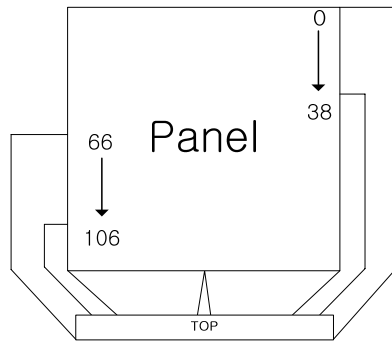


DLN = 11
CDIR = 1
RSK = 11
(96RGB)

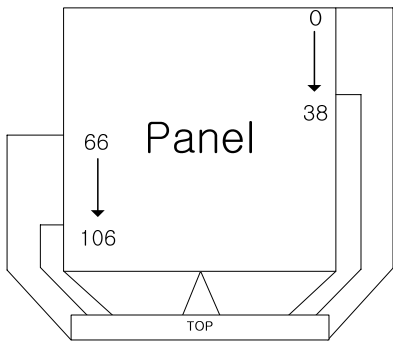
11.4. 80 DUTY DISPLAY (ZIGZAG_MODE=0)



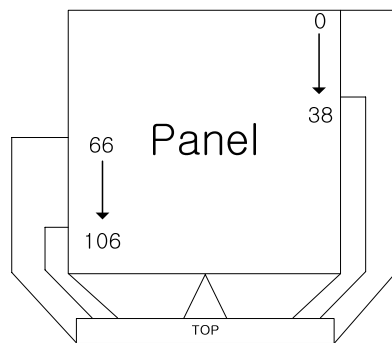
DLN = 10
CDIR = 0
RSK = 00
(132RGB)



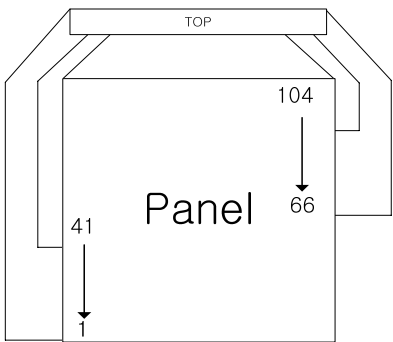
DLN = 10
CDIR = 0
RSK = 10
(120RGB)



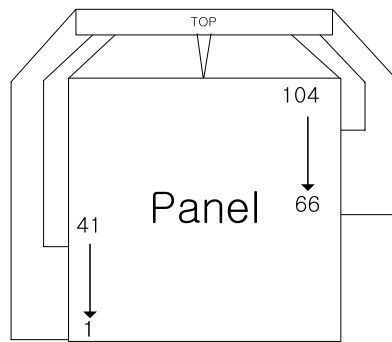
DLN = 10
CDIR = 0
RSK = 01
(104RGB)



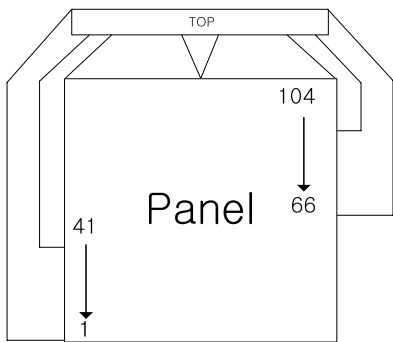
DLN = 10
CDIR = 0
RSK = 11
(96RGB)



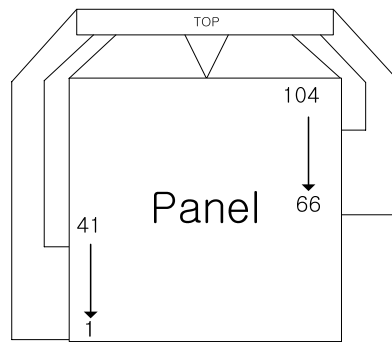
DLN = 10
CDIR = 1
RSK = 00
(132RGB)



DLN = 10
CDIR = 1
RSK = 10
(120RGB)



DLN = 10
CDIR = 1
RSK = 01
(104RGB)



DLN = 10
CDIR = 1
RSK = 11
(96RGB)

12. SPECIFICATIONS

12.1. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage range	VDD3	-0.3 to +5.0	V
	VIN1	-0.3 to +5.0	V
LCD Supply Voltage range	VCC - VEE	25	V
Input Voltage range	Vin	- 0.3 to VDD3 +0.3	V
Operating Temperature range	TOPR	-30 to +70	°C
Storage Temperature range	TSTR	-55 to +150	°C

12.2. Operating voltage

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage (1)	VDD3	1.65	-	3.0	V
Supply Voltage (2)	VIN1	2.4	2.8	3.0	V

12.3. DC CHARACTERISTICS (1)

(VSS = 0V, VDD3 = 1.65 to 3.0V, Ta = -30 to 70 °C)

Item	Symbol	Condition	Min	Typ.	Max	Unit	Remarks
Operating voltage	VDD3		1.65		3.0	V	VDD3
Operating voltage	VIN1		2.4	2.8	3.0	V	VIN1, VIN1A
Operating voltage	VIN45		2.4	-	6.0	V	VIN45
Operating voltage	2Vr	$2Vr = VRP - VRN $	14	-	20	V	VRP, VRN
Output voltage	REG_OUT	REG_OUT voltage	1.5 ± 0.05			V	REG_OUT
Driving voltage input range (*1)	VM	External power supply mode	1.4		2.0	V	VM
	VCC		8.4		12.0	V	VCC
	VEE		-8.0		-5.6	V	VEE
Input voltage	High	VIH	0.8VDD3	-	VDD3	V	
	Low	VIL	VSS	-	0.2VDD3	V	
Output voltage	High	VOH	IOH = 0.5mA	0.8VDD3	-	VDD3	V
	Low	VOL	IOL = -0.5mA	VSS	-	0.2VDD3	V
Input leakage current	IIL	VIN = VDD or VSS	-1.0	-	+1.0	μA	
Output leakage current	IOZ	VIN = VDD or VSS	-3.0	-	+3.0	μA	
Oscillator Frequency Tolerance	Normal or Partial	FOSC1	(fFR=119Hz target), DSG=0, 132 display lines VDDO=1.5V, Temp=25°C	1534.5	1705	1875.5	kHz
Driving voltage input range (*2)	V1		2.8		4.0	V	
	VM		1.4		2.0		

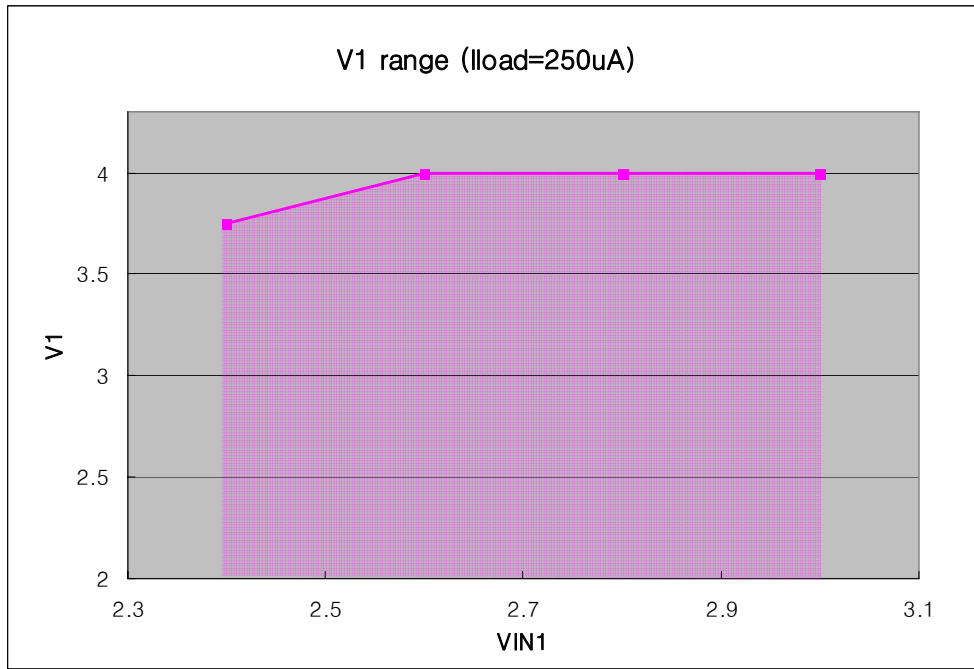
(*1) The Driving voltage range depend on the operating voltage (VIN1).

$V1 < VIN1 * 2 - 1.05$ (@Iload=250uA, V1 maximum voltage=4V)

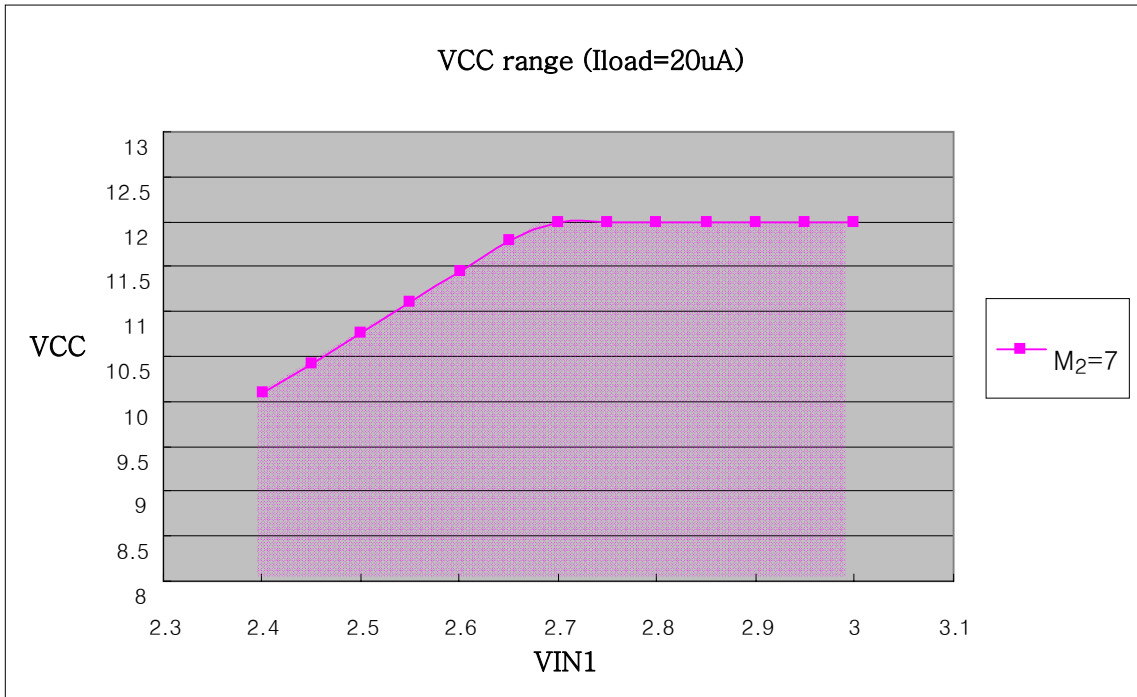
$VCC < (VIN1 - 0.7) * M_2 - 1.8$ (@Iload=20uA, VCC maximum voltage=12V)

$VEE > VIN1 * (M_3) + 0.7 * (-M_3 + 1) + 2.7$ (@Iload=20uA, VEE minimum voltage=-8)

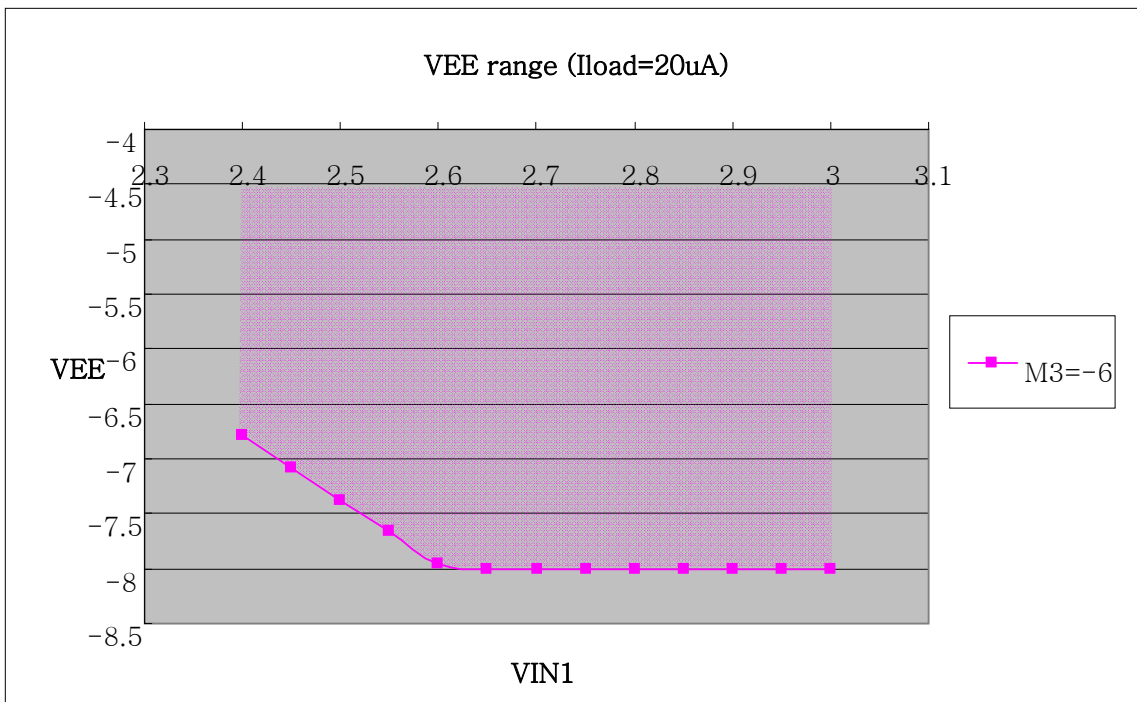
→ M_2 and M_3 is Booster Boosting Ratio. (See Booster Boosting Set (70H))



* $V1 < VIN1 * 2 - 1.05$ (@Iload=250uA, V1 maximum voltage=4V)



* $VCC < (VIN1 - 0.7) * M_2 - 1.8$ (@Iload=20uA, VCC maximum voltage=12V)



* $VEE > VIN1 * (M_3) + 0.7 * (-M_3 + 1) + 2.7$ (@Iload=20uA, VEE minimum voltage=-8)

12.4. DC CHARACTERISTICS (2)

(VSS = 0V, VDD3 = 1.65 to 3.0V, VIN1=2.4 to 3.0V, Ta = -30 to 70 °C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Driver output resistance	SEG	R_{ON-Seg} V1=3.0 V, V0=0V, Ta = 25°C, Iload=50uA	-	1.5	2.0	kΩ	SEgn
	COM	R_{ON-Com} VCC=9 V, VEE=-6.0V, Ta = 25°C, Iload=100uA	-	1.5	2.0	kΩ	COMn
Current consumption	Normal Mode	IDD VDD3=VIN1=3.0V, V1=3.0V, Bias=1/5, DC=x2, Ta=25°C, Display line=132 DSG=0 (1dummy) fOSC=1705kHz (fFR=120Hz) No load, No access, All white pattern	-	900	1100	μA	VDD3 VIN1

* : "IDD" is determined from lowest power consumption for dc-dc converter.

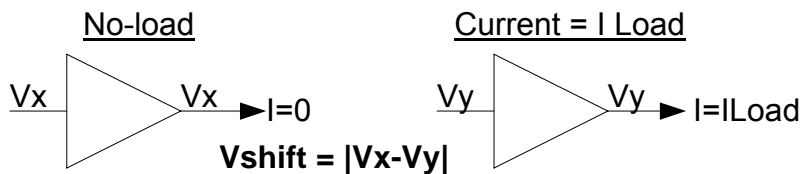
12.5. DC CHARACTERISTICS (3)

(VSS = 0V, VDD3 = 1.65 to 3.0V, VIN1=2.4 to 3.0V, Ta = -30 to 70 °C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Voltage shift range(*1)	Δ VRP	Low current mode Isource = 20uA	-	-	200	mV	VRP
	Δ V1	Low current mode Isource = 250uA	-	-	50	mV	V1
	Δ VM	Low current mode Isource,sink = 250uA	-	-	50	mV	VM
	Δ VRN	Low current mode Isink = 20uA	-	-	200	mV	VRN

(*1) Voltage shift means output voltage deference between output current = Iload and no-load.

Refer to the following figure. (In case of source current mode)



Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Tolerance of Bias ratio	Δ VRP_0 Δ VRN_0(*1)	No load	-200	-	+200	mV	VRP VRN

(*1) Tolerance of bias ratio definition

$$\Delta VRP_0 = (VRP - VM) - VM * Bias$$

$$\Delta VRN_0 = (VM - VRN) - VM * Bias$$

12.6. DC CHARACTERISTICS (4)

(VSS = 0V, VDD3 = 1.65 to 3.0V, VIN1=2.4 to 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks	
Temperature compensation	ΔVt	VDD3=VIN1=3.0V, 25°C to 70 °C	-0.02	-	+0.02	%/°C	V1	
Tolerance of Contrast step of V1	$\Delta Vstep$		3.13	6.27	9.41	mV	V1	
Voltage range	$\Delta V1$	Contrast set = 7Fh	V1	3.95	4.0	4.05	V	V1
			VM	1.95	2.00	2.05	V	VM
	ΔVM	Contrast set = 00h	V1	2.75	2.80	2.85	V	V1
			VM	1.35	1.40	1.45	V	VM

Item		Condition		Max	Unit	Ref	
		Load current	Voltage range				
Offset Voltage	VRP-VM - VM - VRN	I Load = +20uA (VRP)	VRP=8.4~12 V V1=2.8~4.0V VM=1.4~2.0V VRN=-5.6~-8.0 V	100	mV	Fig.1	
		I Load = -20uA (VRN)					
	V1-VM - VM-V0	I Load = +100uA (V1)		50	mV		Fig.2
		I Load = +100uA (VM)					
		I Load = +100uA (V1)					
		I Load = -100uA (VM)					

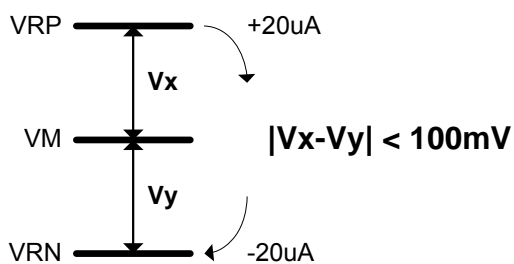


Fig. 1: Offset voltage definition (VRP,VM,VRN)

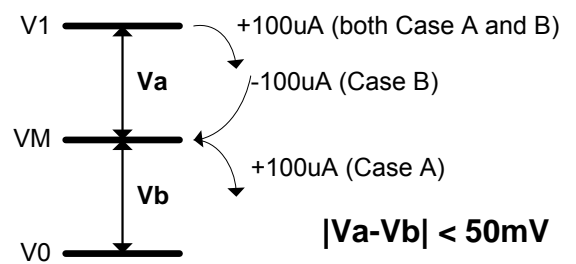


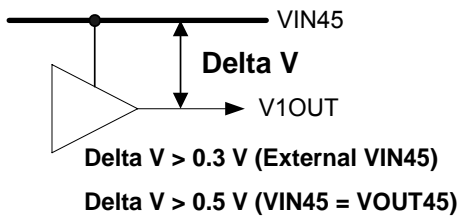
Fig. 2: Offset voltage definition (V1,VM,V0)

12.7. DC CHARACTERISTICS (5)

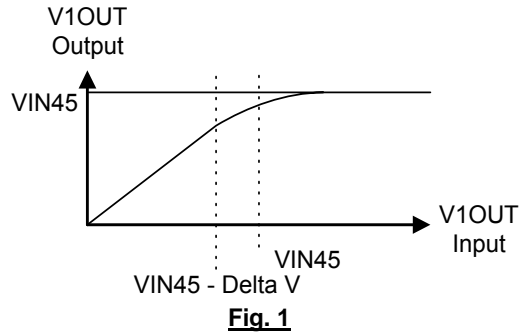
(VSS = 0V, VDD3 = 1.65 to 3.0V, VIN1=2.4 to 3.0V, Ta = -30 to 70 °C)

Item		Range	
		Min	Max (DC = X2.0)
Voltage Level	V1OUT	2.8 V	4.0 V(*1)
	VMOUT	1.4 V	2.0 V(*2)

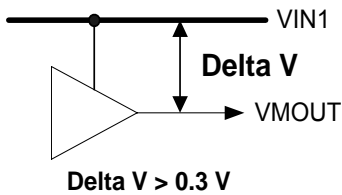
(*1) This definition is shown as below



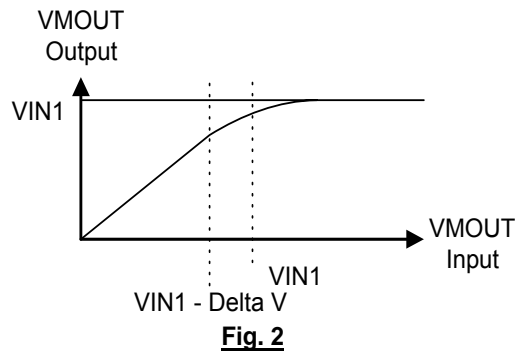
If V1OUT input voltage is set over VIN45, V1OUT output voltage must be clipped near VIN45. In this case, V1OUT output level must not be unstable. Refer to Fig.1



(*2) This definition is shown as below



If VMOUT input voltage is set over VIN1, VMOUT output voltage must be clipped near VIN1. In this case, VMOUT output level must not be unstable. Refer to Fig.2



12.8. AC CHARACTERISTICS

12.8.1. Read / Write Characteristics (8080-series MPU)

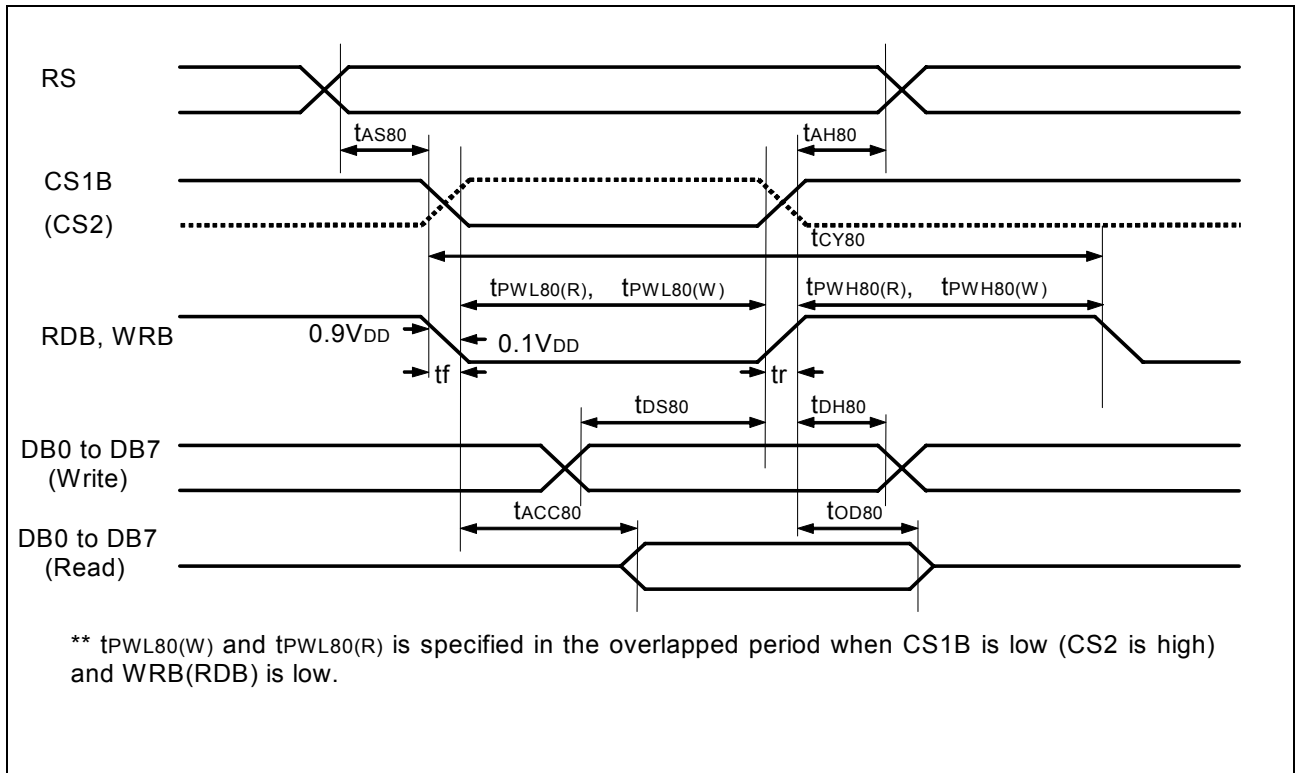


Figure 15. Parallel Interface (8080-series MPU) Timing Diagram

Table 23. AC Characteristics (8080-series Parallel Mode)

(VSS=0V, VDD3 = 1.8V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min	Max	Unit
Address setup time	RS	t_{AS80}		0		ns
Address hold time		t_{AH80}		0		
System cycle time(Write)		t_{CY80}		100		Ns
Pulse width low for write	WRB	$t_{PWL80(W)}$		40		Ns
Pulse width High for write		$t_{PWH80(W)}$		40		
Pulse width low for read	RDB	$t_{PWL80(R)}$		200		Ns
Pulse width high for read		$t_{PWH80(R)}$		100		
Data setup time	DB0 to DB7	t_{DS80}		10		Ns
Data hold time		t_{DH80}		10		
Read access time	DB0 to DB15	t_{ACC80}	CL = 50 pF		150	Ns
Output disable time		t_{OD80}	no load	20		Ns

NOTE : (tr + tf) < (tCY80 - tPWL80(W) - tPWH80(W)) for write,
 (tr + tf) < (tCY80 - tPWL80(R) - tPWH80(R)) for read

12.8.2. Read / Write Characteristics (6800-series MPU)

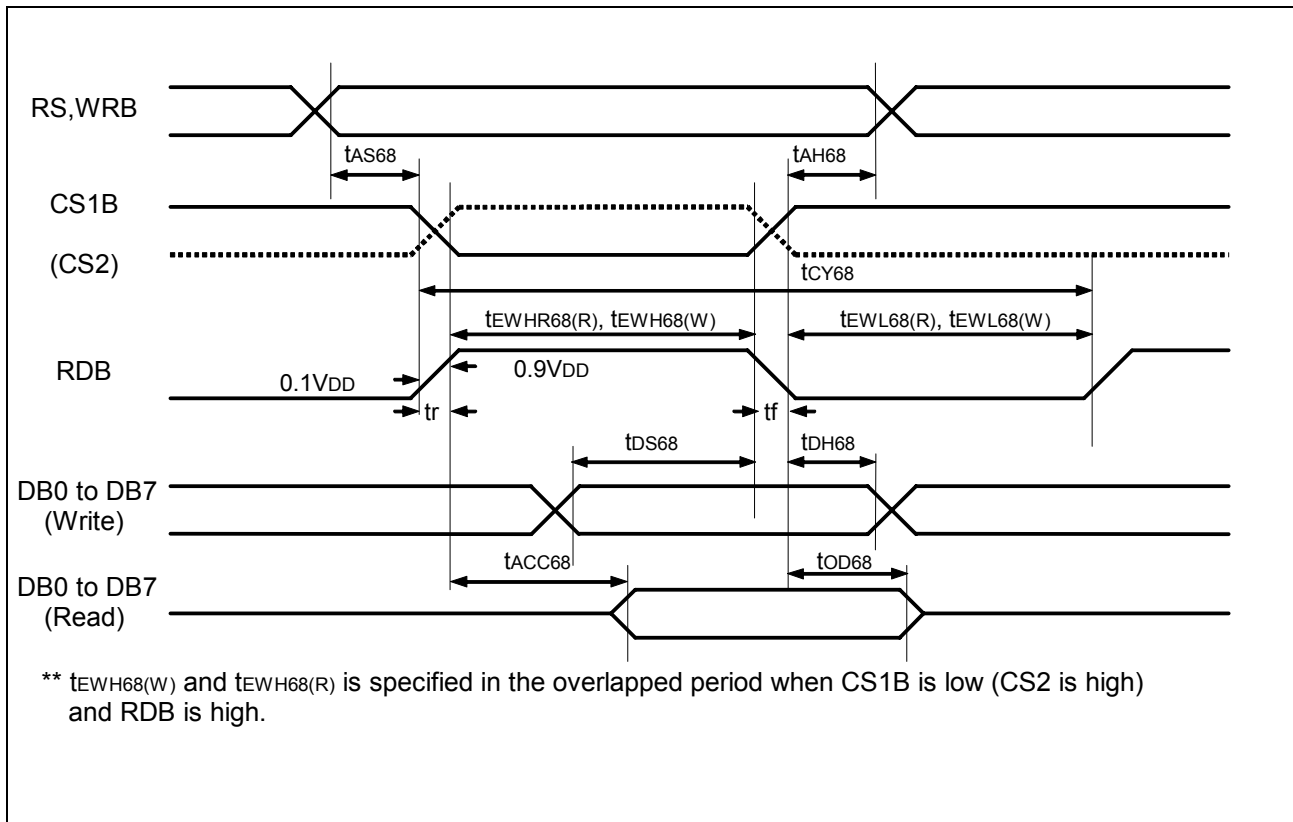


Figure 16. Parallel Interface (6800-series MPU) Timing Diagram

Table 24. AC Characteristics (6800-series Parallel Mode)

(VSS=0V, VDD3 = 1.8V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min	Max	Unit
Address setup time	RS	tAS68		0		Ns
Address hold time	WRB	tAH68		0		Ns
System cycle time(Write)		tCY68		100		Ns
Enable width high for write	RDB	tEWH68(W)		40		Ns
Enable width low for write		tEWL68(W)		40		Ns
Enable width high for read	RDB	tEWH68(R)		200		Ns
Enable width low for read		tEWL68(R)		100		Ns
Data setup time	DB0 to DB15	tDS68		10		Ns
Data hold time		tDH68		10		Ns
Read access time		TACC68	CL = 50 pF		150	Ns
Output disable time		tOD68	no load	20		Ns

NOTE: (tr + tf) < (tCY68 - tEWH68(W) - tEWL68(W)) for write,
 (tr + tf) < (tCY68 - tEWH68(R) - tEWL68(R)) for read

12.8.3. Serial Data Interface (4 Pin) Timing

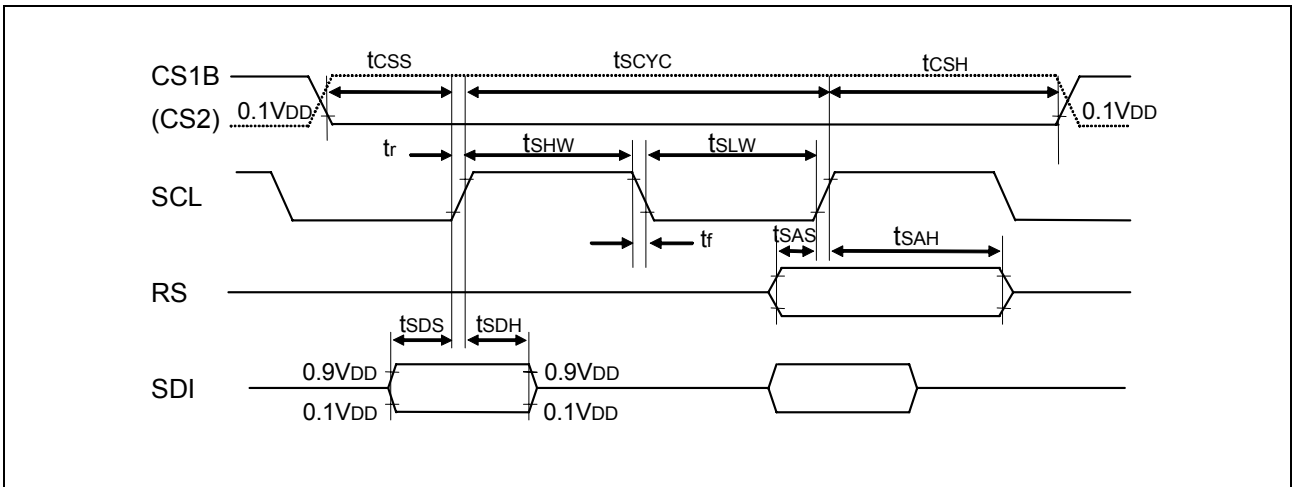


Figure 17. Serial Interface (4 Pin) Timing Diagram

Table 25. Serial Data Interface Timing

(VSS=0V, VDD3 = 1.8V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min	Unit
SCL Cycle Time	SCL	tSCYC		75	ns
SCL High Pulse Width	SCL	tSHW		20	ns
SCL Low Pulse Width	SCL	tSLW		20	ns
SDI Setup time	SDI	tSDS		10	ns
SDI Hold time	SDI	tSDH		10	ns
RS Setup time	RS	tSAS		10	ns
RS Hold time	RS	tSAH		10	ns
Chip Select Setup time	CS1B (CS2)	tCSS		10	ns
Chip Select Hold time	CS1B (CS2)	tCSH		0	ns

NOTE: $(tr + tf) < (tSCYC - tSHW - tSLW)$ for write,

12.8.4. Serial Data Interface (3 Pin) Timing

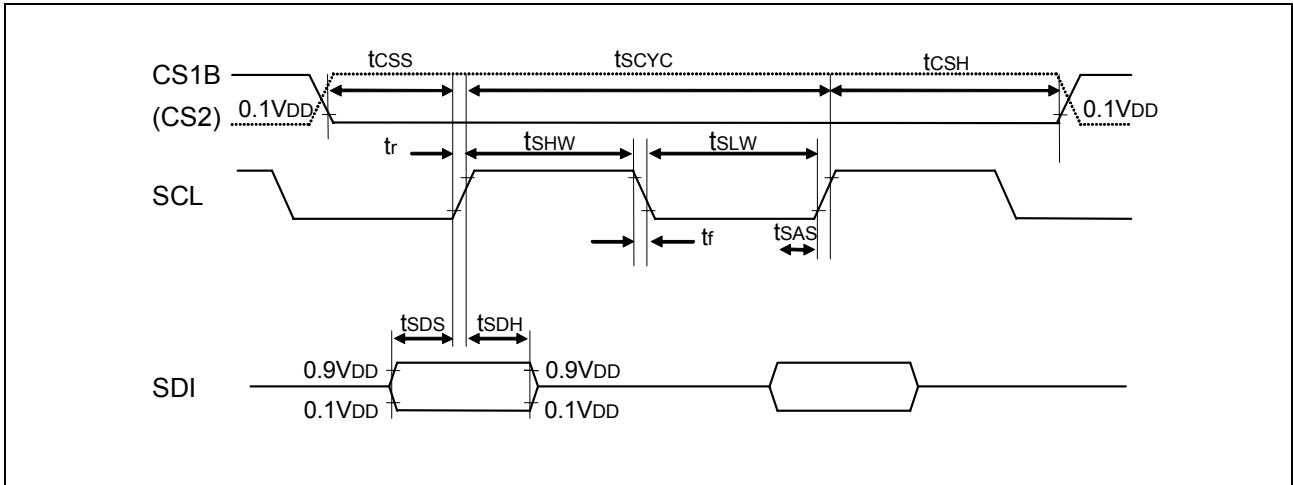


Figure 18. Serial Interface (3 Pin) Timing Diagram

Table 26. Serial Data Interface Timing

(VSS=0V, VDD3 = 1.8V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min	Unit
SCL Cycle Time	SCL	tSCYC		75	ns
SCL High Pulse Width	SCL	tSHW		20	ns
SCL Low Pulse Width	SCL	tSLW		20	ns
SDI Setup time	SDI	tSDS		10	ns
SDI Hold time	SDI	tSDH		10	ns
Chip Select Setup time	CS1B (CS2)	tCSS		10	ns
Chip Select Hold time	CS1B (CS2)	tCSH		0	ns

NOTE: $(t_r + t_f) < (t_{SCYC} - t_{SHW} - t_{SLW})$ for write,

12.8.5. Reset Input Timing

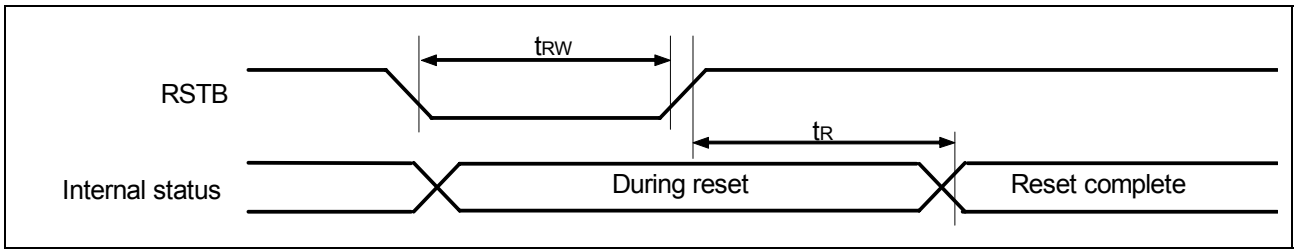


Figure 19. Reset Input Timing Diagram

Table 27. AC Characteristics (Reset mode)

(VSS=0V, VDD3 = 1.8V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset low pulse width	RSTB	TRW		1000	-	ns
Reset time	-	tR		-	1000	ns

13. MTP CALIBRATION MODE

13.1. Sequence for Setting the Modified Electronic Volume

Next figure is a Block Diagram of Sequence for Setting the Modified Electronic Volume.

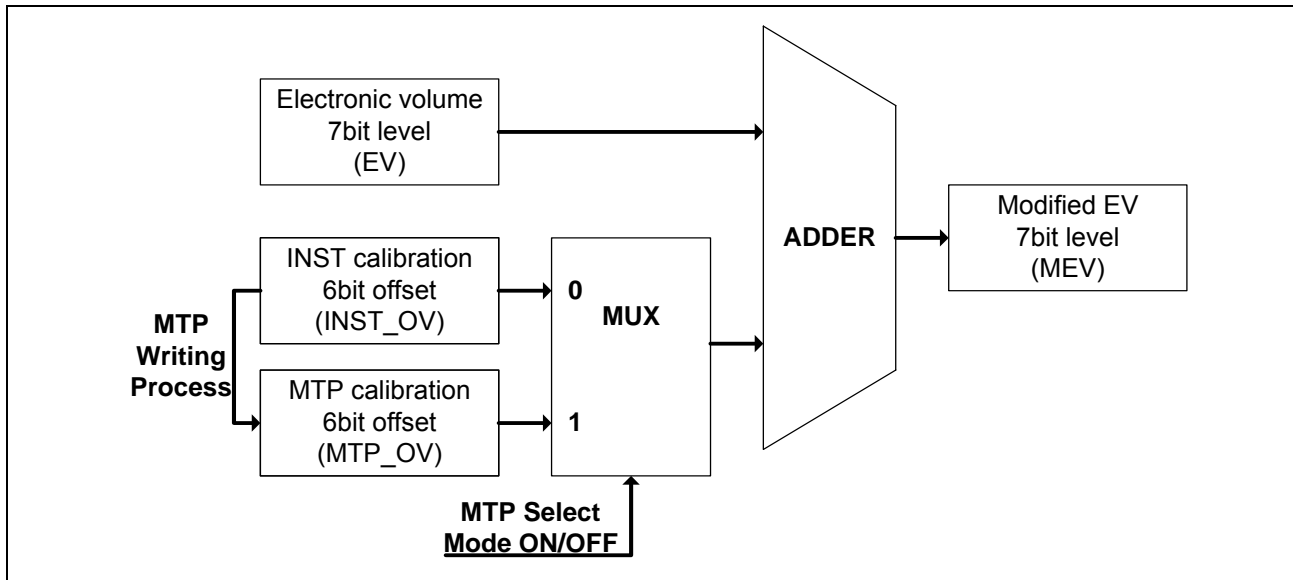


Figure 20. Sequence for Setting the Modified Electronic Volume

Initially, MTP cell is not programmed and has 6'b00000 value. When the external reset is applied, MTP select mode is On. MEV is EV + MTP_OV. Since MTP_OV is 6'b00000, MEV is EV. For V1OUT calibration, the instruction "MTP select mode off" is executed, and then MEV is EV + OV and user can adjust MEV value using the instruction "Set offset volume register". When MEV overflows or underflows, MEV will be saturated. Repeat this step until end of the calibration. If V1OUT calibration is suitable, MTP writing process is executed, and then MTP cell is programmed and MTP_OV is programmed with OV. Finally, V1OUT calibration process is finished. Again, when the external reset is applied, MTP select mode is ON. MEV is EV + MTP_OV. Accordingly MEV is the EV that has always the offset with MTP_OV value. However, if programmed MTP_OV is unlike, the instruction "MTP select mode off" can be executed and then MEV will be EV + OV. Accordingly OV can be adjusted with instructions although MTP cell is programmed.

13.2. EEPROM Cell Structure

MTP (Multi Time Programmable) has been implemented on the S6B3301. The EEPROM stores the offset volume for V1OUT calibration after the device has been assembled and calibrated on a LCD module. For MTP programming, P_MTP pin is used. These pin should be available to on the module glass by ITO.

The MTP block of the S6B3301 consists of 7 bits. 1 bit is used for MTP mode protection bit (MPRT), and 6 bits are used for V1OUT calibration (MOV5~MOV0). MPRT can be read or written automatically in this LSI.

13.2.1. EEPROM block

MSB							LSB	
MPRT	MOV5	MOV4	MOV3	MOV2	MOV1	MOV0		

13.2.2. Description

MPRT : The Offset Volume(OV) can be written to EEPROM cells only when MPRT bit = '0'

MOV5~MOV0 : The MOV is used for calibrating the V1OUT voltage as an offset to the EV register value.

13.3. V1OUT Calibration flow

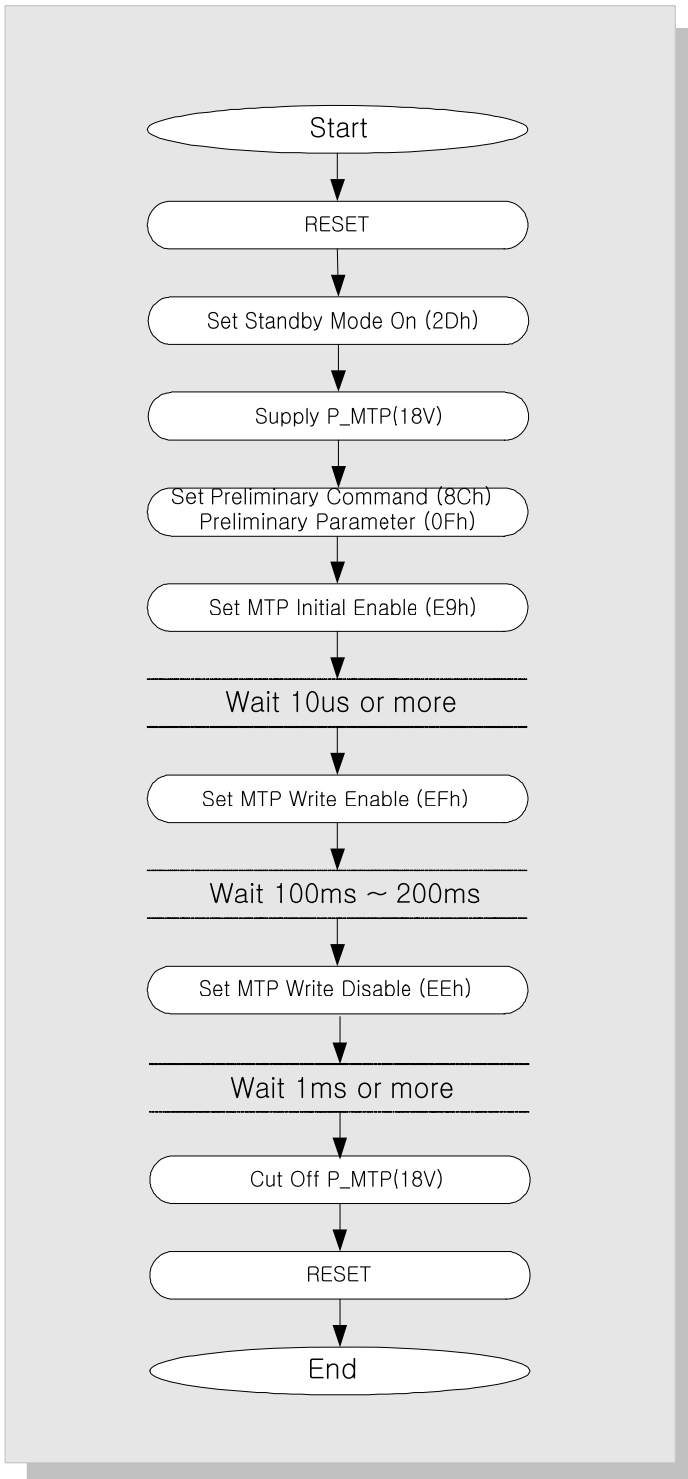
V1OUT may be calibrated with MTP in the following order.(ex : EV = 32, OV=-3)

STEP	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
1.											Execute MTP erase sequence.
2.											Apply external reset. (MTP data load)
3.	0	0	0	0	1	0	1	0	1	0	Set contrast control using instruction. (EV = 32)
	0	0	0	0	1	0	0	0	0	0	
4.	0	0	1	1	1	0	1	0	1	0	MTP select mode off by using the instruction.
5.	0	0	1	1	1	0	1	1	0	1	Set offset volume by using the instruction. (OV = -3)
	0	0	0	0	1	1	1	1	0	1	
6.											Repeat STEP 4. Until the end of the calibration.
7.	0	0	0	0	1	0	1	1	0	1	Standby on by using the instruction.
8.											Apply programming voltages for MTP programming. (P_MTP=18.0V±500mV) Wait 1ms or more.
9.	0	0	1	0	0	0	1	1	0	0	Preliminary Command.(8Ch)
	0	0	0	0	0	0	1	1	1	1	Preliminary parameter. (0Fh)
10.	0	0	1	1	1	0	1	1	1	1	Set MTP write enable. (Only available when MPRT= 0). Wait 100ms ~ 200ms.
11.	0	0	1	1	1	0	1	1	1	0	Set MTP write disable. Wait 1ms or more.
12.											Cut off programming voltages for MTP programming (P_MTP)
13.											Apply external reset.

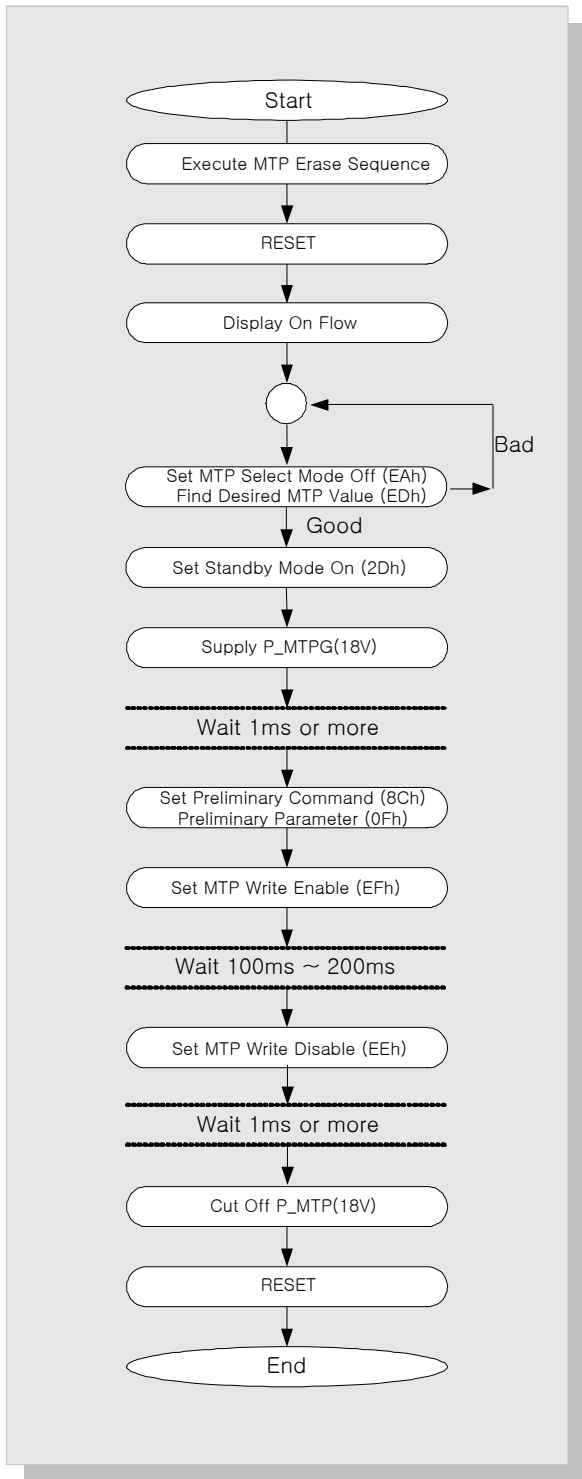
After the external reset, the calibrated data are automatically transferred to the 6-bit reference voltage control register.

*MTP_WRITING PROCESS is available when MPRT is zero (if MPRT = 1, MTP cell could not be programmed).

13.4. MTP Erase Sequence



13.5. MTP Write Sequence



13.5.1. Voltages and waveforms for MTP programming

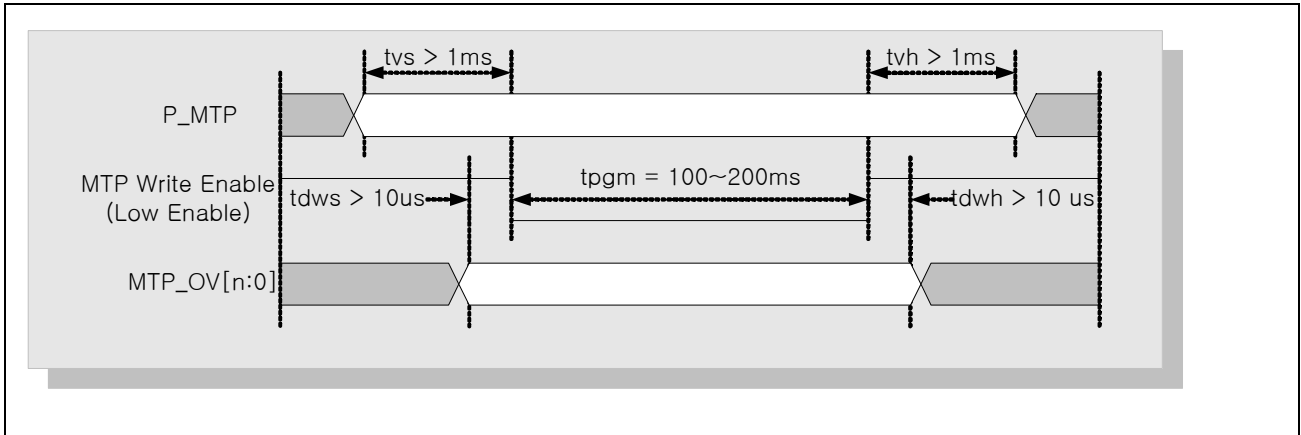


Figure 21. Voltages and waveforms for MTP programming

* Note: MTP_OV is offset volume.

13.5.2. Specific timings

Timing	Min	Max
Tvs	1ms	-
Tvh	1ms	-
Tdws	10us	-
Tdwh	10us	-
Tpgm	100ms	200ms

13.5.3. P_MTP Voltage Tolerance

Item	Pgm	Min	Typ	Max	Unit	Remarks
Tolerance of P_MTP	Erase		18		V	$\pm 500\text{ mV}$
	Write		18			

14. SYSTEM APPLICATION DIAGRAM

14.1. Internal Power Mode

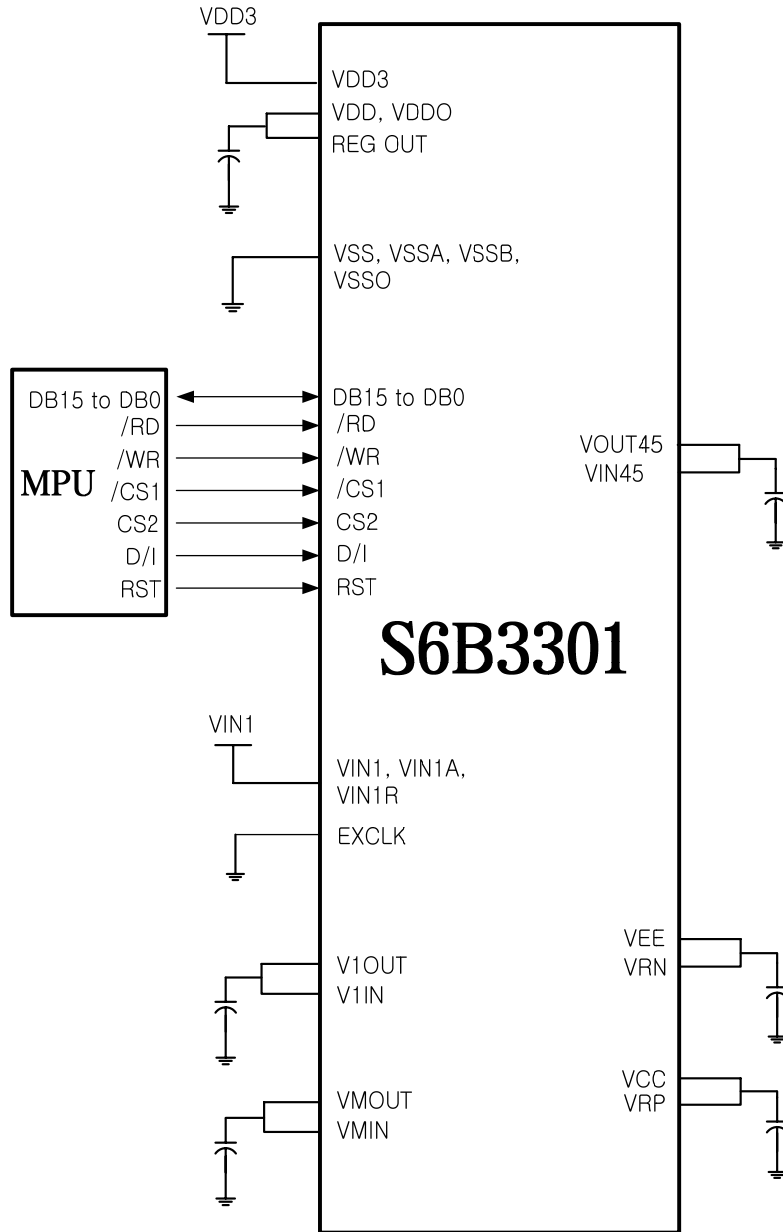


Figure 22. Application Circuit (80 Series MPU, Internal Power Mode)

14.2. External Power Mode

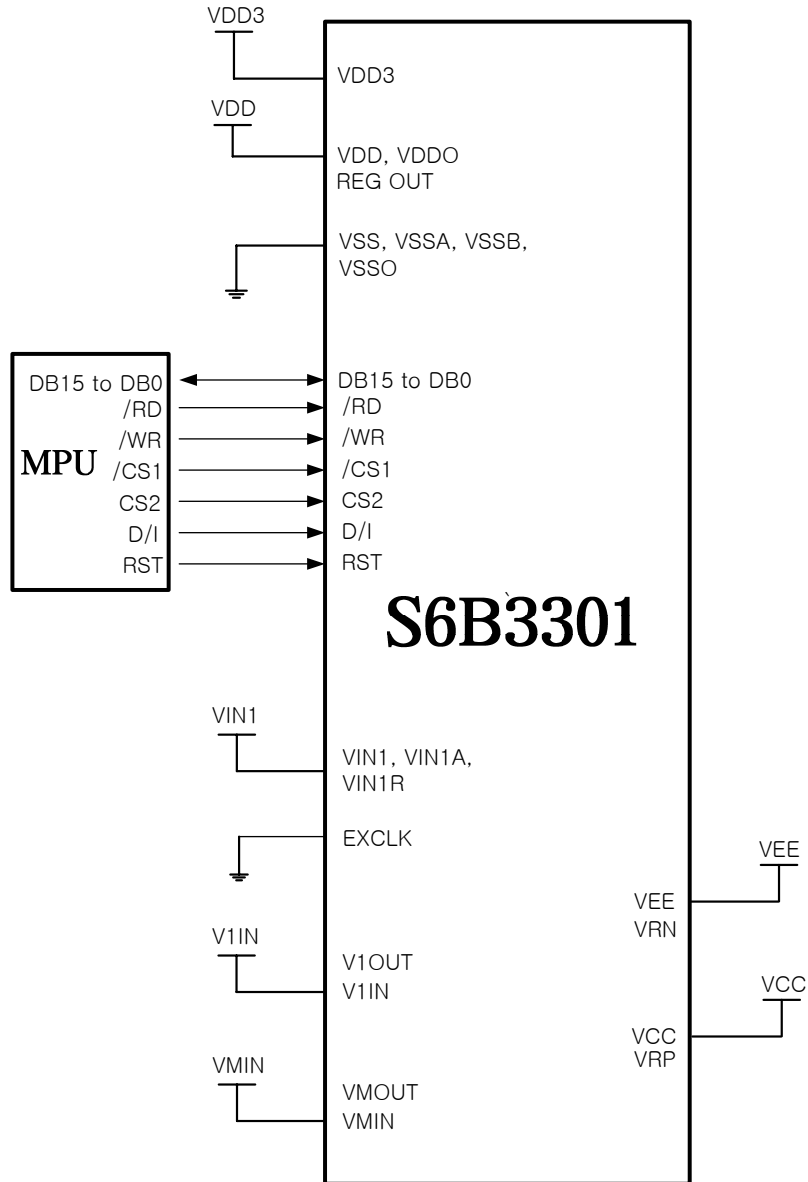


Figure 23. Application Circuit (80 Series MPU, External Power Mode)

14.3. External Component

Table 28. External Component

Name	Device	Value	Item	Maximum Rating Voltage of Capacitors
C1	Capacitors	1.0 μ F to 4.7 μ F	REG_OUT – GND	3V
C2	Capacitors	1.0 μ F	VOUT45 – GND–	10V
C3	Capacitors	1.0 μ F	Vm – GND	3V
C4	Capacitors	1.0 μ F	V1 – GND	10V
C5	Capacitors	1.0 μ F	VRP – GND	18V
C6	Capacitors	1.0 μ F	VRN – GND	18V

*1 Vforward = Max. 0.3V at 1mA
 Vreverse = Min. 15V