

HIGH-VOLTAGE MIXED-SIGNAL IC

UC1681

68 x 98RGB C-STN LCD Controller-Driver
w/ 32-Shade Modulation Engine, 13-bit per RGB
(Dither to 60,543 Colors with 16-bit 5R-6G-5B input)

MP Specifications
Revision 1.0

October 7, 2004

ULTRACHIP

The Coolest LCD Driver, Ever!!

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UC1681

*Single-Chip, Ultra-Low Power
68COM x 294SEG Matrix
Passive Color LCD Controller-Driver*

INTRODUCTION

UC1681 is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images, with well balanced gray shades and vivid colors.

In addition to low power COM and SEG drivers, UC1681 contains all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones and other battery operated palm top devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver for 68x98 matrix C-STN LCD with comprehensive support for input format and color depth:
 - 8-bit RGB: 256 color
 - 12-bit RGB: 4K color
 - 16-bit RGB: 60.5K color (dither)
 - 24-bit RGB: 465K color (dither)
- Support video rate CSTN applications.
- One software readable ID pin to support configurable vender identification.
- Partial scroll function and programmable data update window to support flexible manipulation of screen data.

- Support both row ordered and column ordered display buffer RAM access
- Support industry standard 3-wire, 4-wire serial bus (S9, S8, S8uc) and 8-bit/4-bit parallel bus (8080 or 6800).
- Special driver structure and gray shade modulation scheme. Ultra-low power consumption under all display patterns.
- No power consumption or image quality penalty when used with video rate CSTN
- Fully programmable Mux Rate, partial display window, Bias Ratio and Line Rate allow many flexible power management options.
- Software programmable four temperature compensation coefficients.
- Self-configuring 6x charge pump with on-chip pumping capacitors. Only 3 external capacitors are required to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Very low pin count (10 pins with S9) allows exceptional image quality in COG format on conventional ITO glass.
- Many on-chip and I/O pad layout features to support optimized COG applications.
- V_{DD} (digital) range: 1.8V ~ 3.3V
 V_{DD} (analog) range: 2.4V ~ 3.3V
LCD V_{OP} range: 4.8V ~ 11.8V
- OTP V_{LCD} trimming circuit to support precise LCD contrast matching
- Available in gold bump dies and COF:
 - Bump pitch: 41.5 μ M
 - Bump gap: 17.4 μ M
 - Bump surface: > 3,000 μ M²

ORDERING INFORMATION

GOLD BUMPED DIE

Part Number	OTP	Description
UC1681tGAB	Yes	Gold bumped die with OTP function.

General Notes**APPLICATION INFORMATION**

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of UltraChip's delivery. There is no post wafer saw/pack testing performed on individual die. Although the latest processes are utilized for wafer sawing and die pick-&-place into wafer pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their applications in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

OTP LIGHT SENSITIVITY

The OTP memory cell is sensitive to photon excitation. Under extended exposure to strong ambient light, the OTP cells can lose its content before the specified memory retention time span. The system designer is advised to provide proper light shields to realize full OTP content retention performance.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER

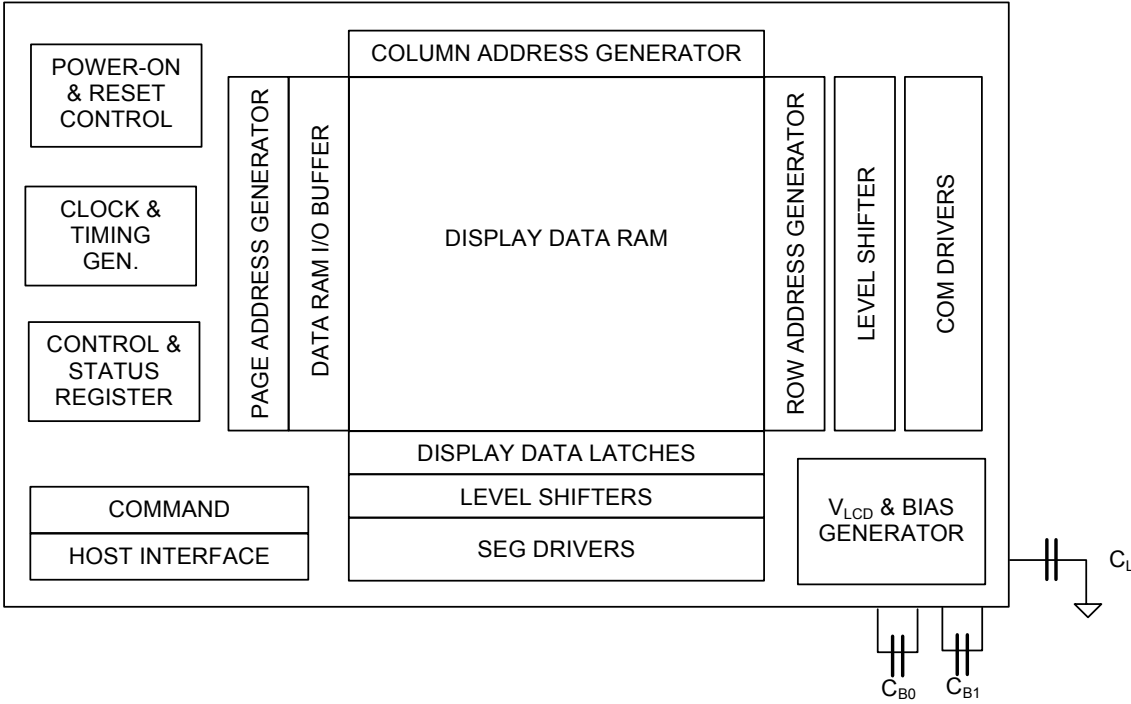
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BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	# Pads	Description
MAIN POWER SUPPLY			
V _{DD} V _{DD2} V _{DD3}	PWR	10 8 6	V _{DD2} /V _{DD3} is the analog power supply and it should be connected to the same power source. V _{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V _{DD2} /V _{DD3} . Please maintain the following relationship: $V_{DD} + 1.3V \geq V_{DD2/3} \geq V_{DD}$. Minimize the trace resistance for V _{DD} and V _{DD2} /V _{DD3} .
V _{SS} V _{SS2}	GND	12 8	Ground. Connect V _{SS} and V _{SS2} to the shared GND pin. Minimize the trace resistance for these two nodes.
LCD POWER SUPPLY & VOLTAGE CONTROL			
V _{B1+} V _{B1-} V _{B0+} V _{B0-}	PWR	9 9 9 9	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C _{BX} value between V _{BX+} and V _{BX-} . The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
V _{LCDIN} V _{LCDOUT}	PWR	2 2	High voltage LCD Power Supply. Connect these pins together. Capacitor C _L should be connected between V _{LCD} and V _{SS} . In COG applications, keep the ITO trace resistance between 50~80 Ω.

NOTE

- Recommended capacitor values:
C_B: 300 x LCD load capacitance or 2.2μF (2V), whichever is higher.
C_L: 15nF~50nF (16V) is appropriate for most applications.

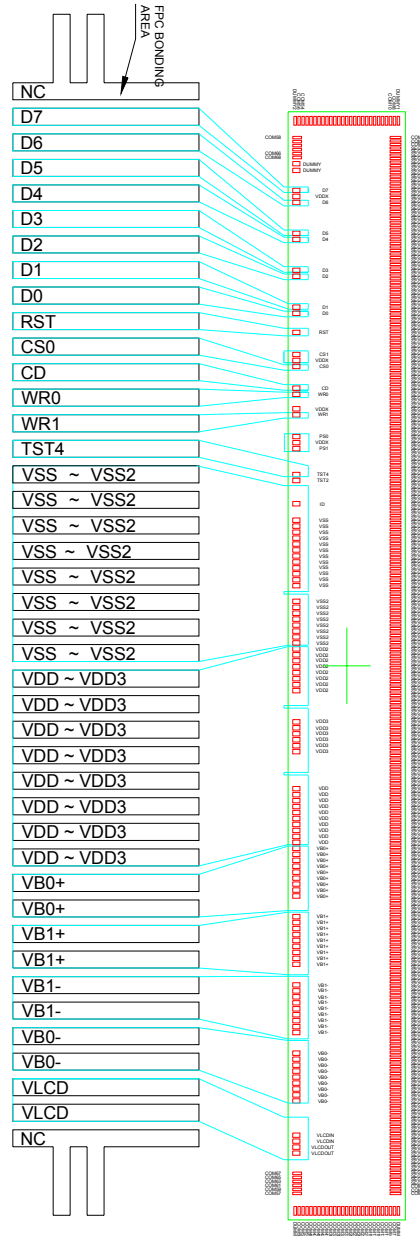
Name	Type	# Pads	Description																																													
HOST INTERFACE																																																
BM0 BM1	I	2	<p>Bus mode: The interface bus mode is determined by BM[1:0] and D[7:6] by the following relationship:</p> <table border="1"> <thead> <tr> <th>BM[1:0]</th> <th>D[7:6]</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>11</td> <td>Data</td> <td>6800/8-bit</td> </tr> <tr> <td>10</td> <td>Data</td> <td>8080/8-bit</td> </tr> <tr> <td>01</td> <td>00</td> <td>6800/4-bit</td> </tr> <tr> <td>00</td> <td>00</td> <td>8080/4-bit</td> </tr> <tr> <td>01</td> <td>10</td> <td>3-wire SPI w/ 9-bit token (S9: conventional)</td> </tr> <tr> <td>00</td> <td>10</td> <td>4-wire SPI w/ 8-bit token (S8: conventional)</td> </tr> <tr> <td>00</td> <td>11</td> <td>3/4-wire SPI w/ 8-bit token (S8uc: Ultra-Compact)</td> </tr> </tbody> </table>	BM[1:0]	D[7:6]	Mode	11	Data	6800/8-bit	10	Data	8080/8-bit	01	00	6800/4-bit	00	00	8080/4-bit	01	10	3-wire SPI w/ 9-bit token (S9: conventional)	00	10	4-wire SPI w/ 8-bit token (S8: conventional)	00	11	3/4-wire SPI w/ 8-bit token (S8uc: Ultra-Compact)																					
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CS0 CS1	I	2	Chip Select. Chip is selected when CS1="H" and CS0 = "L". When the chip is not selected, D[7:0] will be high impedance.																																													
RST	I	1	<p>When RST="L", all control registers are re-initialized by their default states. Since UC1681 has built-in Power-ON Reset and Software Reset command, so RST pin is not be required for most systems. However, if the V_{DD} On-Off behavior is not "clean", it is possible for UC1681's Power-ON reset to become confused.</p> <p>An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V_{DD}.</p>																																													
CD	I	1	<p>Select Control data or Display data for read/write operation. In S9 mode, CD pin is not used. Connect CD to V_{SS} when not used.</p> <p>"L": Control data "H": Display data</p>																																													
ID	I	1	<p>ID pin is for production control.</p> <p>The connection will affect the content of D[7] when using <i>Get Status</i> command. Connect to V_{DD} for "H" or V_{SS} for "L".</p>																																													
WR0 WR1	I	2	<p>WR[1:0] controls the read/write operation of the host interface. See Host Interface section for more detail.</p> <p>In parallel mode, WR[1:0] meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V_{SS}.</p>																																													
D0~D7	I/O	8	<p>Bi-directional bus for both serial and parallel host interfaces.</p> <p>In serial modes, connect D[0] to SCK, D[3] to SDA,</p> <table border="1"> <thead> <tr> <th></th> <th>BM=1x (Parallel)</th> <th>BM=0x (Parallel)</th> <th>BM=01 (S9)</th> <th>BM=00 (S8/S8uc)</th> </tr> </thead> <tbody> <tr> <td>D0</td> <td>D0</td> <td>D0/D4</td> <td>SCK</td> <td>SCK</td> </tr> <tr> <td>D1</td> <td>D1</td> <td>D1/D5</td> <td>–</td> <td>–</td> </tr> <tr> <td>D2</td> <td>D2</td> <td>D2/D6</td> <td>–</td> <td>–</td> </tr> <tr> <td>D3</td> <td>D3</td> <td>D3/D7</td> <td>SDA</td> <td>SDA</td> </tr> <tr> <td>D4</td> <td>D4</td> <td>–</td> <td>–</td> <td>–</td> </tr> <tr> <td>D5</td> <td>D5</td> <td>–</td> <td>–</td> <td>–</td> </tr> <tr> <td>D6</td> <td>D6</td> <td>–</td> <td>0</td> <td>S8/S8uc</td> </tr> <tr> <td>D7</td> <td>D7</td> <td>0</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>Connect unused pins to V_{DD} or V_{SS}.</p>		BM=1x (Parallel)	BM=0x (Parallel)	BM=01 (S9)	BM=00 (S8/S8uc)	D0	D0	D0/D4	SCK	SCK	D1	D1	D1/D5	–	–	D2	D2	D2/D6	–	–	D3	D3	D3/D7	SDA	SDA	D4	D4	–	–	–	D5	D5	–	–	–	D6	D6	–	0	S8/S8uc	D7	D7	0	1	1
	BM=1x (Parallel)	BM=0x (Parallel)	BM=01 (S9)	BM=00 (S8/S8uc)																																												
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D4	D4	–	–	–																																												
D5	D5	–	–	–																																												
D6	D6	–	0	S8/S8uc																																												
D7	D7	0	1	1																																												

Name	Type	# Pads	Description
HIGH VOLTAGE LCD DRIVER OUTPUT			
SEG1 ~ SEG294	HV	294	SEG (column) driver outputs. Support up to 98 x RGB pixels. Leave unused drivers open-circuit.
COM1 ~ COM68	HV	68	COM (row) driver outputs. Support up to 68 rows. When designing LCM, always start from COM1. If the LCM has N pixel rows and N is less than 68, set CEN to be $N-1$, and leave COM drivers [N+1 ~ 68] open-circuit.
MISC. PINS			
V _{DDX}	O	4	Auxiliary V _{DD} . These pins are connected to the main V _{DD} bus on chip. They are provided to facilitate chip configurations in COG and COF applications. These pins should not be used to provide V _{DD} power to the chip. It is not necessary to connect V _{DDX} to main V _{DD} externally.
TST4	I/HV	1	TST4 controls test mode and is also used to supply one of the high voltage required for OTP Program operation. Leave TST4 open during normal LCD operation. In COG applications keep TST4 trace resistance between 50 ~ 100 Ω.
TST2	I/O	1	Test I/O pins. Leave these pins open during normal LCD operation.

Note:

- Several control registers will specify "0 based index" for COM and SEG electrodes. In those situations, COM_X or SEG_X will correspond to index $X-1$, and the value ranges for those index registers will be 0~67 for COM and 0~293 for SEG.

REFERENCE COG LAYOUT



Notes for V_{DD} with COG:

The V_{DD}=1.65V, min. operation condition of UC1681, must be met under all operation conditions. To give UC1681 capability of supporting video, the peak of I_{DD} during high speed SRAM write can be 25~28mA, (depends on the bus speed and V_{DD}). Special care of V_{DD}, V_{DD2/3} ITO traces are recommended for COG applications where V_{DD} and V_{DD2/3} are separated. High resistance on V_{DD} trace can cause actual on-chip V_{DD} to drop below V_{DD}=1.65V during high speed data write condition and cause the IC to malfunction. Therefore, V_{DD}, V_{DD2/3} ITO traces need to be very carefully designed for COG modules where V_{DD} and V_{DD2/3} use separate power supplies.

CONTROL REGISTERS

UC1681 contains registers which control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meanings and default values. The commands supported by UC1681 will be described in the next two sections, starting with a summary table, followed by detailed descriptions.

Name: The Symbolic reference of the register.
 Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after *Power-Up-Reset* and *System-Reset*.

Name	Bits	Default	Description
SL	7	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (67– 2x(FLT+FLB)). Setting SL outside of this range causes undefined effect on the displayed image.
FLT FLB	4 4	0H 0H	Fixed Lines. The first FLTx2 lines and the last FLBx2 lines (relative to CEN) of each frame are fixed and are not affected by scrolling (SL). When FLT and/or FLB are non-zero, the screen is effectively separated into three regions: one scrollable, surrounded by two non-scrollable regions. When partial display mode is activated, the display of these 2xFLT and 2xFLB lines is also controlled by LC[0]. When LC[0]=1, the display will have three sections, 2xFLT on one side non-scrollable, 2XFLB on the other side also non-scrollable, and scrollable DST~DEN in the middle.
CR	7	0H	Return Column Address. Useful for cursor implementation.
CA	7	0H	Display Data RAM Column Address (counted in RGB triplet) (Used in Host to Display Data RAM access)
RA	7	0H	Display Data RAM Row Address (Used in Host to Display Data RAM access)
BR	2	2H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS} . 00b: 5 01b: 7 10b: 8 11b: 9
TC	2	0H	Temperature Compensation (per °C) 00b: -0.05% 01b: -0.10% 10b: -0.15% 11b: -0.20%
PM	8	6CH	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
PMO	8	00H	PM offset. The effective PM value $PMV = PM \pm PMO$. \pm is determined by the sign: PMO[5]. Make sure PMV formula does not overflow or underflow. PMO[7:6] are for UltraChip use only. Do <u>NOT</u> overwrite PMO[7:6].
OM	2	–	Operating Modes (Read only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
ID	1	PIN	Access the connected status of ID pin.
RS	1	–	Reset in progress. Host Interface not ready

Name	Bits	Default	Description
PC	4	DH	Power Control. PC[1:0]: Panel Loading 00b: LCD: $\leq 7nF$ 01b: LCD: 7~9nF 10b: LCD: 9~12nF 11b: LCD: 12~16nF PC[3:2]: Pump Control 00b: External V_{LCD} 11b: Internal V_{LCD} (Standard)
DC	5	18H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default 0: OFF) DC[1]: APO: All Pixels ON (Default 0: OFF) DC[2]: Display ON/OFF (Default 0: OFF) DC[3]: Gray-shade Modulation mode. 0: 8-shade mode 1: 32-shade Mode DC[4]: Dither Function Control. 0: Disable Dither Function 1: Enable Dither Function
AC	5	1H	Address Control: AC[0]: WA: Automatic column/row Wrap Around (Default 1: ON) AC[1]: Auto-Increment order 0: Column (CA) first 1: Row (RA) first AC[2]: RID: RA (row address) auto increment direction (L:+1 H:-1) AC[3]: CUM: Cursor update mode, (Default 0: OFF) when CUM=1, CA increment on write only, wrap around suspended AC[4]: Window Program Enable 0: Disable 1: Enable
MSK	3	0H	R/G/B Write Data mask bits MSK[2:0] = {MR, MG, MB} (Default: 000b) 0: Write 1: Block
WPC0	8	00H	Window program starting column address. Value range: 0 ~ 97.
WPP0	8	00H	Window program starting row address. Value range: 0 ~ 67.
WPC1	8	61H	Window program ending column address. Value range: 0 ~ 97.
WPP1	8	43H	Window program ending row address. Value range: 0 ~ 67.
CEN	7	43H	COM scanning end (last COM with full line cycle, 0 based index)
DST	7	00H	Partial display start (first COM with active scan pulse, 0 based index)
DEN	7	43H	Partial display end (last COM with active scan pulse, 0 based index)
			Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN \geq DEN \geq DST + 9

Name	Bits	Default	Description
LC	10	088H	<p>LCD Control:</p> <p>LC[0]: Enable the first FLx2 lines in partial display mode (Default OFF).</p> <p>LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: OFF)</p> <p>LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: OFF)</p> <p>LC[4:3]: Line Rate (Klps: Kilo-Line-per-second)</p> <p>00b: 14.0 Klps 01b: 16.1 Klps</p> <p>10b: 18.4 Klps 11b: 21.0 Klps</p> <p>(Frame-Rate = Line-Rate / Mux-Rate)</p> <p>LC[5] : RGB filter order (as mapped to SEG1, SEG2, SEG3)</p> <p>0 : BGR-BGR 1 : RGB-RGB</p> <p>LC[7:6] : Color and input mode</p> <p>when DC[4]=1:</p> <p>00b : 256 color mode. 3R-3G-2B (8-bit/RGB)</p> <p>01b : 4K color mode. 4R-4G-4B (12-bit/RGB)</p> <p>10b : 60.5K color mode. 5R-6G-5B (16-bit/RGB)</p> <p>11b : 465K color mode. 6R-7G-6B (24-bit/RGB)</p> <p>when DC[4]=0:</p> <p>00b : 256 color mode. 3R-3G-2B (8-bit/RGB)</p> <p>01b : 4K color mode. 4R-5G-3B (12-bit/RGB)</p> <p>10b : 8K color mode. 4R-5G-4B (16-bit/RGB)</p> <p>11b : 8K color mode. 4R-5G-4B (24-bit/RGB)</p> <p>For data over 4R-5G-4B, the redundant LSB of each color will be truncated. For example: R0, G0, and B0 will be truncated for</p> <p style="text-align: center;">R4 R3 R2 R1 <u>R0</u> - G5 G4 G3 G2 G1 <u>G0</u> - B4 B3 B2 B1 <u>B0</u>.</p> <p>LC[9:8] : Partial Display Control</p> <p>0xb: Disable Mux-Rate = CEN+1 (DST, DEN not used)</p> <p>10b: Enabled Mux-Rate = CEN+1</p> <p>11b: Enabled Mux-Rate = DEN-DST+1+LC[0]x(FLT+FLB)x2</p>
APC0	5	6DH	Advanced Program Control. For UltraChip only. Please do not use.
APC1	8	3EH	
OD	1	–	OTP option flag: Always 1 (With OTP)
OS	1	–	OTP programming in-progress
WS	1	–	OTP Operation Succeeded
OTPC	6	10H	<p>OTP Programming Control:</p> <p>OTPC[2:0] : OTP command</p> <p>000 : Sleep 001 : Read</p> <p>010 : Erase 011 : Program</p> <p>1XX : For UltraChip debug use only</p> <p>OTPC[3] : OTP Enable (automatically cleared after each OTP command)</p> <p>OTPC[4] : Use/ignore OTP value. 0: Ignore 1: Normal</p> <p>OTPC[5] : For testing only. Set to 0 for normal operation.</p>
OTPM	8	00H	<p>OTP Write Mask. Bit =1: program, Bit=0: no action.</p> <p>PM[7:6] are reserved for UltraChip use only. Do <i>NOT</i> overwrite OTP[7:6].</p>

COMMAND TABLE

The following is a list of host commands supported by UC1681

C/D: 0: Control, 1: Data
 W/R: 0: Write Cycle, 1: Read Cycle
 #: Useful Data bits -: Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status & PM	0	1	ID PM7	MX PM6	MY PM5	WA PM4	DE PM3	WS PM2	OD PM1	OS PM0	Get Status	N/A
				PMO[7:6]			PMO[5:0]						
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	-	#	#	#	Set CA[6:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0
6	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	1
7	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b
8	Set Adv. Program Control (double byte command)	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0], R = 0, or 1	N/A
		0	0	#	#	#	#	#	#	#	#		
9	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	-	#	#	#	Set SL[6:4]	0
10	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0
	Set Row Address MSB	0	0	0	1	1	1	-	#	#	#	Set RA[6:4]	0
11	Set V _{BIAS} Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	6CH
		0	0	#	#	#	#	#	#	#	#		
12	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[9:8]	0: Disable
13	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set {FLT,FLB}	0
		0	0	#	#	#	#	#	#	#	#		
15	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	01b
16	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
17	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
18	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	100b
19	Set Color Mask	0	0	1	0	1	1	0	#	#	#	Set MSK[2:0]	0
20	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	0
21	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0 (BGR)
22	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b
23	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
24	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
25	Set Test Control (double byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
26	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	10b: 8
27	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	AC[3]=0
28	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	AC[3]=1
29	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	67
		0	0	-	#	#	#	#	#	#	#		
30	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
		0	0	-	#	#	#	#	#	#	#		
31	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	67
		0	0	-	#	#	#	#	#	#	#		
32	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Set WPC0[7:0]	0
		0	0	#	#	#	#	#	#	#	#		
33	Set Window Programming Starting Row Address	0	0	1	1	1	1	0	1	0	1	Set WPP0[7:0]	0
		0	0	#	#	#	#	#	#	#	#		
34	Set Window Programming Ending Column Address	0	0	1	1	1	1	0	1	1	0	Set WPC1[7:0]	97
		0	0	#	#	#	#	#	#	#	#		
35	Set Window Programming Ending Row Address	0	0	1	1	1	1	0	1	1	1	Set WPP1[7:0]	67
		0	0	#	#	#	#	#	#	#	#		
36	Enable window program	0	0	1	1	1	1	1	0	0	#	Set AC[4]	0: Disable

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
37	Set OTP Operation control	0 0	0 0	1 -	0 -	1 #	1 #	1 #	0 #	0 #	0 #	Set OTPC[5:0]	0
38	Set OTP Write Mask	0 0	0 0	1 #	0 #	1 #	1 #	1 #	0 #	0 #	1 #	Set OTPM[7:0]	0
39	Set V_{OTP1} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with Window Programming commands	N/A
40	Set V_{OTP2} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #		
41	Set OTP Write Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #		
42	Set OTP Read Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		

Notes:

- Other than commands listed above, all other bit patterns may result in undefined behavior.
- The interpretation of commands 38~42 depends on register OTPC[3].
- Command 39~42 are shared with command 32~35, and they have exactly the same code. When OTPC[3]=0, command 39~42 are interpreted as *Window Programming* commands. When OTPC[3]=1, they are *OTP Control* commands.
- OTPM and PM are actually the same register. Only one of the command (38 or 11) is valid at any time, and it is determined by OTPC[3].
- After OTP-ERASE or OTP-PROGRAM operation, please always perform the following steps,
 - a) disconnect TST4 power source
 - b) Do a full V_{DD} ON-OFF cycle (make sure V_{DD} drops below 50mV).
 before resuming normal operation.

COMMAND DESCRIPTION

(1) Write Data To Display Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8bits data write to SRAM							

UC1681 will convert input RAM data to 13-bits of RGB data. Please refer to command (22) *Set Color Mode* for detail of data-write sequence.

(2) Read Data From Display Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8bits data from SRAM							

Each RGB triplet is stored as 13-bit in the display RAM. Each 13-bits RGB data takes 2 RAM read cycles. The data read will start with the high byte [D[12:5] and then low byte [D[4:0], 4'b000]. The read out RGB data is *after-dither* for 60.5K color and 465K color mode and *after-extension* for 256 color mode.

R3	R2	R1	R0	G4	G3	G2	G1	G0	B3	B2	B1	B0	0	0	0
1st Read								2nd Read							

Write/Read Data Byte (command 1/2) operation uses internal Row Address register (RA) and Column Address register (CA). RA and CA can be programmed by issuing *Set Row Address* and *Set Column Address* commands. If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the CA boundary, and system programmers need to set the values of RA and CA manually. If WA is ON (1), when CA reaches end of column address, CA will be reset to 0 and RA will be increased or decreased, depending on the setting of Row Increment Direction (RID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 67), RA will be wrapped around to the other end of RAM and continue.

(3) Get Status & PM

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	ID	MX	MY	WA	DE	WS	OD	OS
			PM[7:0]							
			PMO[7:0]							

Status flag definitions:

- ID: Provide access to ID pin connection status.
- MX: Status of register LC[1], mirror X.
- MY: Status of register LC[2], mirror Y.
- WA: Status of register AC[0]. Automatic column/row wrap around.
- DE: Display enable flag. DE=1 when display is enabled
- WS: OTP Operation succeeded
- OD: OTP Option (Yes for OTP version, no for non-OTP version)
- OS: OTP action status.

PMO[7:0]: OTP cell's value.

If multiple *Get Status* commands are issued consecutively within one single CD 1=>0=>1 transaction, the *Get Status* command will return {Status, PM, PMO, Status, PM, PMO, Status, PM, PMO, ...} alternating.

(4) Set Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	0	0	0	0	CA3	CA2	CA1	CA0
Set Column Address MSB CA[6:4]	0	0	0	0	0	1	-	CA6	CA5	CA4

Set SRAM column address for read/write access. CA is counted in RGB triplets, not individual SEG electrode.

CA value range: **0~97**

(5) Set Temperature Compensation

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	0	0	1	0	0	1	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:

00b = -0.05%/°C **01b** = -0.10%/°C **10b** = -0.15%/°C **11b** = -0.20%/°C

(6) Set Panel Loading

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	0	0	1	0	1	0	PC1	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

Panel loading definition: **00b** : ≤ 7nF **01b** = 7~9nF **10b** = 9~12nF **11b** = 12~16nF

(7) Set Pump Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[3:2]	0	0	0	0	1	0	1	1	PC3	PC2

Set PC[3:2] to program the build-in charge pump stages.

Pump control definition:

00b = External V_{LCD} **11b** = Internal V_{LCD}

(8) Set Advanced Program Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Adv. Program Control APC[0] (Double byte command)	0	0	0	0	1	1	0	0	0	R
	0	0	APC register parameter							

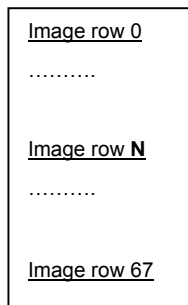
For UltraChip only. Please do NOT use.

(9) Set Scroll Line

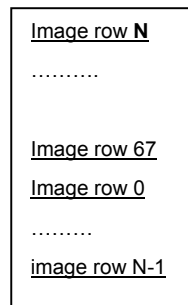
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	0	1	0	0	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[6:4]	0	0	0	1	0	1	-	SL6	SL5	SL4

Set the scroll line number.

Scroll line setting will scroll the displayed image up by SL rows. FLT and FLB are the register values programmed by *Set Fixed Lines* command.



SL=0



SL=N

(10) Set Row Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Row Address LSB RA [3:0]	0	0	0	1	1	0	RA3	RA2	RA1	RA0
Set Row Address MSB RA [6:4]	0	0	0	1	1	1	-	RA6	RA5	RA4

Set SRAM row address for read/write access.

Possible value = **0-67**

(11) Set V_{BIAS} Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V _{BIAS} Potentiometer. PM [7:0] (Double byte command)	0	0	1	0	0	0	0	0	0	1
	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range: **0 ~ 255**

(12) Set Partial Display Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [9:8]	0	0	1	0	0	0	0	1	LC9	LC8

This command is used to enable partial display function.

LC[9:8] : **0Xb**: Disable Partial Display, Mux-Rate = CEN+1 (DST, DEN not used.)

10b: Enable Partial Display, Mux-Rate = CEN+1

11b: Enable Partial Display, Mux-Rate = DEN-DST+1+ LC[0]x(FLT+FLB)x2

(13) Set RAM Address Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	1	0	0	0	1	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/row wrap around.

0: CA or RA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary

1: CA or RA (depends on AC[1]= 0 or 1) will restart, and RA or CA will increment by one step.

AC[1]: Auto-Increment order

0 : column (CA) increment (+1) first until CA reaches CA boundary, then RA will increment by (+/-1).

1 : row (RA) increment (+/-1) first until RA reach RA boundary, then CA will increment by (+1).

AC[2]: RID, row address (RA) auto increment direction (0/1 = +/- 1)

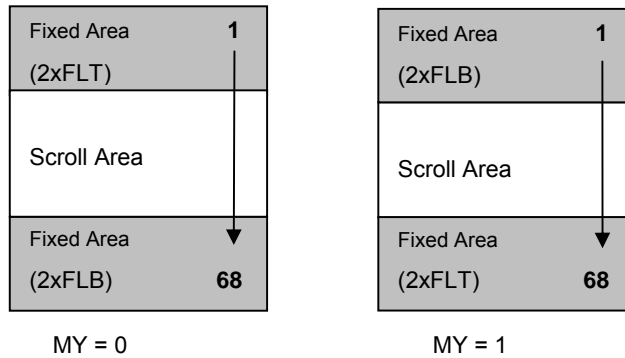
When WA=1 and CA reaches CA boundary, RID controls whether row address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and RA. When Window Program is enabled (AC[4]=ON), see command description (32) ~ (36) for more details. If WPC[1:0] and WPP[1:0] values are the default values, the behavior of CA, RA auto-increment will be the same, no matter what the setting of AC[4] is.

(14) Set Fixed Lines

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines {FLT,FLB} (Double byte command)	0	0	1	0	0	1	0	0	0	0
	0	0	FLT[3:0]				FLB[3:0]			

The fixed line function is used to implement the partial scroll function by dividing the screen into Scroll and Fixed areas. Set Fixed Lines command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFLT rows and bottom 2xFLB for mirror Y (MY) is 0, or covers the top 2xFLB rows and bottom 2xFLT rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.



When partial display mode is activated, the display of these 2x(FLT+FLB) lines is also controlled by LC[0]. Before turning on LC[0], please make sure

MY=0 $DST \geq FLT \times 2$
 $DEN \leq (CEN - FLB \times 2)$.

MY=1 $DST \geq FLB \times 2$
 $DEN \leq (CEN - FLT \times 2)$

(15) Set Line Rate

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	1	0	1	0	0	0	LC4	LC3

Program LC [4:3] for line rate setting (Frame-Rate = Line-Rate / Mux-Rate). The line rate is automatically scaled down by 1/2 and 1/3 at Mux-Rate = 28 and 16.

The following are line rates at Mux Rate = 29 ~ 68.

00b: 14.0 Klps **01b: 16.1 Klps** 10b: 18.4 Klps 11b: 21.0 Klps
(Klps: Kilo-Line-per-second)

(16) Set All Pixel ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	1	0	1	0	0	1	0	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(17) Set Inverse Display

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	1	0	1	0	0	1	1	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

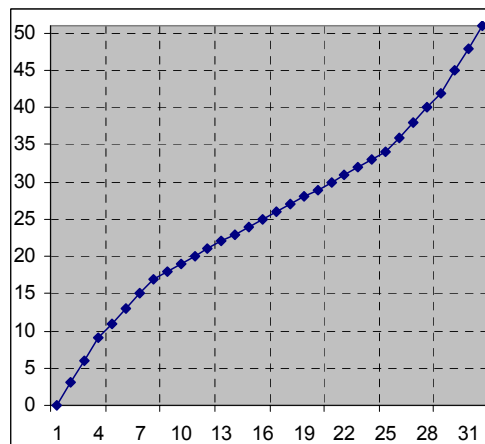
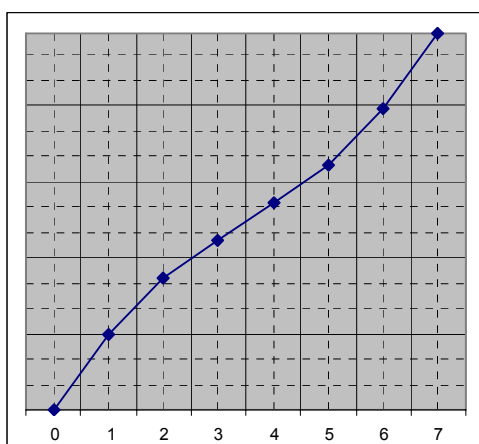
(18) Set Display Enable

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [4:2]	0	0	1	0	1	0	1	DC4	DC3	DC2

This command is for programming register DC[4:2].

When DC[2] is set to 0, the IC will put itself into Sleep mode. All drivers, voltage generation circuit and timing circuit will be halted to conserve power. When DC[2] is set to 1, UC1681 will first exit from Sleep mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

DC[3] controls the gray shade modulation modes. UC1681 has two gray shade modulation modes: an 8-shade mode and a 32-shade mode. The modulation curves are shown below. Horizontal axes are the gray shade data. The vertical axes are the ON-OFF ratio.



DC[4] enables dither function. Refer to (22) *Set Color Mode* for more information.

0b: Dither Disable **1b: Dither Enable**

(19) Set Color Mask

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Mask MSK [2:0]	0	0	1	0	1	1	0	MSK[2:0]		

This command is used for program MSK[2:0] which will control whether the input RGB data will be blocked from updating RGB data in the RAM. (1: Block, 0: Normal. MSK[2:0] = {MSK_R, MSK_G, MSK_B})

Example: Let color mode = 256 color, MSK[2:0] = 100b (MSK_R = 1, MSK_G = 0, MSK_B = 0). There is one pixel to be updated, and the original data for the pixel is 11100110b (RRR-GGG-BB). Suppose the new input RGB data is 00000000b, since R is masked, the data for the pixel would be updated as 11100000b.

(20) Set LCD Mapping Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	1	1	0	0	0	MY	MX	LC0

This command is used for program LC[2:0] for COM (row) mirror (MY), SEG (column) mirror (MX).

LC[2] controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

LC[1] controls Mirror X (MX): MX is implemented by selecting the CA or 97-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

LC[0] controls whether the two soft icon sections (2xFLT on the top and 2xFLB on the bottom) is displayed during partial display mode or not.

(21) Set Color Pattern

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Pattern LC [5]	0	0	1	1	0	1	0	0	0	LC5

UC1681 supports on-chip swapping of R↔B data mapping to the SEG drivers.

LC[5]	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	...	SEG304	SEG293	SEG294
0	B	G	R	B	G	R	...	B	G	R
1	R	G	B	R	G	B	...	R	G	B

The definition of R/G/B input data is determined by LC[7:6], as described in *Set Color Mode* below.

(22) Set Input Color Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Mode LC [7:6]	0	0	1	1	0	1	0	1	LC7	LC6

Program color mode and RGB input pattern. Color mode (LC[7:6]) definition:

Dither Option ON (DC[4]=1):

LC[7:6] = 00b (RRR-GGG-BB, 256 color)

One byte of input data is extended and stored to 13 RAM bits. No dither is performed.

Data Write Sequence	D[7:0]
1 st Byte Write Data	R2 R1 R0 G2 G1 G0 B1 B0

LC[7:6] = 01b (RRRR-GGGG-BBBB, 4K color)

1-bit extension for G. 12 bits of input data is stored to 13 RAM bits.

3 bytes of input data will be merged into 2 sets of RGB data. No dither is performed.

Data Write Sequence	D[7:0]
1 st Byte Write Data	R3 R2 R1 R0 G3 G2 G1 G0
2 nd Byte Write Data	B3 B2 B1 B0 R3 R2 R1 R0
3 rd Byte Write Data	G3 G2 G1 G0 B3 B2 B1 B0

LC[7:6] = 10b (RRRRR-GGGGG-BBBBB, 60.5K color)

1-bit dither for R/G/B each. 16 bits input data dithered to 13 RAM bits.

Data Write Sequence	D[7:0]
1 st Byte Write Data	R4 R3 R2 R1 R0 G5 G4 G3
2 nd Byte Write Data	G2 G1 G0 B4 B3 B2 B1 B0

LC[7:6] = 11b (RRRRRRXX-GGGGGGX-BBBBBBXX, 465K color)

2-bit dither per color. 19 out of 24 bits input data is dithered to 13 RAM bits.

Data Write Sequence	D[7:0]
1 st Byte Write Data	R5 R4 R3 R2 R1 R0 -- --
2 nd Byte Write Data	G6 G5 G4 G3 G2 G1 G0 --
3 rd Byte Write Data	B5 B4 B3 B2 B1 B0 -- --

Data Read Sequence

for LC[7:6] = 0.

Data Read Sequence	D[7:0]
1 st Byte Read Data	R2 R1 R0 R _M G2 G1 G0 G _{M2}
2 nd Byte Read Data	G _{M1} B1 B0 B _{M1} B _{M0} 0 0 0

for LC[7:6] = 1.

Data Read Sequence	D[7:0]
1 st Byte Read Data	R3 R2 R1 R0 G3 G2 G1 G0
2 nd Byte Read Data	G _{M3} B3 B2 B1 B0 0 0 0

R/G/B: the input Red/Green/Blue data.

R/G_{MN}: the Red/Green bits mapped from RGB input data.

for LC[7:6] = 2, 3.

Data Read Sequence	D[7:0]
1 st Byte Read Data	R _{D3} R _{D2} R _{D1} R _{D0} G _{D4} G _{D3} G _{D2} G _{D1}
2 nd Byte Read Data	G _{D0} B _{D3} B _{D2} B _{D1} B _{D0} 0 0 0

R/G/B_{DN} : the N-th bit of after-dither Red/Green/Blue input data.

Dither Option Off (DC[4]=0):

LC[7:6] = 00b (RRR-GGG-BB, 256 color)

One byte of input data is extended and stored to 13 RAM bits.

Data Write Sequence	D[7:0]
1 st Byte Write Data	R2 R1 R0 G2 G1 G0 B1 B0

LC[7:6] = 01b (RRRR-GGGGG-BBB, 4K color)

12 bits of input data is stored to 13 RAM bits. 3 bytes of input data will be merged into 2 sets of RGB data.

Data Write Sequence	D[7:0]
1 st Byte Write Data	R3 R2 R1 R0 G4 G3 G2 G1
2 nd Byte Write Data	G0 B2 B1 B0 R3 R2 R1 R0
3 rd Byte Write Data	G4 G3 G2 G1 G0 B2 B1 B0

LC[7:6] = 10b (RRRRX-GGGGX-BBBBX, 8K color)

1-bit truncation each for R/G/B. 16 bits input data truncated to 13 RAM bits.

Data Write Sequence	D[7:0]
1 st Byte Write Data	R4 R3 R2 R1 -- G5 G4 G3
2 nd Byte Write Data	G2 G1 -- B4 B3 B2 B1 --

LC[7:6] = 11b (RRRRXXX-GGGGXXX-BBBBXXX, 8K color)

2-bit truncation for per color. 18 out of 24 bits input data is truncated to 13 RAM bits.

Data Write Sequence	D[7:0]
1 st Byte Write Data	R3 R2 R1 R0 -- -- -- --
2 nd Byte Write Data	G4 G3 G2 G1 G0 -- -- --
3 rd Byte Write Data	B3 B2 B1 B0 -- -- -- --

Data Read Sequence

for LC[7:6] = 0, read data sequence is same as Dither Enabled mode.

for LC[7:6] = 1.

Data Read Sequence	D[7:0]
1 st Byte Read Data	R3 R2 R1 R0 G4 G3 G2 G1
2 nd Byte Read Data	G0 B2 B1 B0 B _{M2} 0 0 0

R/G/B: the input Red/Green/Blue data.

R/G_{MN}: the Red/Green bits mapped from RGB input data.

for LC[7:6] = 2, 3.

Data Read Sequence	D[7:0]
1 st Byte Read Data	R _{T3} R _{T2} R _{T1} R _{T0} G _{T4} G _{T3} G _{T2} G _{T1}
2 nd Byte Read Data	G _{T0} B _{T3} B _{T2} B _{T1} B _{T0} 0 0 0

R/G/B_{TN} : the N-th bit of after-truncated Red/Green/Blue input data.

(23) System Reset

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	1	1	1	0	0	0	1	0

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(24) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	1	1	1	0	0	0	1	1

This command is used for "no operation".

(25) Set Test Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT (Double byte command)	0	0	1	1	1	0	0	1	TT	
	0	0	Testing parameter							

This command is used for UltraChip production testing. Please do not use.

(26) Set LCD Bias Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	1	1	1	0	1	0	BR1	BR0

Bias ratio definition:

00b = 5

01b = 7

10b = 8

11b = 9

(27) Reset Cursor Update Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Reset Cursor Update Mode AC[3]=0 CA=CR	0	0	1	1	1	0	1	1	1	0

This command is used to reset cursor update mode function.

(28) Set Cursor Update Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC[3]=1 CR=CA	0	0	1	1	1	0	1	1	1	1

This command is used for set cursor update mode function. When cursor update mode is set, UC1681 will update register CR with the value of register CA. The column address CA will increment with write RAM data operation but the address wraps around will be suspended no matter what WA setting is. However, the column address will not increment in read RAM data operation.

The set cursor update mode can be used to implement "write after read RAM" function. The column address (CA) will be restored to the value, which is before the set cursor update mode command, when resetting cursor update mode.

The purpose of this pair of commands and their features is to support "write after read" function for cursor implementation.

(29) Set COM End

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN (Double byte command)	0	0	1	1	1	1	0	0	0	1
	0	0	CEN register parameter							

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD. When the LCD has less than 68 pixel rows, the LCM designer should set CEN to $N-1$ (where N is the number of pixel rows) and use COM1 through COM- N as COM driver electrodes.

(30) Set Partial Display Start

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST (Double byte command)	0	0	1	1	1	1	0	0	1	0
	0	0	DST register parameter							

This command programs the starting COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

(31) Set Partial Display End

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN (Double byte command)	0	0	1	1	1	1	0	0	1	1
			<i>DEN</i> register parameter							

This command programs the ending COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

CEN, DST, and DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[9]=1, two partial display modes are possible with UC1681:

LC[8]=1: ON-OFF only, ultra-low-power mode (if Mux-Rate ≤ 30, set BR=5).

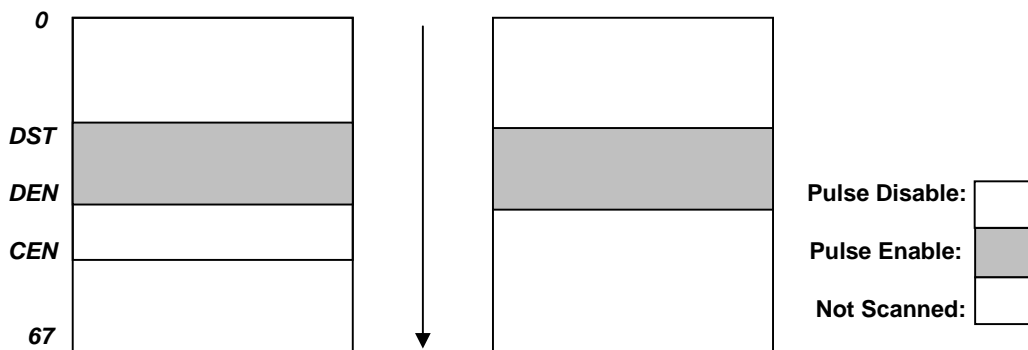
LC[8]=0: Full gray shade low power mode (BR and PM stays the same)

When LC[9:8]=10b, the Mux-Rate is still CEN+1. This is achieved by suppressing only the scanning pulses, but not the scanning time slots for COM electrodes that are outside of DST~DEN. Under this mode, the gray-scale quality of the display is preserved, while the power is reduced significantly.

When LC[9:8]=11b, the Mux-Rate is narrowed down to DST-DEN + LC[0]x(FLT+FLB)x2. When MUX rate is reduced, reduce the line rate accordingly to reduce power. Changing MUX rate also require BR and V_{LCD} to be readjusted. When Mux-Rate is under 30, it is recommend to set BR=5.

For minimum power consumption, set LC[9:8]=11b, set (DST, DEN, FLT, FLB, CEN) to minimize MUX rate, use slowest line rate which satisfies the flicker requirement, use 8-gray-shade mode, set PC[1:0]=00b, and use lowest BR, lowest V_{LCD} which satisfies the contrast requirement.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



(32) Set Window Program Starting Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0 (Double byte command)	0	0	1	1	1	1	0	1	0	0
			<i>WPC0[7:0]</i> register parameter							

This command is to program the starting column address of RAM program window.

(33) Set Window Program Starting Row Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0 (Double byte command)	0	0	1	1	1	1	0	1	0	1
<i>WPP0</i> register parameter										

This command is to program the starting row address of RAM program window.

(34) Set Window Program Ending Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 (Double byte command)	0	0	1	1	1	1	0	1	1	0
<i>WPC1[7:0]</i> register parameter										

This command is to program the ending column address of RAM program window.

(35) Set Window Program Ending Row Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1 (Double byte command)	0	0	1	1	1	1	0	1	1	1
<i>WPP1</i> register parameter										

This command is to program the ending row address of RAM program window.

(36) Set Window Program Enable

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[4]	0	0	1	1	1	1	1	0	0	AC4

This command is to enable the Window Program Function. Window Program Enable should always be reset when changing the window program boundary and then set right before starting the new boundary program.

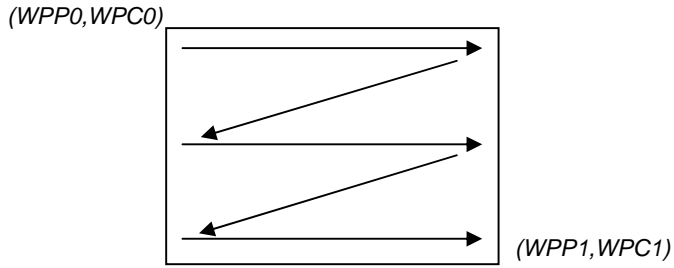
Window Program Function can be used to refresh the RAM data in a specified window of SRAM address. When window programming is enabled, the CA and RA increment and wrap around will be automatically adjusted, and therefore allow effective data update within the window.

The direction of Window Program will depend on the WA (AC[0]), RID (AC[2]), auto-increment order (AC[1]) and MX (LC[1]) register setting. WA decides whether the program RAM address advances to next row/column after reaching the specified window column / row boundary. RID controls the RAM address incrementing from WPP0 toward WPP1 (RID=0) or reverse the direction (RID=1). Auto-increment order directs the RAM address increment vertically (AC[1]=1) or horizontally (AC[1]=0). MX results the RAM column address incrementing from 97-WPC0 to 97-WPC1 (MX=1) or WPC0 to WPC1 (MX=0).

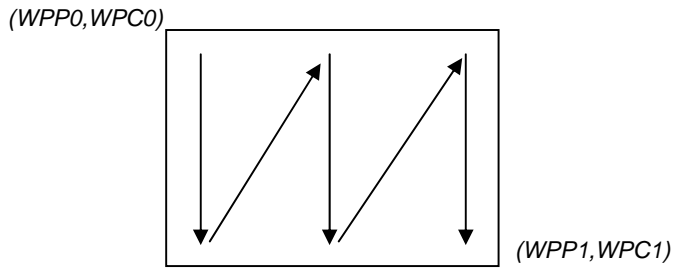
By different combination of RID, AC[1], MX, and by setting CA, RA at proper corners of the "window", effects such as mirrors and rotations can be easily achieved.

Setting or resetting AC[4] does not affect the value of CA and RA. After Window Program is enabled, remember to reposition CA, RA to a pixel inside the "window". If CA, RA points to a pixel outside the "window", the subsequent data write can produce undefined results.

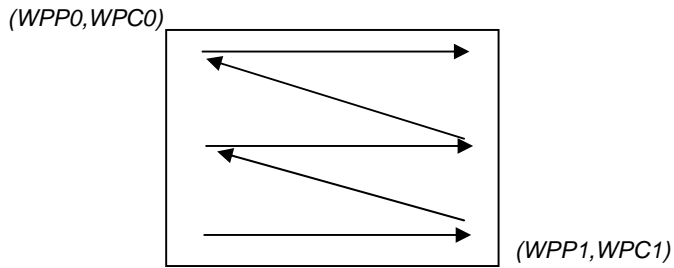
Auto-increment order = 0 MX=0 RID = 0



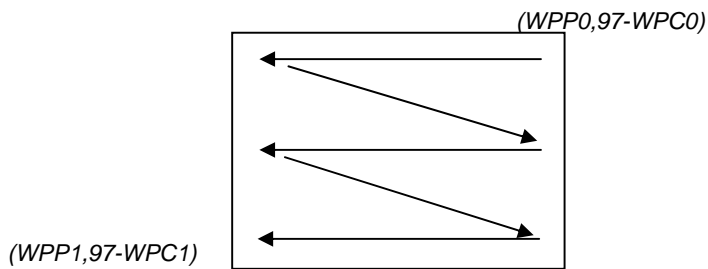
Auto-increment order = 1 MX=0 RID = 0



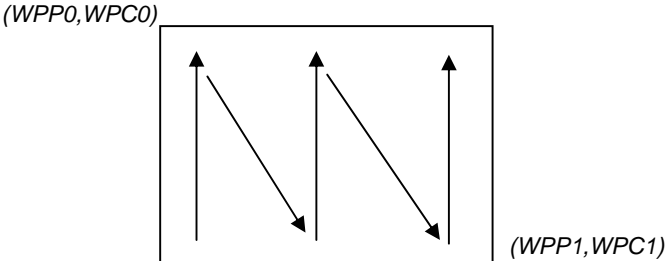
Auto-increment order = 0 MX=0 RID = 1



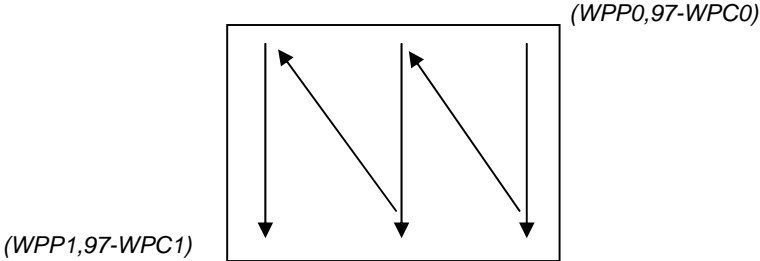
Auto-increment order = 0 MX=1 RID = 0



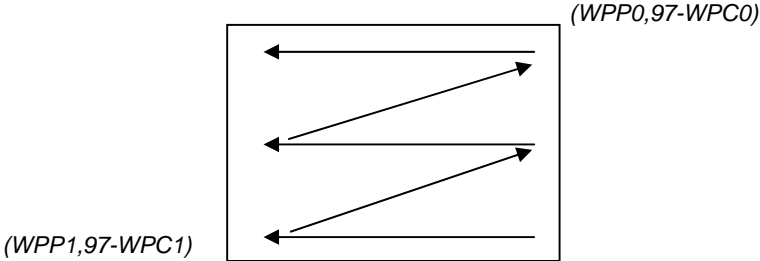
Auto-increment order = 1 MX=0 RID = 1



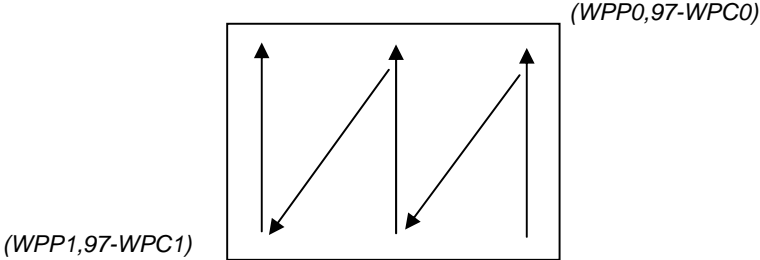
Auto-increment order = 1 MX=1 RID = 0



Auto-increment order = 0 MX=1 RID = 1



Auto-increment order = 1 MX=1 RID = 1



(37) Set OTP Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set OTPC (Double byte command)	0	0	1	0	1	1	1	0	0	0
<i>OTPC</i> register parameter										

This command is for OTP operation control:

OTPC[2:0] : OTP command

- 000 : Sleep
- 001 : OTP Read
- 010 : OTP Erase
- 011 : OTP Program
- 1XX : For UltraChip use only.

- OTPC[3] : OTP Enable (automatically cleared each time after OTP command is done)
- OTPC[4] : OTP value valid (ignore OTP value when L)
- OTPC[5] : For testing only. Set to 0 for normal operation

The following commands (38~42) are only valid when OTPC[3]=1.

DC[2] and OTPC[3] are mutually exclusive. Only one of these two control flags can be set to ON at any time. In other words, when DC[2] is ON, all OTP operations will be blocked, and, when OTP operation is active, set DC[2] to 1 will be blocked.

(38) Set OTP Write Mask

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set OTPM (Double byte command)	0	0	1	0	1	1	1	0	0	1
<i>OTPM</i> register parameter										

This command will enable write to each of the 8 individual OTP bits and is valid only when OTPC[3]=1.

When OTPM[x]=1, the x-th bit of the OTP memory will be programmed to "1". OTPM[x]=0 means no write action for x-th bit. And the content of this bit will not change.

The amount of "programming current" increases with the number of 1's in OTPM. If the "programming current" appears to be too high for the LCM design (e.g. TST4 ITO trace is not wide enough to supply the current), use multiple write cycles and distribute the 1's evenly into these cycles.

PMO[7:6] is used for UC1682 production tuning and is reserved for UltraChip use only. Please do NOT overwrite the content of these two OTP cells by always keeping OTPM[7:6]=00b.

OTPM [5:0]: Set PMO value

OTPM [7:6]: Set LRO value (to fine-tune *Line Rate*)

- 00: No change**
- 01: -10%
- 10: +10%
- 11: +20%

This command is only valid when OTPC[3]=1.

(39) Set VOTP1 Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set OTP2 (Double byte command)	0	0	1	1	1	1	0	1	0	0
Shared register parameter										

This command is for fine tuning V_{OTP1} setting (use with BR=00) and is valid only when OTPC[3]=1.

(40) Set VOTP2 Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set OTP3 (Double byte command)	0	0	1	1	1	1	0	1	0	1
Shared register parameter										

This command is for fine tuning V_{OTP2} PM setting (use with BR=10) and is valid only when OTPC[3]=1.

(41) Set OTP Write Timer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set OTP4 (Double byte command)	0	0	1	1	1	1	0	1	1	0
Shared register parameter										

This command is valid only when OTPC[3]=1.

(42) Set OTP Read Timer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set OTP5 (Double byte command)	0	0	1	1	1	1	0	1	1	1
Shared register parameter										

This command is valid only when OTPC[3]=1.

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1681 via registers CEN, DST, DEN, FLT, FLB, and partial display control flags LC[9:8] and LC[0].

Combined with low power partial display mode and a low bias ratio of 5, UC1681 can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS} , i.e.

$$BR = V_{LCD} / V_{BIAS},$$

where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux} + 1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=68), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally can not maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as Mux Rate decreases, and the shades near the two ends of the spectrum will start to lose visibility.

UC1681 supports four *BR* as listed below. *BR* can be selected by software program.

BR	0	1	2	3
Bias Ratio	5	7	8	9

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four (4) different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per °C	-0.05	-0.10	-0.15	-0.20

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[3:2]. For good product reliability, it is recommended to keep V_{LCD} under 11.8V over the entire operating range.

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and *TC* (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T \%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of *BR* register, as illustrated in the table on the next page,

PM is the numerical value of *PM* register,

T is the ambient temperature in °C, and

C_T is the temperature compensation coefficient as selected by *TC* register.

V_{LCD} FINE TUNING

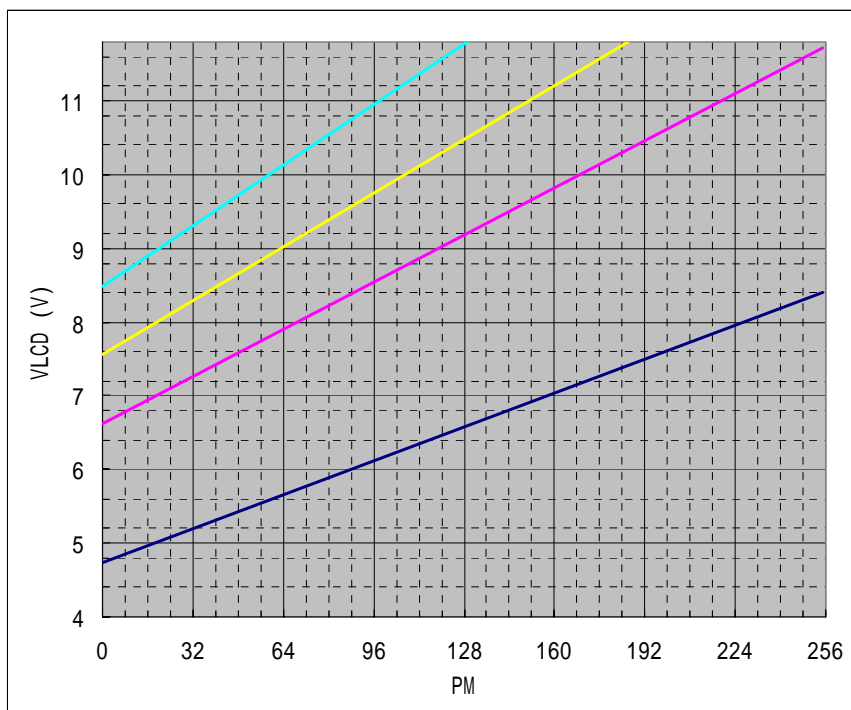
Color STN LCD is sensitive to even a 0.5% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different vendors. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

For the best results, software or OTP based V_{LCD} adjustment is the recommended method for V_{LCD} fine tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

LOAD DRIVING STRENGTH

The power supply circuit of UC1681 is designed to handle LCD panels with loading up to ~12nF using 10-Ohm/Sq ITO glass with $V_{DD2/3} \geq 2.65V$. For larger LCD panels use lower resistance ITO glass or COF packaging.

Due to crosstalk consideration, ~12nF is also the recommended maximum LCD panel size for COG applications, unless 7-Ω/Sq or lower resistance ITO glass is used.

V_{LCD} QUICK REFERENCEV_{LCD}-PM relationship for different BR setting at 25°C.

BR	V _{CO} (V)	V _{PM} (mV)	PM	V _{LCD} (V)
5	4.7391	14.364	0	4.739
			255	8.402
7	6.6126	20.047	0	6.613
			255	11.725
8	7.5538	22.856	0	7.554
			186	11.805
9	8.4757	25.737	0	8.476
			130	11.822

Note:

1. For good product reliability, keep V_{LCD (max)} under 11.8V under all operating temperature.
2. The integer values of BR above are for reference only and may have slight shift.

HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

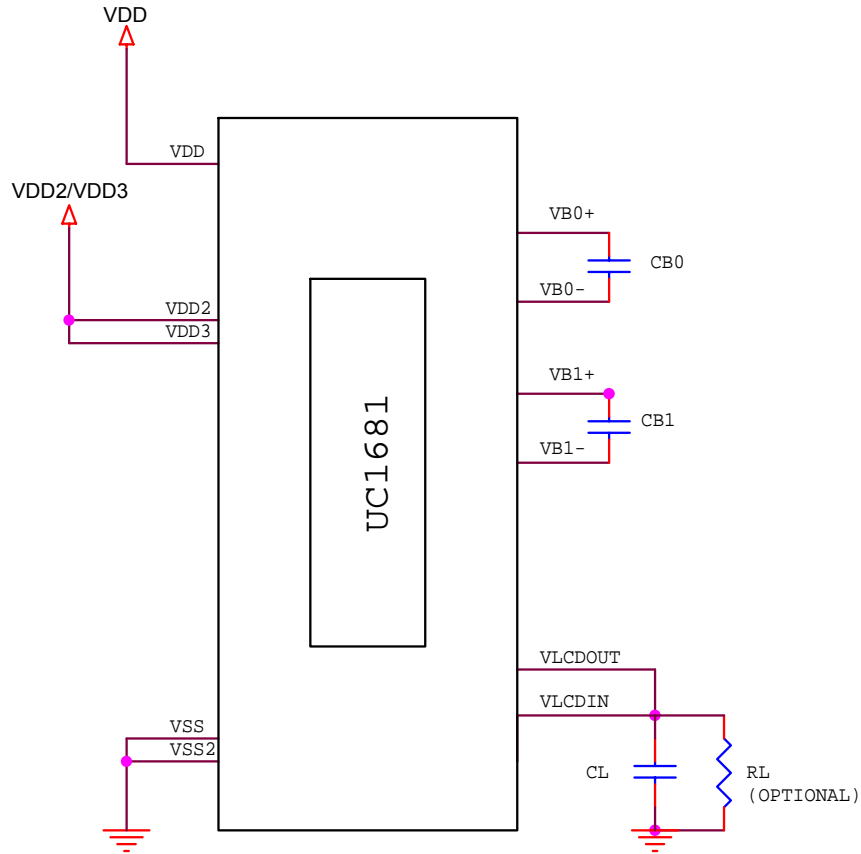


FIGURE 1: Reference circuit using internal Hi-V generator circuit

Note

Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)

C_B : 300x LCD load capacitance or 2.2 μ F (2V), whichever is higher.

C_L : 15nF~50nF (16V) is appropriate for most applications.

R_L : 3.3~10M Ω to act as a draining circuit when V_{DD} is shut down abruptly.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1681 contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Four different line rates are provided for system design flexibility. The line rate is controlled by register LC[4:3]. When Mux-Rate is above 28, frame rate is calculated as:

$$\text{Frame Rate} = \text{Line-Rate} / \text{Mux-Rate.}$$

When Mux-Rate is lowered to 28 (and 20), line rate will be scaled down by 2 (and 3) times automatically reduce power consumption.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Frame rate 220Hz or higher is recommended for 32-shade mode. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

When switching from 32-shade modulation to 8-shade modulation, line rate will be scaled down automatically by ~30%.

Under most situations, flicker behavior is similar between these two different modulation schemes. However, it is recommended to test each mode to make sure the result is as expected.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG drivers are in Idle mode, they will be connected together to ensure zero DC condition on the LCD.

DRIVER ARRANGEMENTS

The naming conventions are: COM(x), where x=1~68, refers to the COM driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via *Set Display Enable* command. When DC[2] is set to OFF (logic "0"), both COM and SEG drivers will become idle and UC1681 will put itself into Sleep mode to conserve power.

When DC[2] is set to ON, the DE flag will become "1", and UC1681 will first exit from Sleep mode, restore the power (V_{LCD} , V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL SCROLL

Control register FLT and FLB specify two regions of rows which are not affected by the SL register. Since SL register can be used to implement scroll function. FLT and FLB registers can be used to implement fixed regions when the other part of the display is scrolled by SL.

PARTIAL DISPLAY

UC1681 provides flexible control of Mux Rate and active display area. Please refer to command *Set COM End*, *Set Partial Display Start*, and *Set Partial Display End* for more detail.

GRAY-SHADE MODULATION MODE

UC1681 has two gray-shade modulation modes: 32-shade and 8-shade.

The 8-shade mode will consume roughly 25~30% less power than the 32-shade mode, and can be used for situations where power consumption is more critical than color fidelity.

Changing gray-shade modulation mode does not affect the content of SRAM display buffer, and the image data will remain the same after switching back and forth between 8-shade mode and 32-shade mode.

INPUT COLOR FORMATS

UC1681 supports the following four different input color formats.

256C (8-bit/RGB): This is the most compact color mode, and is intended to minimize the bus cycle required to refresh the display buffer. On-chip extension circuit will automatically expand the input RGB data into on-chip RAM buffer format.

4KC (12-bit/RGB): In this color mode, G will be extended while B will be dithered, and the input data will be converted into 4R-5G-4B format before they are stored to display RAM.

60.5KC (16-bit/RGB): On-chip dither engine will convert the input data into internal 13-bit-per-RGB pixel format and store it to on-chip display RAM. This is the default mode.

465KC (24-bit/RGB): On-chip dither engine will convert input data into 4R-5G-4B format and store it to on-chip display RAM. This mode provides the smoothest shades and the most vivid color in the LCD.

Changing color mode does not affect the content already stored in the display buffer RAM. Users can use several color modes together in real time.

For example, the menu portion can be painted in 256-color mode for fast update speed, and then switch to 60.5K-color mode, together with window programming option, and take advantage of built-in dither engine to produce smooth graphics images.

ITO LAYOUT AND LC SELECTION

Since the COM scanning pulse of UC1681 can be as short as 32 μ s, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

COM ITO TRACES

Excessive COM scanning pulse RC decay can cause fluctuation of contrast and increase COM direction crosstalk.

Please limit the worst case of COM signals RC delay (RC_{MAX}) as calculated below

$$(R_{ROW} / 2.7 + R_{COM} + R_{OUT}) \times C_{ROW} < 2.2\mu S$$

where

- C_{ROW} : LCD loading capacitance of one row of pixels. It can be calculated by $C_{LCD}/\text{Mux-Rate}$, where C_{LCD} is the LCD panel capacitance.
- R_{ROW} : ITO resistance over one row of pixels within the active area
- R_{COM} : COM routing resistance from IC to the active area + COM driver output impedance.

In addition, please also make sure

$$|RC_{MAX} - RC_{MIN}| < 0.5\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

(Use worse case parameters for the above calculations.)

SEG ITO TRACES

Excessive SEG signal RC decay can cause image dependent changes of medium gray shades and sharply increase of SEG direction crosstalk.

For good image quality, please minimize SEG ITO trace resistance and limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 0.4\mu S$$

where

- C_{COL} : LCD loading capacitance of one pixel column. It can be calculated by $C_{LCD} / \#_of_column$, C_{LCD} is the LCD panel capacitance.
- R_{COL} : ITO resistance over one column of pixels within the active area

- R_{SEG} : SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worse case parameters for the above calculations.)

SELECTING LIQUID CRYSTAL

The selection of LC material is crucial to achieve the optimum image quality of finished LCM.

When $(V_{90}-V_{10})/V_{10}$ is too large, contrast will drop, color saturation will deteriorate, and images will look murky and dull. When $(V_{90}-V_{10})/V_{10}$ is too small, image contrast becomes too strong, visibility of shades will suffer, and crosstalk will increase sharply for medium shades.

For the best result, it is recommended the LC material has the following characteristics:

$$(V_{90}-V_{10})/V_{10} = (V_{ON}-V_{OFF})/V_{OFF} \times 0.72 \sim 0.80$$

where V_{90} , V_{10} is the LC characteristics, and V_{ON} , V_{OFF} is the ON and OFF V_{RMS} voltage produced by LCD driver IC at the specific Mux-rate.

Two examples are provided below:

Duty	Bias	$V_{ON}/V_{OFF}-1$	x0.80	x0.72
1/68	1/9	12.72%	10.2%	9.16%
1/68	1/8	12.52%	10.0%	9.02%

FAST CSTN & COG

UC1681 can support very fast CSTN for video rate applications. For LCM with $t_r+t_f = 80\text{mS}$ or smaller, it is recommended to set the line rate higher such that the frame rate is 260Hz or higher. For such applications, special attentions are necessary for COG design to minimize crosstalk and ensure sufficient power is available to UC1681 to drive the LCM at such high speed.

- At this fast scan rate, the SEG/COM trace RC decay minimization will be very critical in minimizing crosstalk.
- MPU will perform frequent high speed update to the on-chip video RAM for video applications. Make sure the ITO does not cause on-chip $V_{DD}-V_{SS}$ to fall below 1.65V, and V_{SS} bounce is under 6% x V_{DD} .

For video CSTN applications, it is recommended to use low resistance ITO glass to help reduce SEG signal RC decay, minimize V_{DD} , V_{SS} noise, and ensure sufficient V_{DD2} , V_{SS2} supply for the on-chip DC-DC converter.

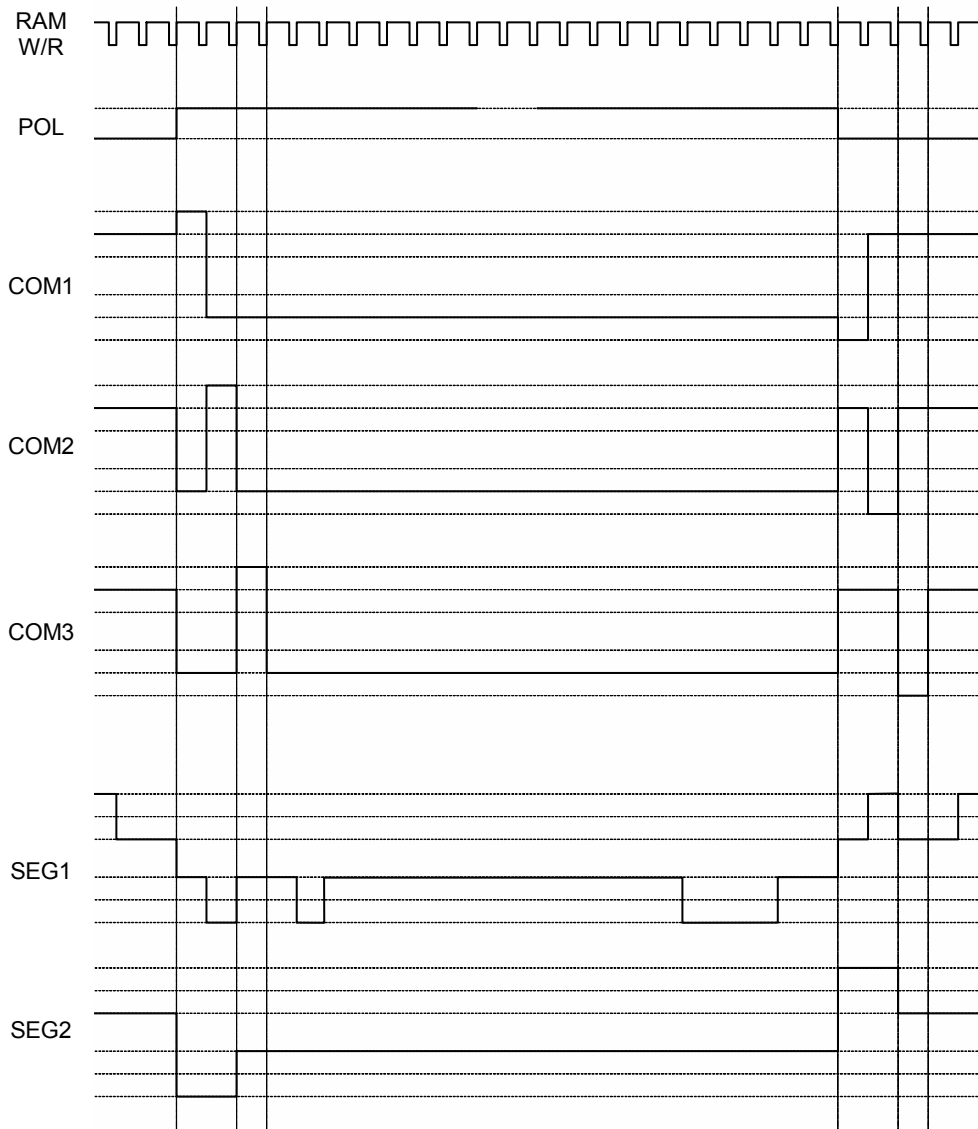


FIGURE 2: COM and SEG Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1681 supports two parallel bus protocols, in either 8-bit or 4-bit bus width, and three serial bus protocols.

Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules.

Bus Type	8080		6800		S8 (4wr)	S8uc (3wr)	S9 (3wr)	
Width	8-bit	4-bit	8-bit	4-bit	Serial			
Access	Read/Write				Write Only			
Control & Data Pins	BM[1:0]	10	00	11	01	00	00	01
	D[7:6]	Data	0X	Data	0X	10	11	10
	CS[1:0]	Chip Select						
	CD	Control/Data						0
	WR0	\overline{WR}		R/W		0		
	WR1	\overline{RD}		EN		0		
	D[5:4]	Data	–	Data	–	–		
	D[3:0]	Data	Data	Data	Data	D0=SCK, D3=SDA		

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}

	CS Disable Interface	CS Init bus state	CD 1<=>0 Init bus state	CD 1=>0 init color mapping	RESET Init bus state	RESET init color mapping
8-bit	✓	–	–	✓	✓	✓
4-bit	✓	–	✓	✓	✓	✓
S8 or S9	✓	✓	–	✓	✓	✓
S8uc	✓	–	✓	✓	✓	✓

- CS disable bus interface – CS can be used to disable Bus Interface Write / Read Access.
- CD refers to CD transitions within valid CS window. CD = 0 means write command or read status.
- CS / CD Sync / RESET can be used to initialize bus state machine (like 4 bits / S8 / S9).
- RESET can be pin reset / soft reset / power on reset.
- CD can be used to initialize the multi-byte input RGB format to/from on-chip SRAM mapping.

Table 3: Host interfaces Summary

PARALLEL INTERFACE

The timing relationship between UC1681 internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, either in 8-bit mode or 4-bit mode, by either *Set CA*, or *Set RA* command, a dummy read cycle needs to be performed before the actual data can propagate through the pipe-line and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

8-BIT & 4-BIT BUS OPERATION

UC1681 supports both 8-bit and 4-bit bus width. The bus width is determined by pin BM[1].

4-bit bus operation exactly doubles the clock cycles of 8-bit bus operation, MSB followed by LSB, including the dummy read, which also requires two clock cycles. The bus cycle of 4-bit mode is reset each time CD pin changes state (when CS is active).

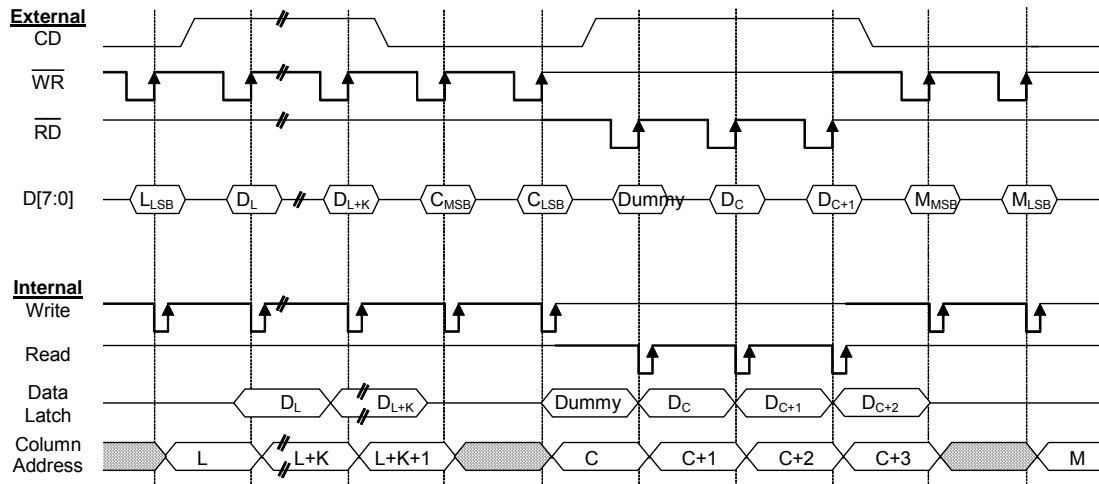


FIGURE 3: 8 bit Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1681 supports three serial modes, one 4-wire SPI mode (S8), one compact 3/4-wire mode (S8uc) and one 3-wire SPI mode (S9). Bus interface mode is determined by the wiring of the BM[1:0] and D[7:6]. See table in last page for more detail.

content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

S8 (4-WIRE) INTERFACE

Only write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

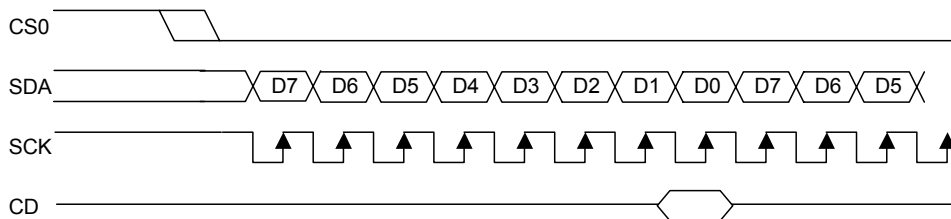


FIGURE 4: 4-wire Serial Interface (S8)

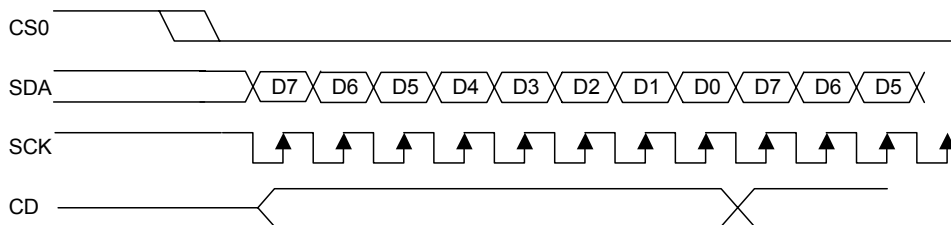


FIGURE 5: 3/4-wire Serial Interface (S8uc)

S8UC (3/4-WIRE) INTERFACE

Only write operations are supported in this 3/4-wire serial mode. The data format is identical to S8. However, in addition to CS pins, CD pin transitions will also reset the bus cycle in this mode. So, if CS pins are hardwired to enable chip-select, the bus can work properly with only three signal pins.

S9 (3-WIRE) INTERFACE

Only write operations are supported in this 3-wire serial mode. Pin CS[1-0] are used for chip select and bus cycle reset. On each write cycle, the first

bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS} . The toggle of CS0 or CS1 for each byte of data/command is recommended but optional.

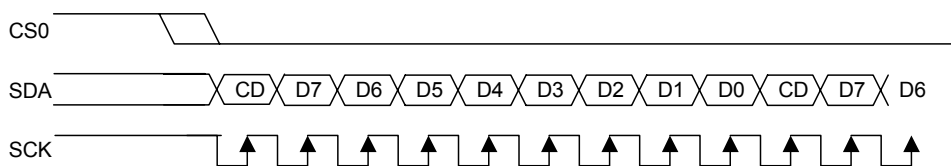


FIGURE 6: 3-wire Serial Interface (S9)

HOST INTERFACE REFERENCE CIRCUIT

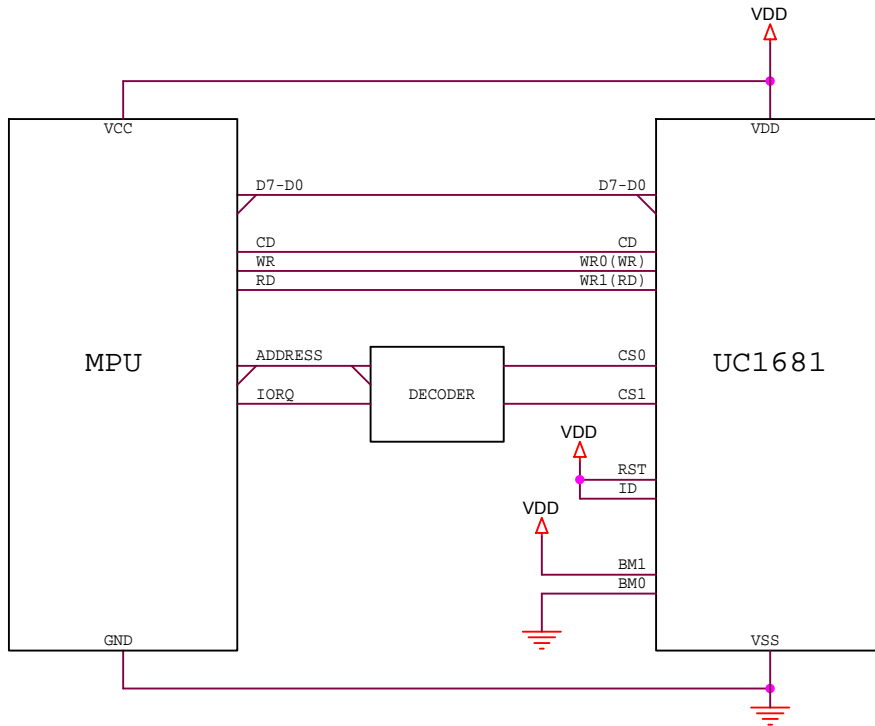


FIGURE 7: 8080/8bit parallel mode reference circuit

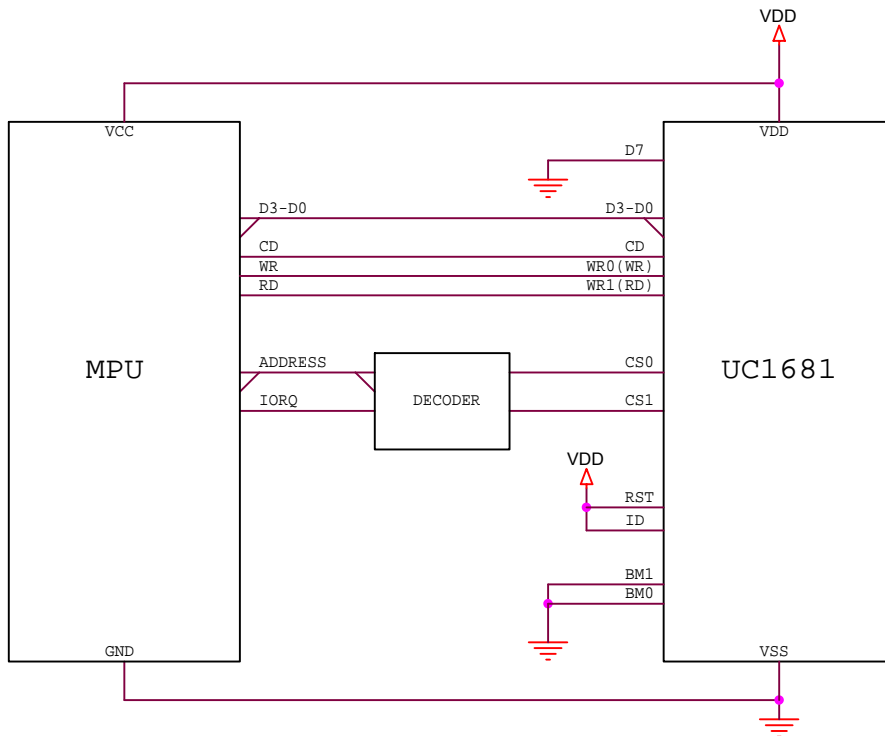


FIGURE 8: 8080/4bit parallel mode reference circuit

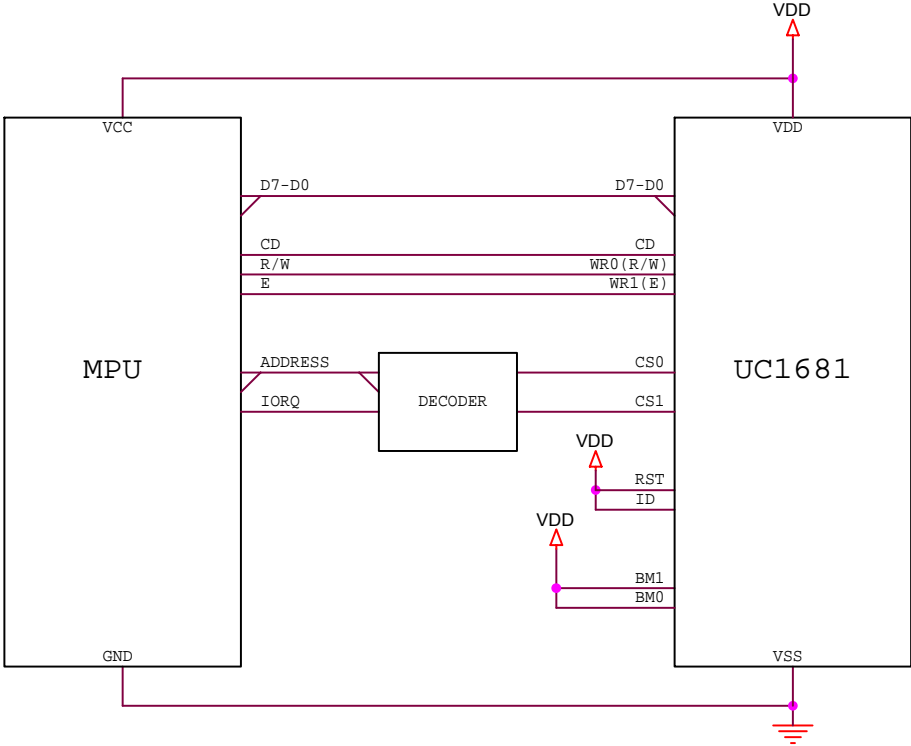


FIGURE 9: 6800/8bit parallel mode reference circuit

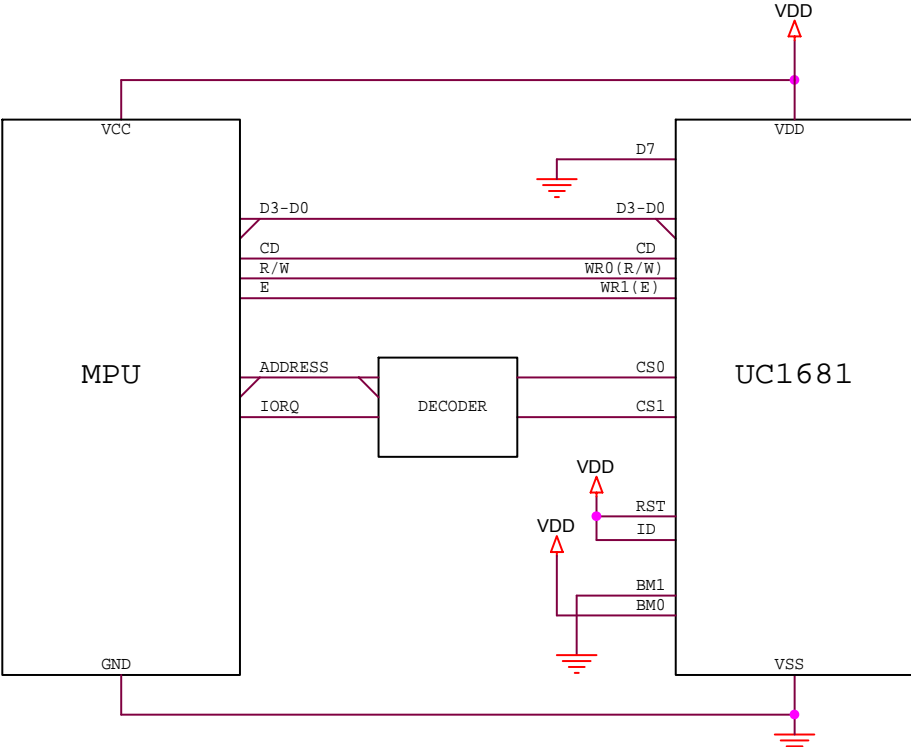


FIGURE 10: 6800/4bit parallel mode reference circuit

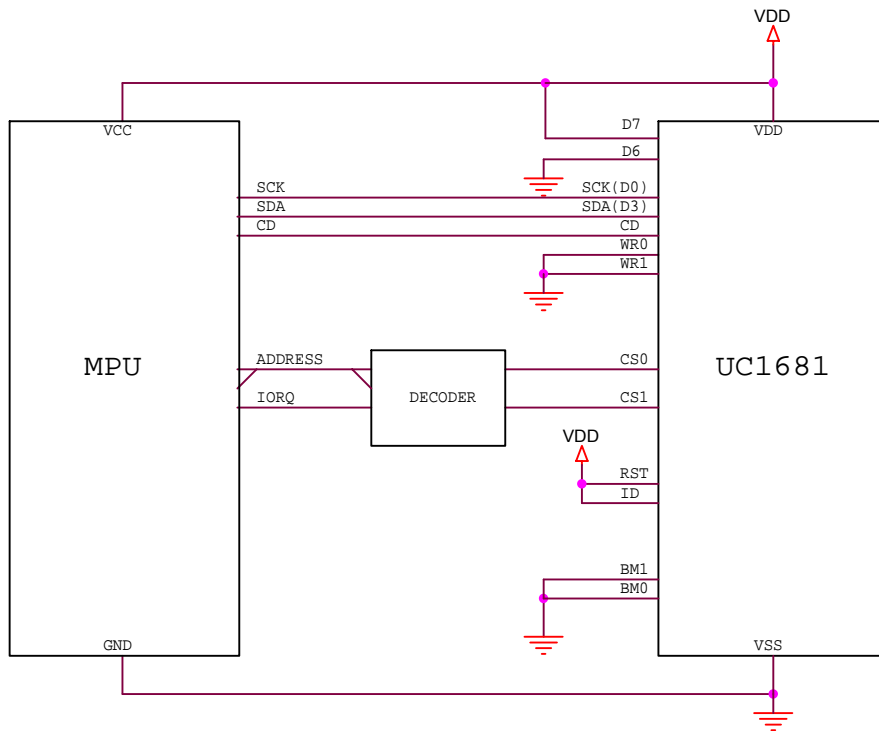


FIGURE 11: 4-Wires SPI (S8) serial mode reference circuit

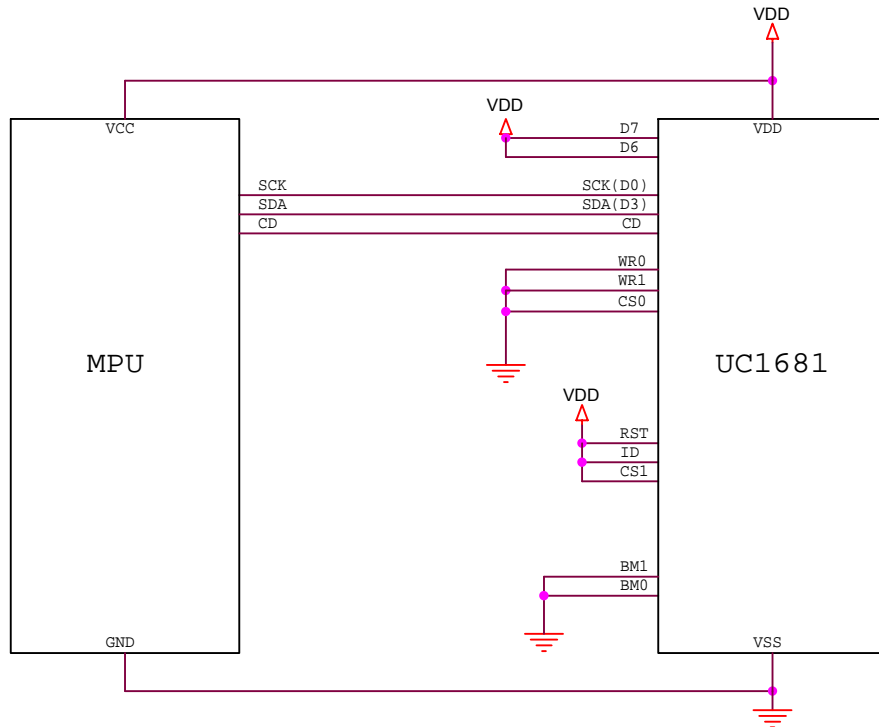


FIGURE 12: 3/4-Wires SPI (S8uc) serial mode reference circuit

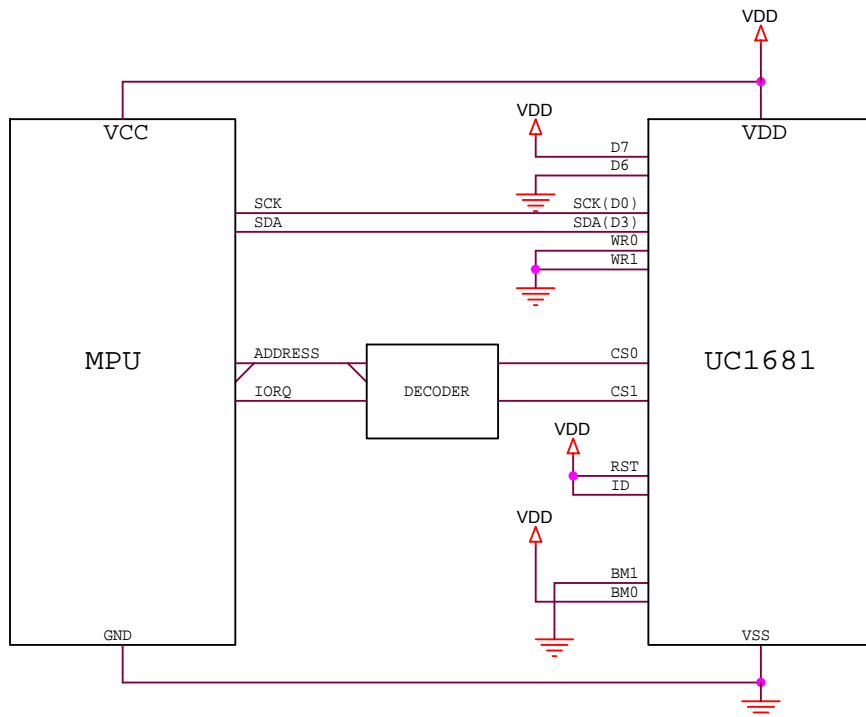


FIGURE 13: 3-Wires SPI (S9) serial mode reference circuit

Note

- ID pin is for production control. The connection will affect the content of D[7] when using *Get Status* command. Connect to V_{DD} for “H” or V_{SS} for “L”.
- RST pin is optional. When RST pin is not used, connect the pin to V_{DD}.

DISPLAY DATA RAM

DATA ORGANIZATION

The input display data (depend on color mode) are stored to a dual port static RAM (RAM, for Display Data RAM) organized as 68x98X13.

After setting CA and RA, the subsequent data write cycles will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing *Set Row Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of row (97), and system programmers need to set the values of RA and CA explicitly.

If WA is ON (1), when CA reaches the end of a row, CA will be reset to 0 and RA will increment or decrement, depending on the setting of row Increment Direction (RID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 67), RA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (97-CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect on the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), Fixed Line (FL) or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning COM electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FL=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field

$$Line = SL$$

Otherwise

$$Line = \text{Mod}(Line+1, 68)$$

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the "loop around" effect as it effectively resets *Line* to 0 when *Line+1* reaches 68. Effects such as scrolling can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field

$$Line = \text{Mod}(SL + MUX-1, 68)$$

where MUX = CEN + 1

Otherwise

$$Line = \text{Mod}(Line-1, 68)$$

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM are not affected by MY.

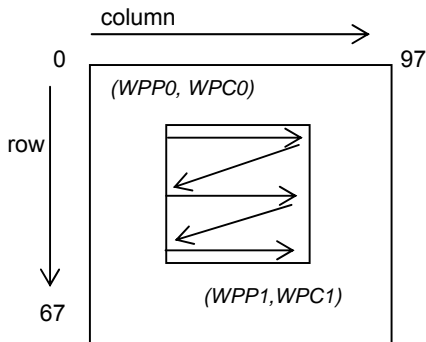
WINDOW PROGRAM

Window program is designed for data write in a specified window range of SRAM address. The procedure should start with window boundary registers setting ($WPP0$, $WPP1$, $WPC0$ and $WPC1$) and then enable AC[4]. After AC[4] sets, data can be written to SRAM within the window address range which is specified by ($WPP0$, $WPC0$) and ($WPP1$, $WPC1$). AC[4] should be cleared after any modification of window boundary registers and then set again in order to initialize another window program.

The data write direction will be determined by AC[2:0] and MX settings. When AC[0]=1, the data write can be consecutive within the range of the specified window. AC[1] will control the data write in either column or row direction. AC[2] will result the data write starting either from row $WPP0$ or $WPP1$. MX is for the initial column address either from $WPC0$ to $WPC1$ or from ($MC-WPC0$ to $MC-WPC1$).

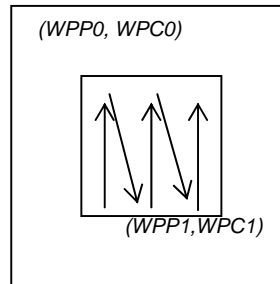
Example 1:

AC[2:0] = 001 MX=0



Example 2:

AC[2:0] = 111 MX = 0



Row Address	RAM										MY=0		MY=1			
	SL=0	SL=16	SL=0	SL=16	SL=0	SL=16	SL=0	SL=16	SL=0	SL=16	SL=0	SL=16	SL=0	SL=16		
00H	Blue	Green	Red	Blue	Green	Red							COM1	COM53	COM68	COM16
01H	Blue	Green	Red	Blue	Green	Red							COM2	COM54	COM67	COM15
02H													COM3	COM55	COM66	COM14
03H													COM4	COM56	COM65	COM13
04H													COM5	COM57	COM64	COM12
05H													COM6	COM58	COM63	COM11
06H													COM7	COM59	COM62	COM10
07H													COM8	COM60	COM61	COM9
08H													COM9	COM61	COM60	COM8
09H													COM10	COM62		COM7
0AH													COM11	COM63		COM6
0BH													COM12	COM64		COM5
0CH													COM13	COM65		COM4
0DH													COM14	COM66		COM3
0EH													COM15	COM67		COM2
0FH													COM16	COM68		COM1
10H													COM17	COM1		COM68
11H													COM18	COM2		COM67
12H													COM19	COM3		COM66
13H													COM20	COM4		COM65
14H													COM21	COM5		COM64
15H													COM22	COM6		COM63
16H													COM23	COM7		COM62
17H													COM24	COM8		COM61
18H													COM25	COM9		COM60
19H													COM26	COM10		COM59
1AH													COM27	COM11		COM58
1BH													COM28	COM12		COM57
1CH													COM29	COM13		COM56
2CH																COM40
2DH																COM39
2EH																COM38
2FH																COM37
30H																COM36
31H																COM35
32H																COM34
33H																COM33
34H																COM32
35H																COM31
36H																COM30
37H																COM29
38H																COM28
39H																COM27
3AH																COM26
3BH																COM25
3CH																COM24
3DH																COM23
3EH																COM22
3FH																COM22
40H													COM64	COM48	COM5	COM21
41H													COM65	COM49	COM4	COM20
42H													COM66	COM50	COM3	COM19
43H													COM67	COM51	COM2	COM18
													COM68	COM52	COM1	COM17

MX	SEG											
	SEG294	SEG293	SEG292	SEG291	SEG290			SEG290	SEG291	SEG292	SEG293	SEG294
0	SEG1	SEG2	SEG3	SEG4	SEG5			SEG290	SEG291	SEG292	SEG293	SEG294
1	SEG294	SEG293	SEG292	SEG291	SEG290			SEG5	SEG4	SEG3	SEG2	SEG1

Example for memory mapping: let MX = 0, MY = 0, SL = 0, LC[7:6] = 10b (RRRRR-GGGGG-BBBBB, 60.5K color), according to the data shown in the above table (R: 11111b, G: 11111b, B: 11111b):

- ⇒ 1st Byte write data: 1111111b
- ⇒ 2nd Byte write data: 1111111b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1681 has two different types of Reset: *Power-ON-Reset* and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about 5~10mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1681 enters RESET sequence:

- Operation mode will be "Reset"
- System Status bits RS and BZ will stay as "1" until the Reset process is completed. When RS=1, the IC will only respond to *Read Status* command. All other commands are ignored.
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1681 has three operating modes (OM): Reset, Normal, Sleep.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	OFF	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to *Power-ON-Reset*, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep mode.

For maximum energy utilization, Sleep mode is designed to retain charges stored in external capacitors C_{B0} , C_{B1} , and C_L . To drain these capacitors, use Reset command to activate the on-chip draining circuit.

Action	Mode	OM
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11
Reset command or RST_ pin pulled "L" Power ON Reset	Reset	00

Table 5: OM changes

Even though UC1681 consumes very little energy in Sleep mode (typically 5uA or less); however, since all capacitors are still charged, the leakage through COM drivers may damage the LCD over the long term. It is therefore recommended to use Sleep mode only for brief Display OFF operations, such as full-frame screen updates, and to use RESET for extended screen OFF operations.

EXITING SLEEP MODE

UC1681 contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1681 internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1681 power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait ~150 ms before the CPU starting to issue commands to UC1681. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands. However, while turning on V_{DD} , $V_{DD2/3}$ should be started not later than V_{DD} .

Delay allowance between V_{DD} and $V_{DD2/3}$ is illustrated as Figure 16.

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitors C_{BX+} , C_{BX-} , and C_L from damaging the LCD, when V_{DD} is switched off, use *Reset* mode to enable the built-in draining circuit and discharge these capacitors.

The draining resistor is 1K Ohm for both V_{LCD} and V_{B+} . It is recommended to wait $3 \times RC$ for V_{LCD} and $1.5 \times RC$ for V_{B+} . For example, if C_L is 15nF, then the draining time required for V_{LCD} is 0.5~1mS.

When external V_{LCD} is used, UC1681 will *NOT* drain V_{LCD} during *RESET*. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD} .

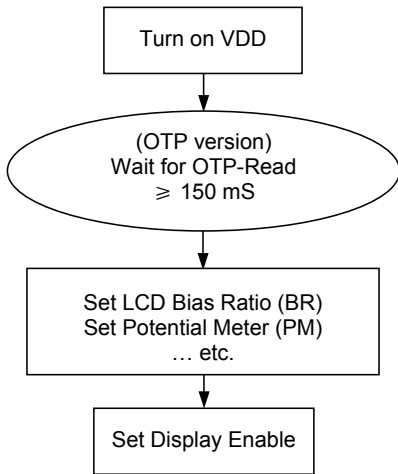


Figure 14: Reference Power-Up Sequence

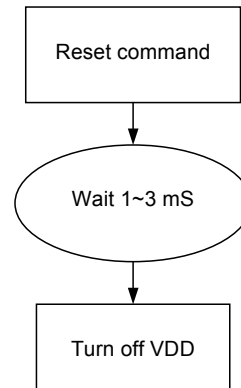


Figure 15: Reference Power-Down Sequence

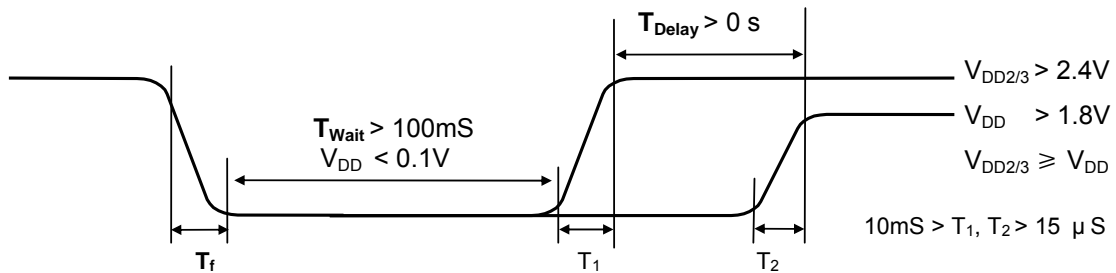


Figure 16: Delay allowance and Power Off-On Sequence

ONE TIME PROGRAMMING (OTP)

OVERVIEW

OTP feature is available for UC1681 such that LCM maker can record an PM offset value in non-volatile memory cells, which can then be used to adjust the effective V_{LCD} value, in order to achieve high level of consistency for LCM contrast across all shipments.

To accomplish this purpose, three operations are supported by UC1681:

OTP-Erase, OTP-Program, OTP-Read.

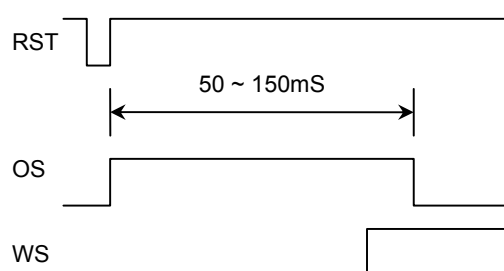
OTP-Program requires an external power source to be supplied to TST4 pin. These two operations should be performed only by the LCM makers.

OTP-Read is facilitated by the internal DC-DC converter built-in on UC1681, no external power source is required, and it is performed automatically after hardware RESET (power-ON or pin RESET).

OPERATION FOR THE SYSTEM USERS

For the OTP version of UC1681, the content of the NV memory will be read automatically after the power-on and hardware pin RESET. There is no user intervention or external power source required. When set up properly, the V_{LCD} will be fine tuned to achieve high level of consistency for the LCM contrast.

The OTP-READ is a relatively slow process and the time required can vary quite a bit. For a successful OTP-READ operation, the OS and WS bits in the *Read Status* commands will exhibit the following waveforms.



As illustrated above, the {OS, WS} will go through a {0,0} \Rightarrow {1,0} \Rightarrow {1,1} \Rightarrow {0,1} transition. When the {OS, WS}={0,1} state is reached, it means the LCM is ready to be turned on.

During the OTP-READ process, it is actually safe to issue commands or perform data write to the LCM. The only thing that is blocked is the LSB of the *Set Display Enable* command, which results in the DC[2] being effectively locked at "0" during this auto-OTP-READ process.

Although user can use *Read Status* command in a polling loop to make sure {OS,WS}={0,1} before proceeding with *Set Display Enable* command, however, it may be simpler to just issue *Set Display Enable* command every 0.2~2 second, repeatedly, together with other LCM optimization settings, such as BR, CEN, TC, etc.

The above "Periodical re-initializing" approach is also an effective safeguard against accidental display off events such as

- ESD strikes
- Mechanical shocks causing LCM connector to malfunction temporarily

HARDWARE VS. SOFTWARE RESET

In addition to the relatively slow cycle time, the OTP-READ cycle life of the OTP cell is limited at roughly 100,000 cycles. Due to this limited cycle life, the auto-OTP-READ is only performed for hardware RESET (power-ON and RST pin), but not for software *RESET* command.

If there is need to reset the LCM during its normal operation, it is recommended to use the software *RESET* for such operation control purpose and use hardware RESET only during the event of power up and power down.

OPERATION FOR THE LCM MAKERS

Always ERASE the OTP NV memory cells, before starting the Write process.

Please contact UltraChip for recommended OTP program sequence for your specific LCM design.

OTP OPERATION FOR LCM MAKERS

1. High voltage supply and timer setting

In OTP Program operation, two different high voltages are needed. In chip design, one high voltage is generated by internal charge pump (V_{LCD}), the other high voltage must be input from TST4 by external voltage source.

V_{LCD} value is controlled by register OTP3 and OTP2. The default values of these two registers are appropriate for most applications.

External TST4 power source is required for OTP Program operation. OTP Programming speed depends on the TST4 voltage. Considering the ITO trace resistance in COG modules, it is recommended to program the OTP cells one at a time, so that the required 7.8V at TST4 can be maintained with proper consistency.

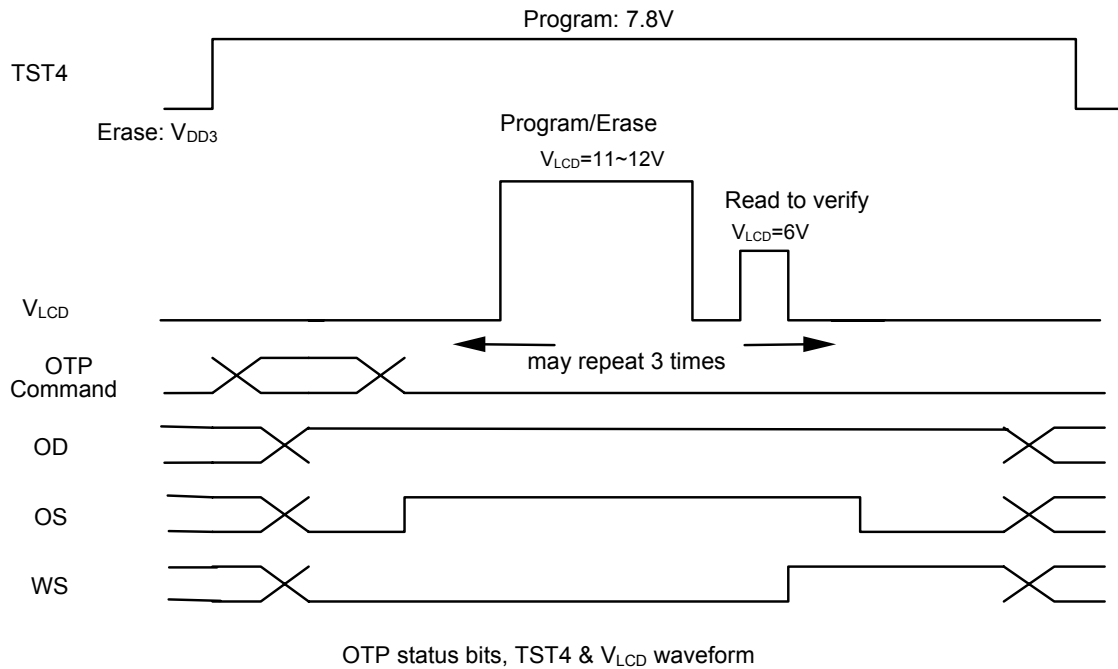
No external power source is required for OTP Erase and Read operation. For these OTP operation, TST4 should be open, or connected to V_{DD3} .

Operation	V_{LCD}	TST4 (external input)
Program	OTP3 : B4h (12V)	7.8V (1mA per bit)
Erase	OTP3 : B4h (12V)	Floating or V_{DD3}
Read	OTP2 : 82h (6V)	Floating or V_{DD3}

Note: Do Erase before Program. Program one bit at a time.

2. Read OTP status bits

With normal Get Status method (CD=0,W/R=1), OTP operation status can be monitored in the real time. There are 3 status bits (WS, OD, OS) in status register. OTP control circuit will read to verify if the operation (program, erase) success or not. If the operation succeeded, and current operation will be ended with WS=1. If it failed, last operation will be automatically retried two more times. If it fails 3 times, WS will be set to 0 and the operation is aborted. OD is OTP ID, which is either 1 for OTP IC or 0 for Non-OTP. No transition.



OTP CELL VALUE USAGE

There are 8 OTP cell bits. They are divided into two groups for different trimming purpose.

(1) OTP[5:0] : V_{LCD} Trimming; PMV is PM with trim; OTP[5:0] is equal to PMO[5:0].

- OTP[5]=0 : PMV = PM + OTP[4:0]
- OTP[5]=1 : PMV = PM – OTP[4:0]

(2) OTP[7:6] : Line rate is adjustable by setting OTP[7:6]

- | | |
|----------------------|----------|
| 00: No change | 01: -10% |
| 10: +10% | 11: +20% |

OTP COMMAND SEQUENCE SAMPLE CODES

The following tables are examples of command sequence for OTP Program and Erase operations. These are only to demonstrate some “*typical, generic*” scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

OTP operations (Erase, Program, Read) and Set Display ON is mutual exclusive. There is no harm done to the IC or the LCM if this is violated. However, the violating commands will be ignored.

Type Required: These items are required
 Customized: These items are not necessary if customer parameters are the same as default
 Advanced: We recommend new users to skip these commands and use default values.
 Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

(1) OTP Program Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip Action	Comments
R	0	0	1	0	1	0	0	0	1	1	(15) Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	(39)Set V _{OTP1} Potentiometer	Set OTP V _{LCD} OTP2:82h(6V)
R	0	0	1	0	0	0	0	0	1	0	(40)Set V _{OTP2} Potentiometer	Set OTP V _{LCD} OTP3:B4h(12V)
R	0	0	1	1	1	1	0	1	0	1	(41)Set OTP Write Timer	Set OTP Timer OTP4:20h(100ms)
R	0	0	0	0	1	0	0	0	0	0	(42)Set OTP Read Timer	Set OTP Timer OTP5:02h(10ms)
R	0	0	1	1	1	1	0	1	1	1	(38)Set OTP Write Mask	Set OTP Bit Mask
C	0	0	0	0	0	0	0	0	0	1		Ex: To program D0 to be 1, set the value to 00000001b *
R	-	-	-	-	-	-	-	-	-	-		Apply TST4 voltage Program: 7.8V **
R	0	0	1	0	1	1	1	0	0	0	(37) Set OTP Control	Set OTPC[3]=1 Set OTPC[2:0]=011
R	0	0	-	-	0	0	1	0	1	1	(3)Get Status & PM	Check OTP Status until OS=0 and WS=1
R												Remove TST4 voltage
R											V _{DD} =0V	Power OFF

* It is recommended that users program one bit at a time.

(2) OTP Erase Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	0	0	1	1	(15) Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	(39) Set V _{OTP1} Potentiometer	Set OTP V _{LCD}
R	0	0	1	0	0	0	0	0	1	0		OTP2:82h(6V)
R	0	0	1	1	1	1	0	1	0	1	(40) Set V _{OTP2} Potentiometer	Set OTP V _{LCD}
R	0	0	1	0	1	1	0	1	0	0		OTP3:B4h(12V)
R	0	0	1	1	1	1	0	1	1	0	(41) Set OTP Write Timer	Set OTP Timer
R	0	0	0	0	1	0	0	0	0	0		OTP4:20h(100ms)
R	0	0	1	1	1	1	0	1	1	1	(42) Set OTP Read Timer	Set OTP Timer
R	0	0	0	0	0	0	0	0	1	0		OTP5:02h(10ms)
R	0	0	1	0	1	1	1	0	0	1	(38) Set OTP Write Mask	Set OTP Bit Mask
C	0	0	0	0	1	1	1	1	1	1		Ex: To erase D[5:0], set the value to 00111111b *
R	0	0	1	0	1	1	1	0	0	0	(37) Set OTP Control	Set OTPC[3]=1
R	0	0	-	-	0	0	1	0	1	0		Set OTPC[2:0]=010
R	0	1	-	-	-	-	-	ws	-	os	(3) Get Status & PM	Check OTP Status
												Until OS=0 WS=1
R											V _{DD} =0V	Power OFF

* It is recommended that users clear all the bits to be programmed.

SAMPLE POWER MANAGEMENT COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "typical, generic" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

Type Rquired: These items are required

Customized: These items are not necessary if customer parameters are the same as default

Advanced: We recommend new users to skip these commands and use default values.

Optional: These commands depend on what users want to do.

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	-	-	-	-	-	-	-	-	-	-	Automatic Power-ON Reset.	Wait ~150mS after V _{DD} is ON
C	0	0	0	0	1	0	0	1	#	#	(5) Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	#	(20) Set LCD Mapping	
A	0	0	1	0	1	0	0	0	#	#	(15) Set Line Rate	Fine tune for power, flicker, contrast, and shading.
C	0	0	1	1	0	1	0	1	#	#	(22) Set Color Mode	
C	0	0	1	1	1	0	1	0	#	#	(26) Set LCD Bias Ratio	
R	0	0	1	0	0	0	0	0	0	1	(11) Set V _{BIAS} Potentiometer	LCD specific operating voltage setting
	0	0	#	#	#	#	#	#	#	#		
O	1	0	#	#	#	#	#	#	#	#	Write display RAM	Set up display image
		
	1	0	#	#	#	#	#	#	#	#		
R	0	0	1	0	1	0	1	1	1	1	(18) Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	(23) System Reset	
R	-	-	-	-	-	-	-	-	-	-	Draining capacitor	Wait ~1mS before V _{DD} OFF

BRIEF DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	(18) Set Display Disable	
C	1	0	#	#	#	#	#	#	#	#	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
		
	1	0	#	#	#	#	#	#	#	#		
R	0	0	1	0	1	0	1	1	1	1	(18) Set Display Enable	

* This is approach is recommended for brief display OFF (under 5 sec).

If image becomes unstable use the *Extended Display OFF* approach as shown below.

EXTENDED DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	(23) System Reset.	C _{B1} , C _{B1} , C _{LCD} discharged.
-	-	-	-	-	-	-	-	-	-	-		Extended display OFF Z z z z . . .
-	-	-	-	-	-	-	-	-	-	-		System waking up
R											Repeat power-up sequence	Repeat power up register setting sequence
C	1	0	#	#	#	#	#	#	#	#	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the RESET state.)
		
	1	0	#	#	#	#	#	#	#	#		
R	0	0	1	0	1	0	1	1	1	1	(18) Set Display Enable	

* The sequence is basically the same as the power up sequence, except *Power-ON Reset* is replaced by *System Reset* command, and an extended idle time in between.

ESD CONSIDERATION

1. UC1600 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is therefore highly recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

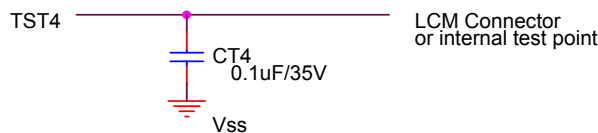
The following pins in UC1681 require special "ESD Sensitivity" consideration in particular:

Pin Name	MM +V _{DD}	MM +V _{SS}	HBM +V _{DD}	HBM +V _{SS}
TST4	Pass 75V	Pass 75V	Pass 500V	Pass 1000V

* MM: Machine Mode; HBM: Human Body Mode

According to UltraChip's Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

2. LCM design suggestions: Since TST4 is used as the power for programming the EEPROM cells, it is always possible for the OTP cell content to be changed by strong external pulse (such as ESD strike). To reduce such possibilities and minimize potential ESD damages to the finished LCD modules, consider adopting the following circuit:



- a) use a hidden testing point, instead of LCM connector pin, as a TST4 access point.
- b) use a good quality bypass capacitor as CT4 and place it close to the IC.

If TST4 access point is a hidden test-pin on a COG module, then CT4 is not critical. However, CT4 is highly recommended if

- i) the LCM is a COF module,
- ii) the LCM is a COG module with a connector pin used as TST4.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, note 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}-V_{DD}$	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.6	V
V_{LCD}	LCD Driving voltage (-25°C ~ +75°C)	-0.3	+14.0	V
V_{IN}	Digital input signal	-0.4	$V_{DD} + 0.5$	V
T_{OPR}	Operating temperature range	-30	+85	°C
T_{STR}	Storage temperature	-55	+125	°C

Notes

1. V_{DD} is based on $V_{SS} = 0V$
2. Stress beyond ranges listed above may cause permanent damages to the device.

SPECIFICATIONS
DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.8		3.3	V
$V_{DD2/3}$	Supply for bias & pump	$1.3 \geq V_{DD2/3} - V_{DD} \geq 0$	2.4		3.3	V
V_{LCD}	Charge pump output	$V_{DD2/3} = 2.8V, 25^{\circ}C$		10	11.8	V
V_D	LCD data voltage	$V_{DD2/3} = 2.8V, 25^{\circ}C$	0.95		1.65	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
C_{IN}	Input capacitance			5	10	PF
C_{OUT}	Output capacitance			5	10	PF
$R_{ON(SEG)}$	SEG output impedance	$V_{LCD} = 10V$		1.0	2.0	k Ω
$R_{ON(COM)}$	COM output impedance	$V_{LCD} = 10V$		1.2	2.5	K Ω
f_{LINE}	Average Line rate	LC[4:3] = 11b	-10%	21.0	+10%	Klps

POWER CONSUMPTION

$V_{DD} = 2.7V$,
 $V_{LCD} = 10.02V$,
 Mux Rate = 68,
 $C_B = 2\mu F$,
 Color Mode = 60.5K mode,

Bias Ratio = 8,
 Line Rate = 10b,
 Bus mode = 6800,
 Temperature = $25^{\circ}C$,
 All HV outputs are open circuit.

PM = 108,
 Panel Loading (PC[1:0]) = 01b,
 $C_L = 30nF$,
 OTP=80H,

Display Pattern	Conditions	Typ. (μA)	Max. (μA)
All-Pixel-OFF	Data Bus = idle, SEG/COM open	337	506
2-pixel checker	Data Bus = idle, SEG/COM open	441	662
None	Reset (stand-by current)	-	5

AC CHARACTERISTICS

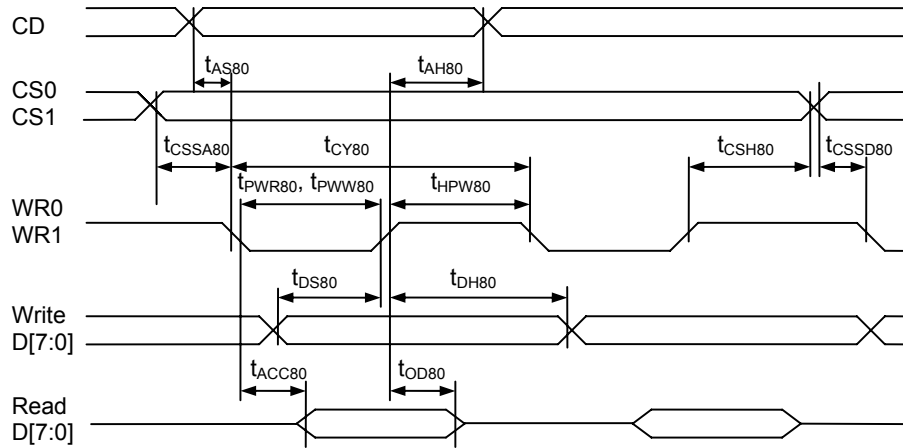


FIGURE 17: Parallel Bus Timing Characteristics (for 8080 MCU)

($2.5V \leq V_{DD} < 3.3V$, $T_a = -30$ to $+85^\circ C$)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 15	-	nS
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		140 80 140 80	-	nS
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits		70 70	-	nS
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits		40 40	-	nS
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		70 40 70 40	-	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 15	-	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	$C_L = 100pF$	- 25	50 50	nS
t_{CSSA80} t_{CSSD80} t_{CSh80}	CS1/CS0	Chip select setup time		5 10 5		nS

$(1.8V \leq V_{DD} < 2.5V, T_a = -30 \text{ to } +85^\circ\text{C})$

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 30	–	nS
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		280 160 280 160	–	nS
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits (read)		140 140	–	nS
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits (write)		80 80	–	nS
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		140 80 140 80	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		60 30	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	$C_L = 100\text{pF}$	- 50		nS
t_{CSSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 20 10		nS

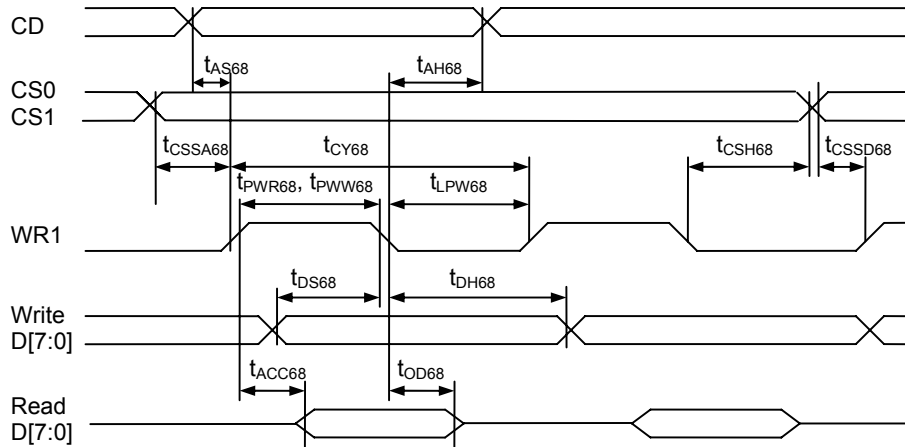


FIGURE 18: Parallel Bus Timing Characteristics (for 6800 MCU)

($2.5V \leq V_{DD} < 3.3V$, $T_a = -30$ to $+85^\circ C$)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 20	–	nS
t_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		140 80 140 80	–	nS
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		70 70	–	nS
t_{PWW68}		Pulse width 8 bits (write) 4 bits		40 40	–	nS
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		70 40 70 40	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 15	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	$C_L = 100pF$	– 25	50 50	nS
t_{CSSA68} t_{CSSD68} t_{CSH68}	CS1/CS0	Chip select setup time		5 10 5		nS

$(1.8V \leq V_{DD} < 2.5V, T_a = -30 \text{ to } +85^\circ\text{C})$

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 40	–	nS
t_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		280 160 280 160	–	nS
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		140 140	–	nS
t_{PWW68}		Pulse width 8 bits (write) 4 bits		80 80	–	nS
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		140 80 140 80	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		60 30	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	$C_L = 100\text{pF}$	- 50		nS
T_{CSSA68} T_{CSSD68} T_{CSH68}	CS1/CS0	Chip select setup time		10 20 10		nS

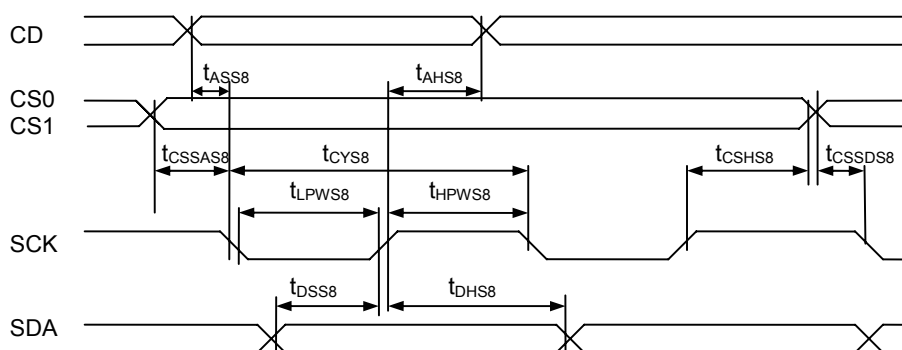


FIGURE 19: Serial Bus Timing Characteristics (for S8)

(2.5V ≤ V_{DD} < 3.3V, Ta= -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t _{ASS8}	CD	Address setup time		0	–	nS
t _{AHS8}		Address hold time		15	–	nS
t _{CYS8}	SCK	System cycle time		80	–	nS
t _{LPWS8}		Low pulse width		35	–	nS
t _{HPWS8}		High pulse width		35	–	nS
t _{DSS8}	SDA	Data setup time		30	–	nS
t _{DHS8}		Data hold time		20	–	nS
t _{CSSAS8}	CS1/CS0	Chip select setup time		5		nS
t _{CSSDS8}				10		
t _{CSHS8}				5		

(1.8V ≤ V_{DD} < 2.5V, Ta= -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t _{ASS8}	CD	Address setup time		0	–	nS
t _{AHS8}		Address hold time		30	–	nS
t _{CYS8}	SCK	System cycle time		160	–	nS
t _{LPWS8}		Low pulse width		70	–	nS
t _{HPWS8}		High pulse width		70	–	nS
t _{DSS8}	SDA	Data setup time		60	–	nS
t _{DHS8}		Data hold time		40	–	nS
t _{CSSAS8}	CS1/CS0	Chip select setup time		10		nS
t _{CSSDS8}				20		
t _{CSHS8}				10		

Note: When V_{DD} < 2.0V, letting V_{IL}=0.1V_{DD} and V_{IH}=0.9V_{DD} is recommended.

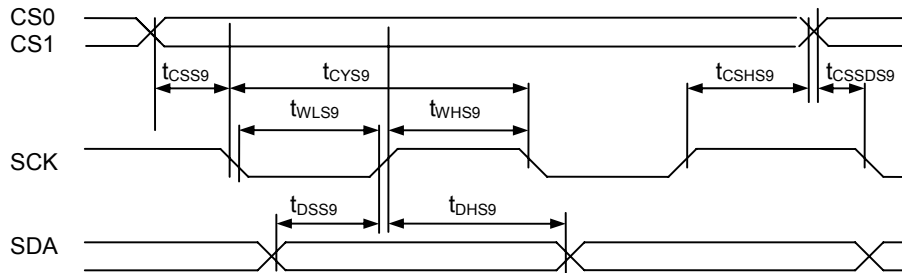


FIGURE 20: Serial Bus Timing Characteristics (for S9)

($2.5V \leq V_{DD} < 3.3V$, $T_a = -30$ to $+85^\circ C$)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		80	–	nS
t_{LPWS9}		Low pulse width		35	–	nS
t_{HPWS9}		High pulse width		35	–	nS
t_{DSS9}	SDA	Data setup time		30	–	nS
t_{DHS9}		Data hold time		20	–	nS
t_{CSSAS9}	CS1/CS0	Chip select setup time		5		nS
t_{CSSDS9}				10		
t_{CSHS9}				5		

($1.8V \leq V_{DD} < 2.5V$, $T_a = -30$ to $+85^\circ C$)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		160	–	nS
t_{LPWS9}		Low pulse width		70	–	nS
t_{HPWS9}		High pulse width		70	–	nS
t_{DSS9}	SDA	Data setup time		60	–	nS
t_{DHS9}		Data hold time		40	–	nS
t_{CSSAS9}	CS1/CS0	Chip select setup time		10		nS
t_{CSSDS9}				20		
t_{CSHS9}				10		

Note: When $V_{DD} < 2.0V$, letting $V_{IL} = 0.1V_{DD}$ and $V_{IH} = 0.9V_{DD}$ is recommended.

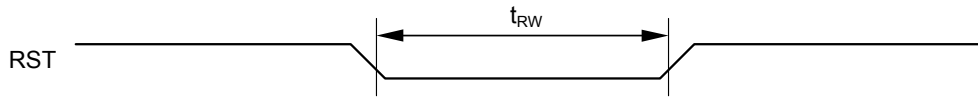


FIGURE 21: Reset Characteristics

($1.8V \leq V_{DD} < 3.3V$, $T_a = -30$ to $+85^{\circ}C$)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		500	–	nS

PHYSICAL DIMENSIONS

PAD COORDINATES

DIE SIZE:
13017 x 1386 μM^2

DIE THICKNESS:
0.5 mm

BUMP HEIGHT:
 $17 \pm 1 \mu\text{M}$ (within die)

BUMP SIZE:
 $128 \times 24.1 \mu\text{M}^2$ (Typ.)

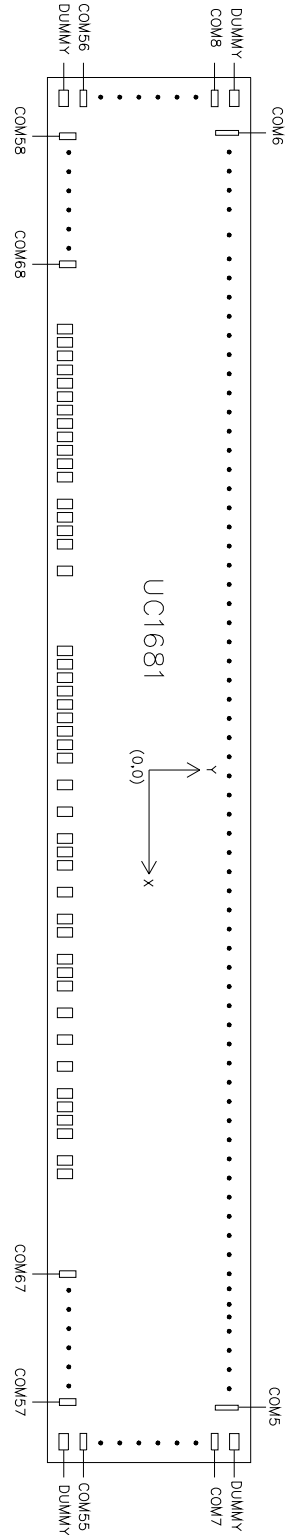
BUMP PITCH:
SEG: $41.5 \mu\text{M}$ (Typ.)
COM: $41.5 \mu\text{M}$ (Typ.)

BUMP GAP:
SEG/COM: $17.4 \mu\text{M}$ (Typ.)

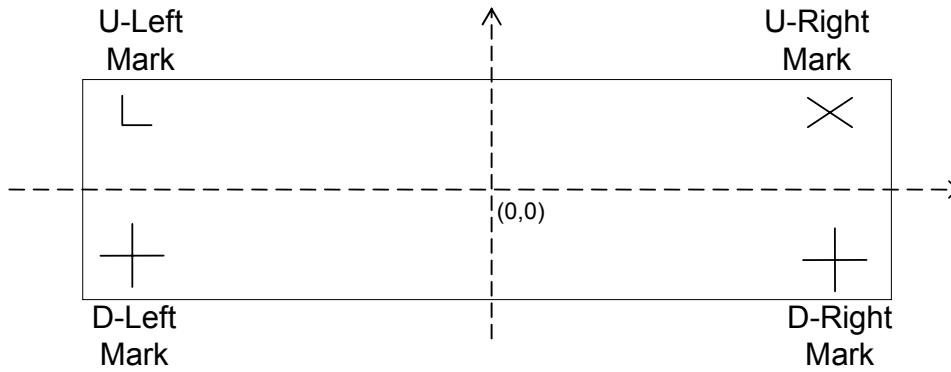
COORDINATE ORIGIN:
Chip center

PAD REFERENCE:
Pad center

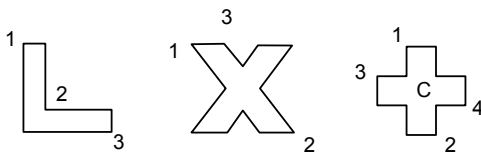
(Drawing and coordinates are for the Circuit/Bump view.)



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

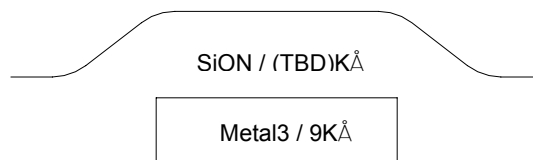
Alignment mark is on Metal3 under Passivation.

COORDINATES:

	U-Left Mark		U-Right Mark	
	X	Y	X	Y
1	-6303.0	643.0	6237.8	643.0
2	-6287.4	621.2	6305.2	608.6
3	-6256.1	605.7	6257.8	643.0

	D-Left Mark		D-Right Mark	
	X	Y	X	Y
1	-6285.0	-609.3	6266.0	-609.3
2	-6274.0	-643.0	6277.0	-643.0
3	-6307.0	-620.7	6244.0	-620.7
4	-6251.9	-631.7	6299.1	-631.7
C	-6279.5	-626.2	6271.5	-626.2

TOP METAL AND PASS



FOR OTP PROCESS CROSS-SECTION

PAD COORDINATES

Pin	Name	X	Y	W	H
1	DUMMY	-6403.0	610.7	104.0	29.6
2	COM8	-6403.0	563.7	104.0	29.6
3	COM10	-6403.0	516.7	104.0	29.6
4	COM12	-6403.0	469.7	104.0	29.6
5	COM14	-6403.0	422.7	104.0	29.6
6	COM16	-6403.0	375.7	104.0	29.6
7	COM18	-6403.0	328.7	104.0	29.6
8	COM20	-6403.0	281.7	104.0	29.6
9	COM22	-6403.0	234.7	104.0	29.6
10	COM24	-6403.0	187.7	104.0	29.6
11	COM26	-6403.0	140.7	104.0	29.6
12	COM28	-6403.0	93.7	104.0	29.6
13	COM30	-6403.0	46.7	104.0	29.6
14	COM32	-6403.0	-0.3	104.0	29.6
15	COM34	-6403.0	-47.3	104.0	29.6
16	COM36	-6403.0	-94.3	104.0	29.6
17	COM38	-6403.0	-141.3	104.0	29.6
18	COM40	-6403.0	-188.3	104.0	29.6
19	COM42	-6403.0	-235.3	104.0	29.6
20	COM44	-6403.0	-282.3	104.0	29.6
21	COM46	-6403.0	-329.3	104.0	29.6
22	COM48	-6403.0	-376.3	104.0	29.6
23	COM50	-6403.0	-423.3	104.0	29.6
24	COM52	-6403.0	-470.3	104.0	29.6
25	COM54	-6403.0	-517.3	104.0	29.6
26	COM56	-6403.0	-564.3	104.0	29.6
27	DUMMY	-6403.0	-611.3	104.0	29.6
28	COM58	-6205.5	-587.5	29.6	104.0
29	COM60	-6158.5	-587.5	29.6	104.0
30	COM62	-6111.5	-587.5	29.6	104.0
31	COM64	-6064.5	-587.5	29.6	104.0
32	COM66	-6017.5	-587.5	29.6	104.0
33	COM68	-5970.5	-587.5	29.6	104.0
34	DUMMY	-5898.7	-597.0	50.4	85.0
35	DUMMY	-5820.7	-597.0	50.4	85.0
36	D7	-5584.9	-597.0	52.0	85.0
37	VDDX	-5514.0	-597.0	52.0	85.0
38	D6	-5443.3	-597.0	52.0	85.0
39	D5	-5081.2	-597.0	52.0	85.0
40	D4	-5009.6	-597.0	52.0	85.0
41	D3	-4647.4	-597.0	52.0	85.0
42	D2	-4575.8	-597.0	52.0	85.0
43	D1	-4213.7	-597.0	52.0	85.0
44	D0	-4142.1	-597.0	52.0	85.0
45	RST	-3917.5	-597.0	52.0	85.0
46	CS1	-3658.5	-597.0	52.0	85.0
47	VDDX	-3587.6	-597.0	52.0	85.0
48	CS0	-3516.9	-597.0	52.0	85.0
49	CD	-3261.9	-597.0	52.0	85.0
50	WR0	-3190.3	-597.0	52.0	85.0
51	VDDX	-3019.3	-597.0	52.0	85.0
52	WR1	-2948.6	-597.0	52.0	85.0
53	BM0	-2693.6	-597.0	52.0	85.0
54	VDDX	-2622.7	-597.0	52.0	85.0
55	BM1	-2552.0	-597.0	52.0	85.0
56	TST4	-2247.4	-597.0	52.0	85.0
57	TST2	-2177.2	-597.0	52.0	85.0
58	ID	-1904.1	-597.0	52.0	85.0
59	VSS	-1711.0	-597.0	52.0	85.0
60	VSS	-1641.0	-597.0	52.0	85.0
61	VSS	-1571.0	-597.0	52.0	85.0

Pin	Name	X	Y	W	H
62	VSS	-1501.0	-597.0	52.0	85.0
63	VSS	-1431.0	-597.0	52.0	85.0
64	VSS	-1361.0	-597.0	52.0	85.0
65	VSS	-1291.0	-597.0	52.0	85.0
66	VSS	-1221.0	-597.0	52.0	85.0
67	VSS	-1151.0	-597.0	52.0	85.0
68	VSS	-1081.0	-597.0	52.0	85.0
69	VSS	-1011.0	-597.0	52.0	85.0
70	VSS	-941.0	-597.0	52.0	85.0
71	VSS2	-759.0	-597.0	52.0	85.0
72	VSS2	-689.0	-597.0	52.0	85.0
73	VSS2	-619.0	-597.0	52.0	85.0
74	VSS2	-549.0	-597.0	52.0	85.0
75	VSS2	-479.0	-597.0	52.0	85.0
76	VSS2	-409.0	-597.0	52.0	85.0
77	VSS2	-339.0	-597.0	52.0	85.0
78	VSS2	-269.0	-597.0	52.0	85.0
79	VDD2	-199.0	-597.0	52.0	85.0
80	VDD2	-129.0	-597.0	52.0	85.0
81	VDD2	-59.0	-597.0	52.0	85.0
82	VDD2	11.0	-597.0	52.0	85.0
83	VDD2	81.0	-597.0	52.0	85.0
84	VDD2	151.0	-597.0	52.0	85.0
85	VDD2	221.0	-597.0	52.0	85.0
86	VDD2	291.0	-597.0	52.0	85.0
87	VDD3	657.7	-597.0	52.0	85.0
88	VDD3	728.0	-597.0	52.0	85.0
89	VDD3	798.0	-597.0	52.0	85.0
90	VDD3	868.0	-597.0	52.0	85.0
91	VDD3	938.0	-597.0	52.0	85.0
92	VDD3	1008.0	-597.0	52.0	85.0
93	VDD	1443.3	-597.0	52.0	85.0
94	VDD	1513.6	-597.0	52.0	85.0
95	VDD	1583.6	-597.0	52.0	85.0
96	VDD	1653.6	-597.0	52.0	85.0
97	VDD	1723.6	-597.0	52.0	85.0
98	VDD	1793.6	-597.0	52.0	85.0
99	VDD	1863.6	-597.0	52.0	85.0
100	VDD	1933.6	-597.0	52.0	85.0
101	VDD	2003.6	-597.0	52.0	85.0
102	VDD	2073.6	-597.0	52.0	85.0
103	VB0+	2143.6	-597.0	52.0	85.0
104	VB0+	2213.6	-597.0	52.0	85.0
105	VB0+	2283.6	-597.0	52.0	85.0
106	VB0+	2353.6	-597.0	52.0	85.0
107	VB0+	2423.6	-597.0	52.0	85.0
108	VB0+	2493.6	-597.0	52.0	85.0
109	VB0+	2563.6	-597.0	52.0	85.0
110	VB0+	2633.6	-597.0	52.0	85.0
111	VB0+	2703.6	-597.0	52.0	85.0
112	VB1+	2945.9	-597.0	52.0	85.0
113	VB1+	3015.9	-597.0	52.0	85.0
114	VB1+	3085.9	-597.0	52.0	85.0
115	VB1+	3155.9	-597.0	52.0	85.0
116	VB1+	3225.9	-597.0	52.0	85.0
117	VB1+	3295.9	-597.0	52.0	85.0
118	VB1+	3365.9	-597.0	52.0	85.0
119	VB1+	3435.9	-597.0	52.0	85.0
120	VB1+	3505.9	-597.0	52.0	85.0
121	VB1-	3748.2	-597.0	52.0	85.0
122	VB1-	3818.2	-597.0	52.0	85.0

Pin	Name	X	Y	W	H
123	VB1-	3888.2	-597.0	52.0	85.0
124	VB1-	3958.2	-597.0	52.0	85.0
125	VB1-	4028.2	-597.0	52.0	85.0
126	VB1-	4098.2	-597.0	52.0	85.0
127	VB1-	4168.2	-597.0	52.0	85.0
128	VB1-	4238.2	-597.0	52.0	85.0
129	VB1-	4308.2	-597.0	52.0	85.0
130	VB0-	4550.5	-597.0	52.0	85.0
131	VB0-	4620.5	-597.0	52.0	85.0
132	VB0-	4690.5	-597.0	52.0	85.0
133	VB0-	4760.5	-597.0	52.0	85.0
134	VB0-	4830.5	-597.0	52.0	85.0
135	VB0-	4900.5	-597.0	52.0	85.0
136	VB0-	4970.5	-597.0	52.0	85.0
137	VB0-	5040.5	-597.0	52.0	85.0
138	VB0-	5110.5	-597.0	52.0	85.0
139	VLCDIN	5513.1	-597.0	52.0	85.0
140	VLCDIN	5583.1	-597.0	52.0	85.0
141	VLCDOUT	5653.3	-597.0	52.0	85.0
142	VLCDOUT	5723.3	-597.0	52.0	85.0
143	COM67	5962.5	-587.5	29.6	104.0
144	COM65	6009.5	-587.5	29.6	104.0
145	COM63	6056.5	-587.5	29.6	104.0
146	COM61	6103.5	-587.5	29.6	104.0
147	COM59	6150.5	-587.5	29.6	104.0
148	COM57	6197.5	-587.5	29.6	104.0
149	DUMMY	6403.0	-611.3	104.0	29.6
150	COM55	6403.0	-564.3	104.0	29.6
151	COM53	6403.0	-517.3	104.0	29.6
152	COM51	6403.0	-470.3	104.0	29.6
153	COM49	6403.0	-423.3	104.0	29.6
154	COM47	6403.0	-376.3	104.0	29.6
155	COM45	6403.0	-329.3	104.0	29.6
156	COM43	6403.0	-282.3	104.0	29.6
157	COM41	6403.0	-235.3	104.0	29.6
158	COM39	6403.0	-188.3	104.0	29.6
159	COM37	6403.0	-141.3	104.0	29.6
160	COM35	6403.0	-94.3	104.0	29.6
161	COM33	6403.0	-47.3	104.0	29.6
162	COM31	6403.0	-0.3	104.0	29.6
163	COM29	6403.0	46.7	104.0	29.6
164	COM27	6403.0	93.7	104.0	29.6
165	COM25	6403.0	140.7	104.0	29.6
166	COM23	6403.0	187.7	104.0	29.6
167	COM21	6403.0	234.7	104.0	29.6
168	COM19	6403.0	281.7	104.0	29.6
169	COM17	6403.0	328.7	104.0	29.6
170	COM15	6403.0	375.7	104.0	29.6
171	COM13	6403.0	422.7	104.0	29.6
172	COM11	6403.0	469.7	104.0	29.6
173	COM9	6403.0	516.7	104.0	29.6
174	COM7	6403.0	563.7	104.0	29.6
175	DUMMY	6403.0	610.7	104.0	29.6
176	COM5	6200.3	575.5	24.1	128.0
177	COM3	6158.8	575.5	24.1	128.0
178	COM1	6117.3	575.5	24.1	128.0
179	SEG1	6075.8	575.5	24.1	128.0
180	SEG2	6034.3	575.5	24.1	128.0
181	SEG3	5992.8	575.5	24.1	128.0
182	SEG4	5951.3	575.5	24.1	128.0
183	SEG5	5909.8	575.5	24.1	128.0
184	SEG6	5868.3	575.5	24.1	128.0
185	SEG7	5826.8	575.5	24.1	128.0
186	SEG8	5785.3	575.5	24.1	128.0

Pin	Name	X	Y	W	H
187	SEG9	5743.8	575.5	24.1	128.0
188	SEG10	5702.3	575.5	24.1	128.0
189	SEG11	5660.8	575.5	24.1	128.0
190	SEG12	5619.3	575.5	24.1	128.0
191	SEG13	5577.8	575.5	24.1	128.0
192	SEG14	5536.3	575.5	24.1	128.0
193	SEG15	5494.8	575.5	24.1	128.0
194	SEG16	5453.3	575.5	24.1	128.0
195	SEG17	5411.8	575.5	24.1	128.0
196	SEG18	5370.3	575.5	24.1	128.0
197	SEG19	5328.8	575.5	24.1	128.0
198	SEG20	5287.3	575.5	24.1	128.0
199	SEG21	5245.8	575.5	24.1	128.0
200	SEG22	5204.3	575.5	24.1	128.0
201	SEG23	5162.8	575.5	24.1	128.0
202	SEG24	5121.3	575.5	24.1	128.0
203	SEG25	5079.8	575.5	24.1	128.0
204	SEG26	5038.3	575.5	24.1	128.0
205	SEG27	4996.8	575.5	24.1	128.0
206	SEG28	4955.3	575.5	24.1	128.0
207	SEG29	4913.8	575.5	24.1	128.0
208	SEG30	4872.3	575.5	24.1	128.0
209	SEG31	4830.8	575.5	24.1	128.0
210	SEG32	4789.3	575.5	24.1	128.0
211	SEG33	4747.8	575.5	24.1	128.0
212	SEG34	4706.3	575.5	24.1	128.0
213	SEG35	4664.8	575.5	24.1	128.0
214	SEG36	4623.3	575.5	24.1	128.0
215	SEG37	4581.8	575.5	24.1	128.0
216	SEG38	4540.3	575.5	24.1	128.0
217	SEG39	4498.8	575.5	24.1	128.0
218	SEG40	4457.3	575.5	24.1	128.0
219	SEG41	4415.8	575.5	24.1	128.0
220	SEG42	4374.3	575.5	24.1	128.0
221	SEG43	4332.8	575.5	24.1	128.0
222	SEG44	4291.3	575.5	24.1	128.0
223	SEG45	4249.8	575.5	24.1	128.0
224	SEG46	4208.3	575.5	24.1	128.0
225	SEG47	4166.8	575.5	24.1	128.0
226	SEG48	4125.3	575.5	24.1	128.0
227	SEG49	4083.8	575.5	24.1	128.0
228	SEG50	4042.3	575.5	24.1	128.0
229	SEG51	4000.8	575.5	24.1	128.0
230	SEG52	3959.3	575.5	24.1	128.0
231	SEG53	3917.8	575.5	24.1	128.0
232	SEG54	3876.3	575.5	24.1	128.0
233	SEG55	3834.8	575.5	24.1	128.0
234	SEG56	3793.3	575.5	24.1	128.0
235	SEG57	3751.8	575.5	24.1	128.0
236	SEG58	3710.3	575.5	24.1	128.0
237	SEG59	3668.8	575.5	24.1	128.0
238	SEG60	3627.3	575.5	24.1	128.0
239	SEG61	3585.8	575.5	24.1	128.0
240	SEG62	3544.3	575.5	24.1	128.0
241	SEG63	3502.8	575.5	24.1	128.0
242	SEG64	3461.3	575.5	24.1	128.0
243	SEG65	3419.8	575.5	24.1	128.0
244	SEG66	3378.3	575.5	24.1	128.0
245	SEG67	3336.8	575.5	24.1	128.0
246	SEG68	3295.3	575.5	24.1	128.0
247	SEG69	3253.8	575.5	24.1	128.0
248	SEG70	3212.3	575.5	24.1	128.0
249	SEG71	3170.8	575.5	24.1	128.0
250	SEG72	3129.3	575.5	24.1	128.0

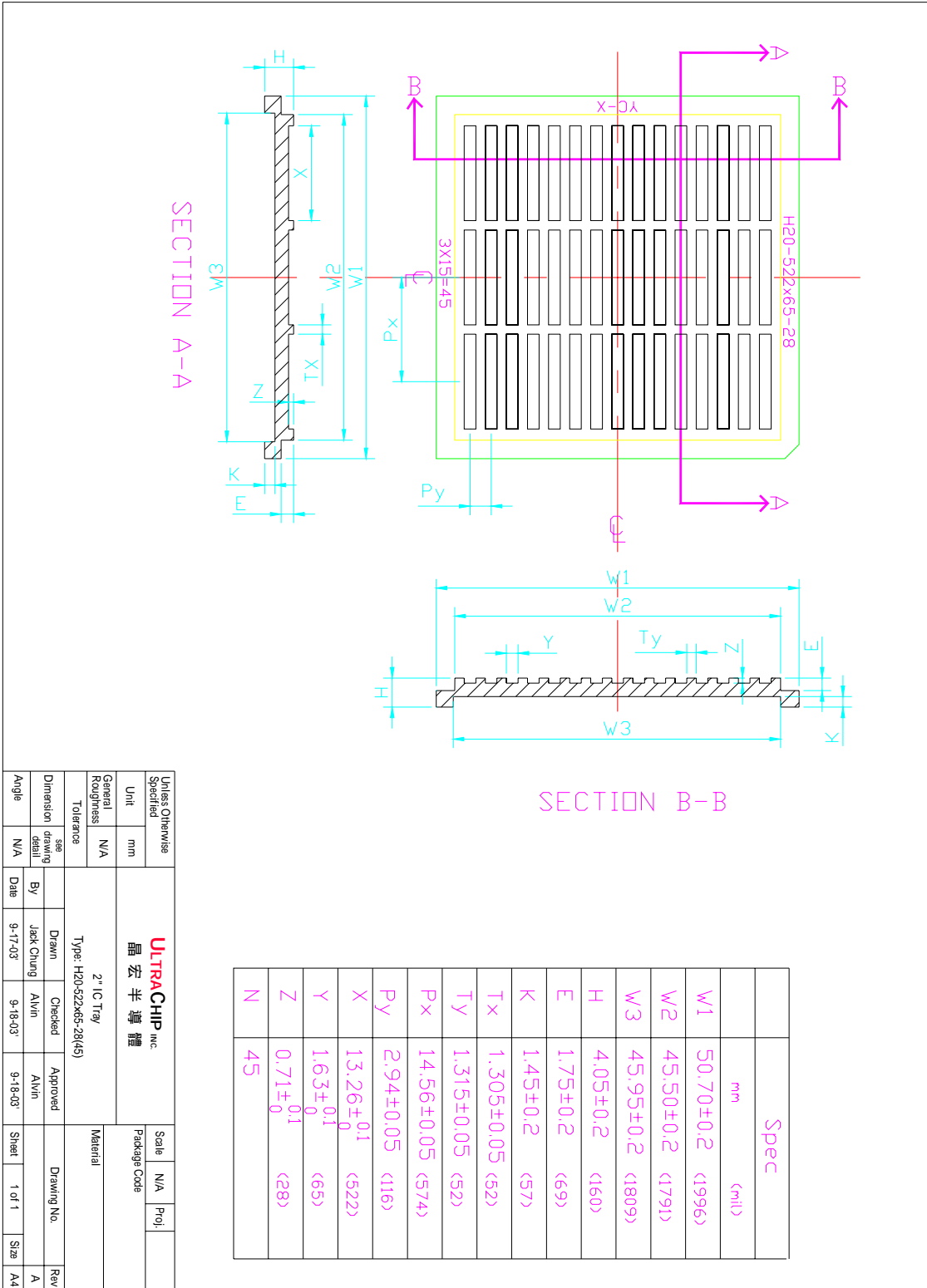
Pin	Name	X	Y	W	H
251	SEG73	3087.8	575.5	24.1	128.0
252	SEG74	3046.3	575.5	24.1	128.0
253	SEG75	3004.8	575.5	24.1	128.0
254	SEG76	2963.3	575.5	24.1	128.0
255	SEG77	2921.8	575.5	24.1	128.0
256	SEG78	2880.3	575.5	24.1	128.0
257	SEG79	2838.8	575.5	24.1	128.0
258	SEG80	2797.3	575.5	24.1	128.0
259	SEG81	2755.8	575.5	24.1	128.0
260	SEG82	2714.3	575.5	24.1	128.0
261	SEG83	2672.8	575.5	24.1	128.0
262	SEG84	2631.3	575.5	24.1	128.0
263	SEG85	2589.8	575.5	24.1	128.0
264	SEG86	2548.3	575.5	24.1	128.0
265	SEG87	2506.8	575.5	24.1	128.0
266	SEG88	2465.3	575.5	24.1	128.0
267	SEG89	2423.8	575.5	24.1	128.0
268	SEG90	2382.3	575.5	24.1	128.0
269	SEG91	2340.8	575.5	24.1	128.0
270	SEG92	2299.3	575.5	24.1	128.0
271	SEG93	2257.8	575.5	24.1	128.0
272	SEG94	2216.3	575.5	24.1	128.0
273	SEG95	2174.8	575.5	24.1	128.0
274	SEG96	2133.3	575.5	24.1	128.0
275	SEG97	2091.8	575.5	24.1	128.0
276	SEG98	2050.3	575.5	24.1	128.0
277	SEG99	2008.8	575.5	24.1	128.0
278	SEG100	1967.3	575.5	24.1	128.0
279	SEG101	1925.8	575.5	24.1	128.0
280	SEG102	1884.3	575.5	24.1	128.0
281	SEG103	1842.8	575.5	24.1	128.0
282	SEG104	1801.3	575.5	24.1	128.0
283	SEG105	1759.8	575.5	24.1	128.0
284	SEG106	1718.3	575.5	24.1	128.0
285	SEG107	1676.8	575.5	24.1	128.0
286	SEG108	1635.3	575.5	24.1	128.0
287	SEG109	1593.8	575.5	24.1	128.0
288	SEG110	1552.3	575.5	24.1	128.0
289	SEG111	1510.8	575.5	24.1	128.0
290	SEG112	1469.3	575.5	24.1	128.0
291	SEG113	1427.8	575.5	24.1	128.0
292	SEG114	1386.3	575.5	24.1	128.0
293	SEG115	1344.8	575.5	24.1	128.0
294	SEG116	1303.3	575.5	24.1	128.0
295	SEG117	1261.8	575.5	24.1	128.0
296	SEG118	1220.3	575.5	24.1	128.0
297	SEG119	1178.8	575.5	24.1	128.0
298	SEG120	1137.3	575.5	24.1	128.0
299	SEG121	1095.8	575.5	24.1	128.0
300	SEG122	1054.3	575.5	24.1	128.0
301	SEG123	1012.8	575.5	24.1	128.0
302	SEG124	971.3	575.5	24.1	128.0
303	SEG125	929.8	575.5	24.1	128.0
304	SEG126	888.3	575.5	24.1	128.0
305	SEG127	846.8	575.5	24.1	128.0
306	SEG128	805.3	575.5	24.1	128.0
307	SEG129	763.8	575.5	24.1	128.0
308	SEG130	722.3	575.5	24.1	128.0
309	SEG131	680.8	575.5	24.1	128.0
310	SEG132	639.3	575.5	24.1	128.0
311	SEG133	597.8	575.5	24.1	128.0
312	SEG134	556.3	575.5	24.1	128.0
313	SEG135	514.8	575.5	24.1	128.0
314	SEG136	473.3	575.5	24.1	128.0

Pin	Name	X	Y	W	H
315	SEG137	431.8	575.5	24.1	128.0
316	SEG138	390.3	575.5	24.1	128.0
317	SEG139	348.8	575.5	24.1	128.0
318	SEG140	307.3	575.5	24.1	128.0
319	SEG141	265.8	575.5	24.1	128.0
320	SEG142	224.3	575.5	24.1	128.0
321	SEG143	182.8	575.5	24.1	128.0
322	SEG144	141.3	575.5	24.1	128.0
323	SEG145	99.8	575.5	24.1	128.0
324	SEG146	58.3	575.5	24.1	128.0
325	SEG147	16.8	575.5	24.1	128.0
326	SEG148	-24.8	575.5	24.1	128.0
327	SEG149	-66.3	575.5	24.1	128.0
328	SEG150	-107.8	575.5	24.1	128.0
329	SEG151	-149.3	575.5	24.1	128.0
330	SEG152	-190.8	575.5	24.1	128.0
331	SEG153	-232.3	575.5	24.1	128.0
332	SEG154	-273.8	575.5	24.1	128.0
333	SEG155	-315.3	575.5	24.1	128.0
334	SEG156	-356.8	575.5	24.1	128.0
335	SEG157	-398.3	575.5	24.1	128.0
336	SEG158	-439.8	575.5	24.1	128.0
337	SEG159	-481.3	575.5	24.1	128.0
338	SEG160	-522.8	575.5	24.1	128.0
339	SEG161	-564.3	575.5	24.1	128.0
340	SEG162	-605.8	575.5	24.1	128.0
341	SEG163	-647.3	575.5	24.1	128.0
342	SEG164	-688.8	575.5	24.1	128.0
343	SEG165	-730.3	575.5	24.1	128.0
344	SEG166	-771.8	575.5	24.1	128.0
345	SEG167	-813.3	575.5	24.1	128.0
346	SEG168	-854.8	575.5	24.1	128.0
347	SEG169	-896.3	575.5	24.1	128.0
348	SEG170	-937.8	575.5	24.1	128.0
349	SEG171	-979.3	575.5	24.1	128.0
350	SEG172	-1020.8	575.5	24.1	128.0
351	SEG173	-1062.3	575.5	24.1	128.0
352	SEG174	-1103.8	575.5	24.1	128.0
353	SEG175	-1145.3	575.5	24.1	128.0
354	SEG176	-1186.8	575.5	24.1	128.0
355	SEG177	-1228.3	575.5	24.1	128.0
356	SEG178	-1269.8	575.5	24.1	128.0
357	SEG179	-1311.3	575.5	24.1	128.0
358	SEG180	-1352.8	575.5	24.1	128.0
359	SEG181	-1394.3	575.5	24.1	128.0
360	SEG182	-1435.8	575.5	24.1	128.0
361	SEG183	-1477.3	575.5	24.1	128.0
362	SEG184	-1518.8	575.5	24.1	128.0
363	SEG185	-1560.3	575.5	24.1	128.0
364	SEG186	-1601.8	575.5	24.1	128.0
365	SEG187	-1643.3	575.5	24.1	128.0
366	SEG188	-1684.8	575.5	24.1	128.0
367	SEG189	-1726.3	575.5	24.1	128.0
368	SEG190	-1767.8	575.5	24.1	128.0
369	SEG191	-1809.3	575.5	24.1	128.0
370	SEG192	-1850.8	575.5	24.1	128.0
371	SEG193	-1892.3	575.5	24.1	128.0
372	SEG194	-1933.8	575.5	24.1	128.0
373	SEG195	-1975.3	575.5	24.1	128.0
374	SEG196	-2016.8	575.5	24.1	128.0
375	SEG197	-2058.3	575.5	24.1	128.0
376	SEG198	-2099.8	575.5	24.1	128.0
377	SEG199	-2141.3	575.5	24.1	128.0
378	SEG200	-2182.8	575.5	24.1	128.0

Pin	Name	X	Y	W	H
379	SEG201	-2224.3	575.5	24.1	128.0
380	SEG202	-2265.8	575.5	24.1	128.0
381	SEG203	-2307.3	575.5	24.1	128.0
382	SEG204	-2348.8	575.5	24.1	128.0
383	SEG205	-2390.3	575.5	24.1	128.0
384	SEG206	-2431.8	575.5	24.1	128.0
385	SEG207	-2473.3	575.5	24.1	128.0
386	SEG208	-2514.8	575.5	24.1	128.0
387	SEG209	-2556.3	575.5	24.1	128.0
388	SEG210	-2597.8	575.5	24.1	128.0
389	SEG211	-2639.3	575.5	24.1	128.0
390	SEG212	-2680.8	575.5	24.1	128.0
391	SEG213	-2722.3	575.5	24.1	128.0
392	SEG214	-2763.8	575.5	24.1	128.0
393	SEG215	-2805.3	575.5	24.1	128.0
394	SEG216	-2846.8	575.5	24.1	128.0
395	SEG217	-2888.3	575.5	24.1	128.0
396	SEG218	-2929.8	575.5	24.1	128.0
397	SEG219	-2971.3	575.5	24.1	128.0
398	SEG220	-3012.8	575.5	24.1	128.0
399	SEG221	-3054.3	575.5	24.1	128.0
400	SEG222	-3095.8	575.5	24.1	128.0
401	SEG223	-3137.3	575.5	24.1	128.0
402	SEG224	-3178.8	575.5	24.1	128.0
403	SEG225	-3220.3	575.5	24.1	128.0
404	SEG226	-3261.8	575.5	24.1	128.0
405	SEG227	-3303.3	575.5	24.1	128.0
406	SEG228	-3344.8	575.5	24.1	128.0
407	SEG229	-3386.3	575.5	24.1	128.0
408	SEG230	-3427.8	575.5	24.1	128.0
409	SEG231	-3469.3	575.5	24.1	128.0
410	SEG232	-3510.8	575.5	24.1	128.0
411	SEG233	-3552.3	575.5	24.1	128.0
412	SEG234	-3593.8	575.5	24.1	128.0
413	SEG235	-3635.3	575.5	24.1	128.0
414	SEG236	-3676.8	575.5	24.1	128.0
415	SEG237	-3718.3	575.5	24.1	128.0
416	SEG238	-3759.8	575.5	24.1	128.0
417	SEG239	-3801.3	575.5	24.1	128.0
418	SEG240	-3842.8	575.5	24.1	128.0
419	SEG241	-3884.3	575.5	24.1	128.0
420	SEG242	-3925.8	575.5	24.1	128.0
421	SEG243	-3967.3	575.5	24.1	128.0
422	SEG244	-4008.8	575.5	24.1	128.0
423	SEG245	-4050.3	575.5	24.1	128.0
424	SEG246	-4091.8	575.5	24.1	128.0
425	SEG247	-4133.3	575.5	24.1	128.0
426	SEG248	-4174.8	575.5	24.1	128.0
427	SEG249	-4216.3	575.5	24.1	128.0
428	SEG250	-4257.8	575.5	24.1	128.0
429	SEG251	-4299.3	575.5	24.1	128.0
430	SEG252	-4340.8	575.5	24.1	128.0
431	SEG253	-4382.3	575.5	24.1	128.0
432	SEG254	-4423.8	575.5	24.1	128.0
433	SEG255	-4465.3	575.5	24.1	128.0
434	SEG256	-4506.8	575.5	24.1	128.0
435	SEG257	-4548.3	575.5	24.1	128.0
436	SEG258	-4589.8	575.5	24.1	128.0
437	SEG259	-4631.3	575.5	24.1	128.0
438	SEG260	-4672.8	575.5	24.1	128.0
439	SEG261	-4714.3	575.5	24.1	128.0
440	SEG262	-4755.8	575.5	24.1	128.0
441	SEG263	-4797.3	575.5	24.1	128.0
442	SEG264	-4838.8	575.5	24.1	128.0

Pin	Name	X	Y	W	H
443	SEG265	-4880.3	575.5	24.1	128.0
444	SEG266	-4921.8	575.5	24.1	128.0
445	SEG267	-4963.3	575.5	24.1	128.0
446	SEG268	-5004.8	575.5	24.1	128.0
447	SEG269	-5046.3	575.5	24.1	128.0
448	SEG270	-5087.8	575.5	24.1	128.0
449	SEG271	-5129.3	575.5	24.1	128.0
450	SEG272	-5170.8	575.5	24.1	128.0
451	SEG273	-5212.3	575.5	24.1	128.0
452	SEG274	-5253.8	575.5	24.1	128.0
453	SEG275	-5295.3	575.5	24.1	128.0
454	SEG276	-5336.8	575.5	24.1	128.0
455	SEG277	-5378.3	575.5	24.1	128.0
456	SEG278	-5419.8	575.5	24.1	128.0
457	SEG279	-5461.3	575.5	24.1	128.0
458	SEG280	-5502.8	575.5	24.1	128.0
459	SEG281	-5544.3	575.5	24.1	128.0
460	SEG282	-5585.8	575.5	24.1	128.0
461	SEG283	-5627.3	575.5	24.1	128.0
462	SEG284	-5668.8	575.5	24.1	128.0
463	SEG285	-5710.3	575.5	24.1	128.0
464	SEG286	-5751.8	575.5	24.1	128.0
465	SEG287	-5793.3	575.5	24.1	128.0
466	SEG288	-5834.8	575.5	24.1	128.0
467	SEG289	-5876.3	575.5	24.1	128.0
468	SEG290	-5917.8	575.5	24.1	128.0
469	SEG291	-5959.3	575.5	24.1	128.0
470	SEG292	-6000.8	575.5	24.1	128.0
471	SEG293	-6042.3	575.5	24.1	128.0
472	SEG294	-6083.8	575.5	24.1	128.0
473	COM2	-6125.3	575.5	24.1	128.0
474	COM4	-6166.8	575.5	24.1	128.0
475	COM6	-6208.3	575.5	24.1	128.0

TRAY INFORMATION



Unless Otherwise Specified	Unit	mm
General Roughness	N/A	
Tolerance	2" IC Tray Type: H20-522x65-28(45)	
Dimension drawing detail	see drawing detail	
Angle	N/A	

ULTRACHIP inc. 晶宏半導體		
Scale	N/A	Proj.
Package Code		
Material		
Drawn	Checked	Approved
By: Jack Chung	Alvin	Alvin
Date: 9-17-03	9-18-03	9-18-03
Drawing No.		Rev.
		A
Sheet	1 of 1	Size A4

REVISION HISTORY

Revision	Contents	Date of Rev.
0.6	Golden release	Jul. 21, 2004
0.8	(1) Some ESD related content is removed (and placed in the ESD section). (Section "Pin Description" - Note, page 6)	Aug. 12, 2004
	(2) The fine-tuning rate of line rate is adjusted: (OTPM[7:6]) 01: -6% → -10% 10: +6% → +10% 11: no change → +20% (Section "Command Description" - (38) Set OTP Write Mask, page 26; Section "OTP Operation for LCM Makers", page 49)	
	(3) V_{LCD} formula is updated. (Section " V_{LCD} Quick Reference", page 29)	
	(4) One note is added on OTP programming. (Section "OTP Operation for LCM Makers", page 48)	
	(5) A new section is inserted. (Section "ESD Consideration", page 54)	
0.9	(1) The V_{LCD} formula is updated. (Section " V_{LCD} Quick Reference", page 29)	Aug. 16, 2004
1.0	(1) A sentence on SL range is removed. (Section "Command Description" – (8) Set Scroll Line, page 14)	Oct. 7, 2004
	(2) Some Dither and non-dither bit contents are corrected. (Section "Command Description" – (22) Set Input Color Mode, Pp 19-20)	
	(3) Machine Mode data are provided. (Section "ESD Consideration", page 54)	
	(4) One more description is added: "All HV outputs are open circuit." (Section "Specifications" – Power Consumption, page 56)	