

PRODUCT : LCD MODULE
SUPPLIER : TRULY SEMICONDUCTORS LTD.



CERT. No.QAC0946535 (ISO9001) CERT. No.HKG002005 (ISO14001)

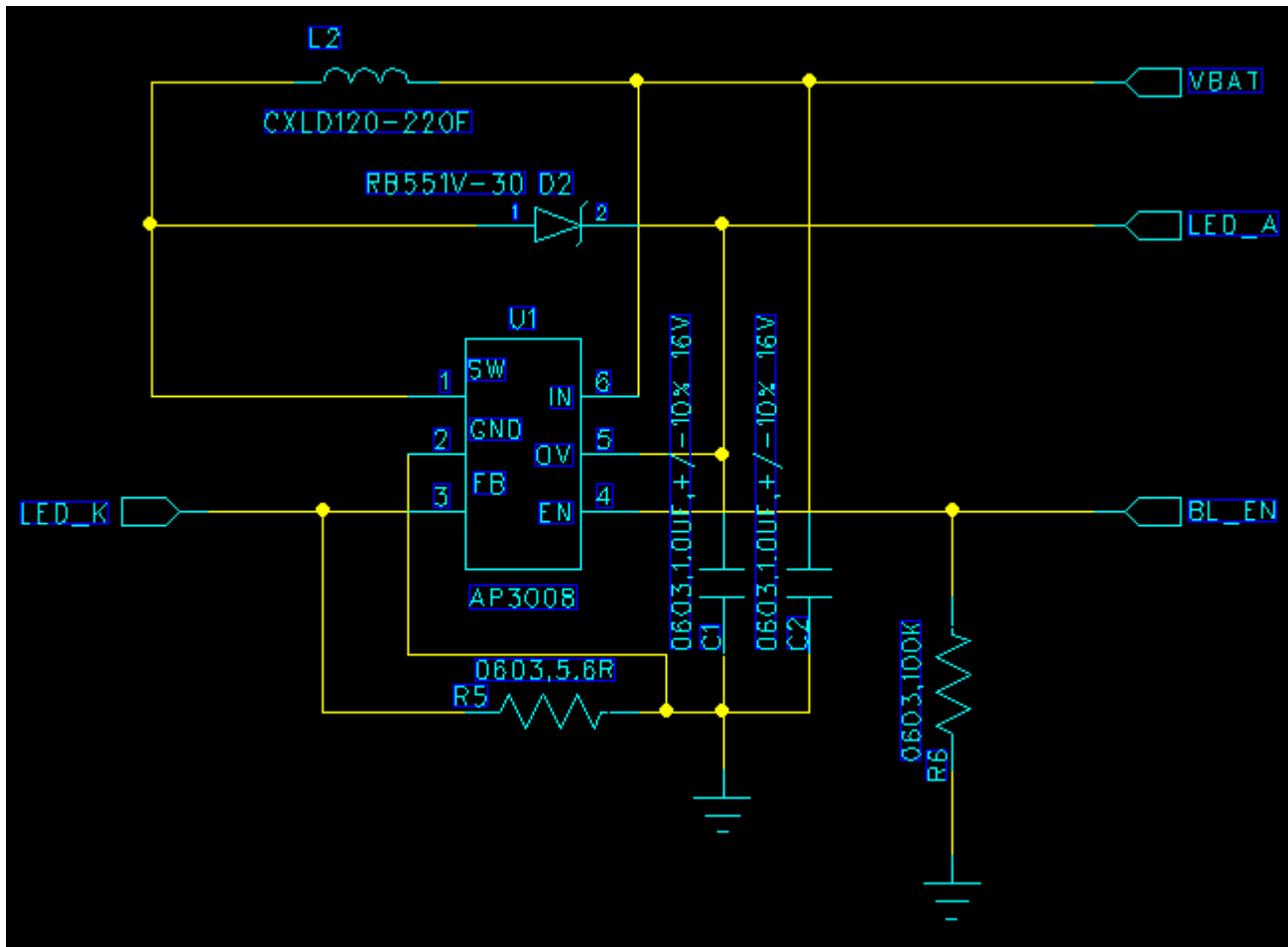
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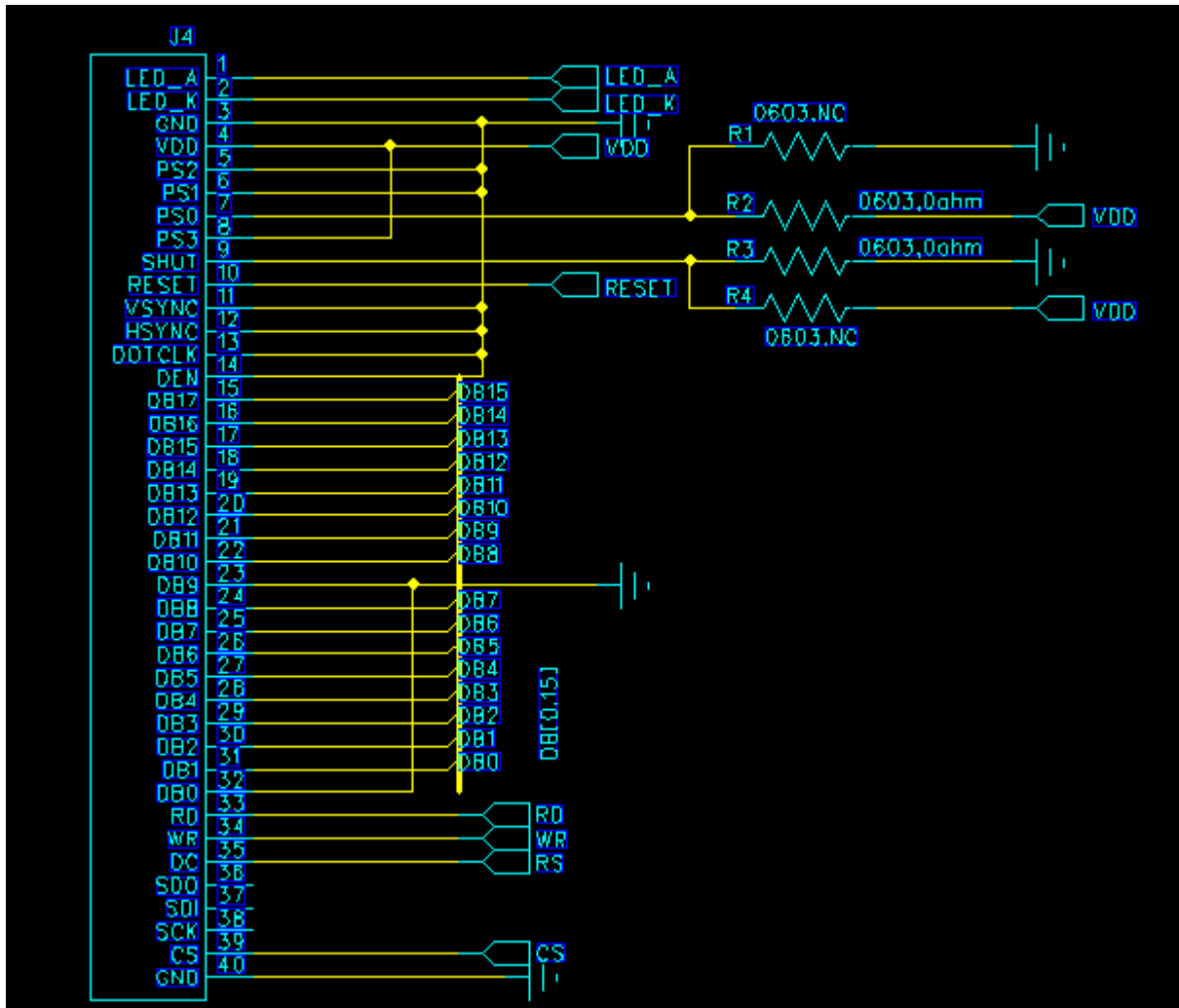
APPLICATION NOTE

This application note is only for reference and maybe changed without any notice .
Please contact TRULY R&D department for update files and product status before design for this product or release the order.

WRITTEN BY	APPROVED BY
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■ APPLICATION CIRCUIT



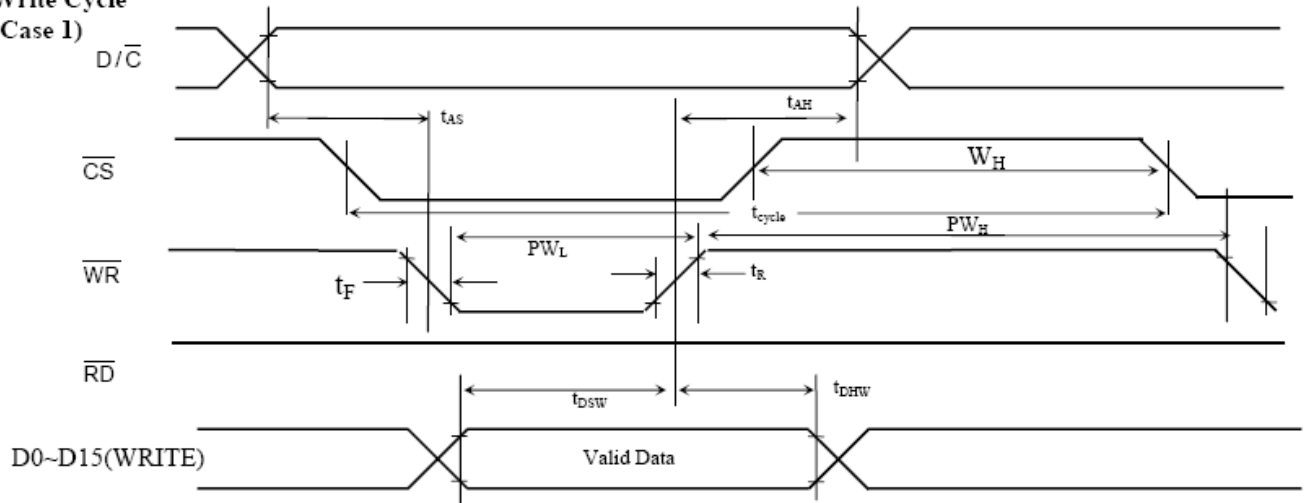


■ TIMING CHART OF INPUT SIGNALS

($T_A = -20$ to 70°C , $V_{DDIO} = 1.65\text{V}$ to 3.6V , $V_{DDEX} = 1.65\text{V}$ to 1.95V , $\text{REGVDD} = 'L'$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	100	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle)	1000	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Data Setup Time	5	-	-	ns
t_{DHW}	Data Hold Time	5	-	-	ns
t_{ACC}	Data Access Time	250	-	-	ns
t_{OH}	Output Hold time	100	-	-	ns
W_H	Width high	20	-	-	ns
PW_L	Pulse Width low (write cycle)	50	-	-	ns
PW_H	Pulse Width high (write cycle)	50	-	-	ns
PW_L	Pulse Width low (read cycle)	500	-	-	ns
PW_H	Pulse Width high (read cycle)	500	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

Write Cycle (Case 1)



Write Cycle (Case 2)

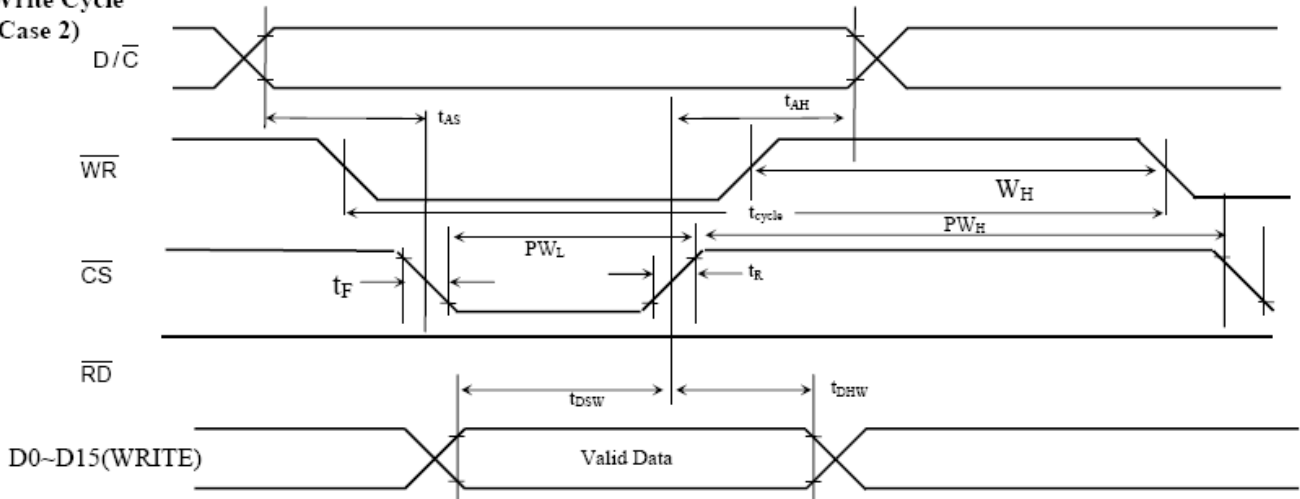


Table 13-3 - Serial Timing Characteristics

($T_A = -20$ to 70°C , $V_{DDIO} = 1.65\text{V}$ to 3.6V , $V_{DDEXT} = 1.65\text{V}$ to 1.95V , $\text{REGVDD} = 'L'$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	77	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	13	MHz
t_{AS}	Register select Setup Time	4	-	-	ns
t_{AH}	Register select Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	2	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	5	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	38	-	-	ns
t_{CLKH}	Clock High Time	38	-	-	ns
t_{R}	Rise time	-	-	4	ns
t_{F}	Fall time	-	-	4	ns

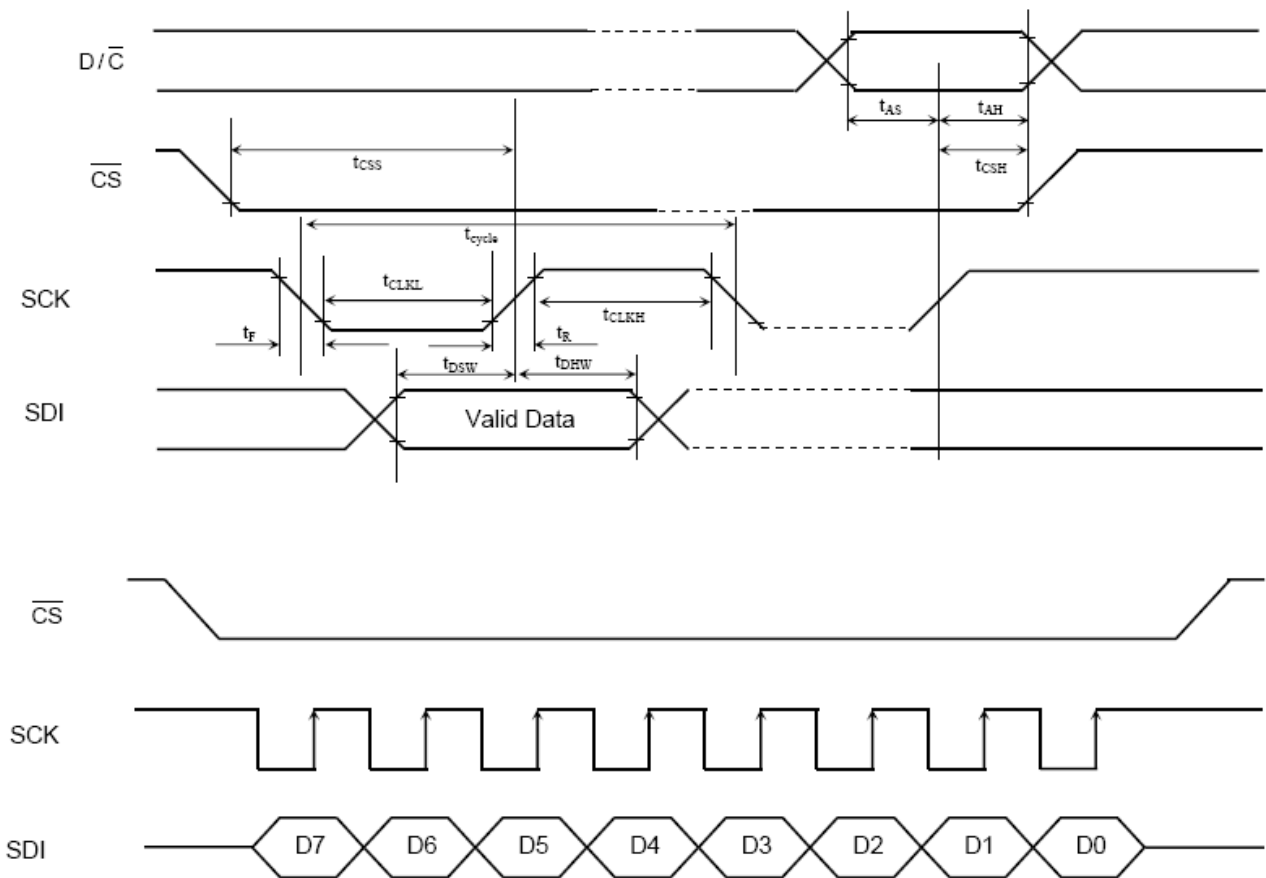
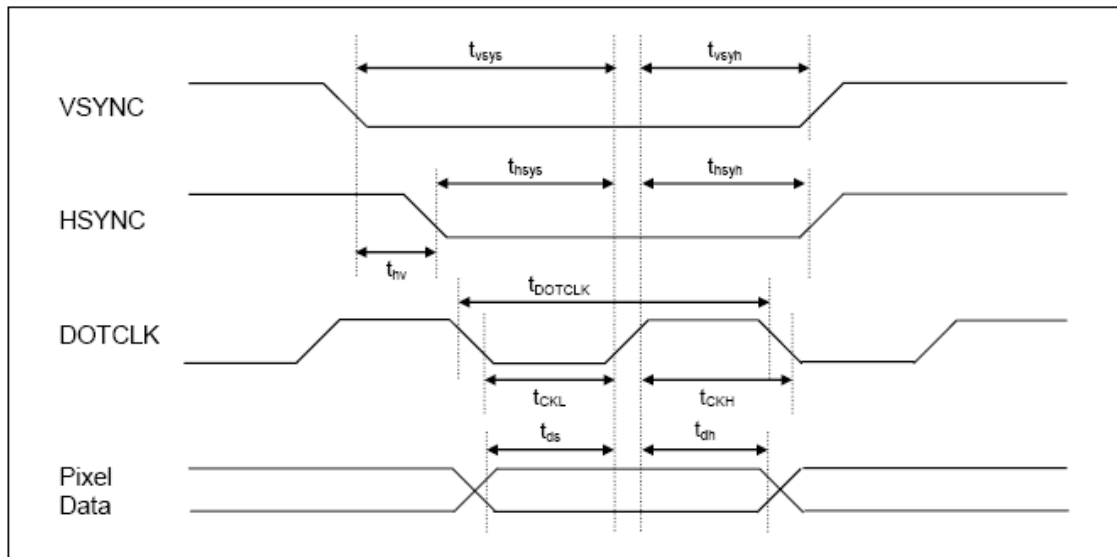
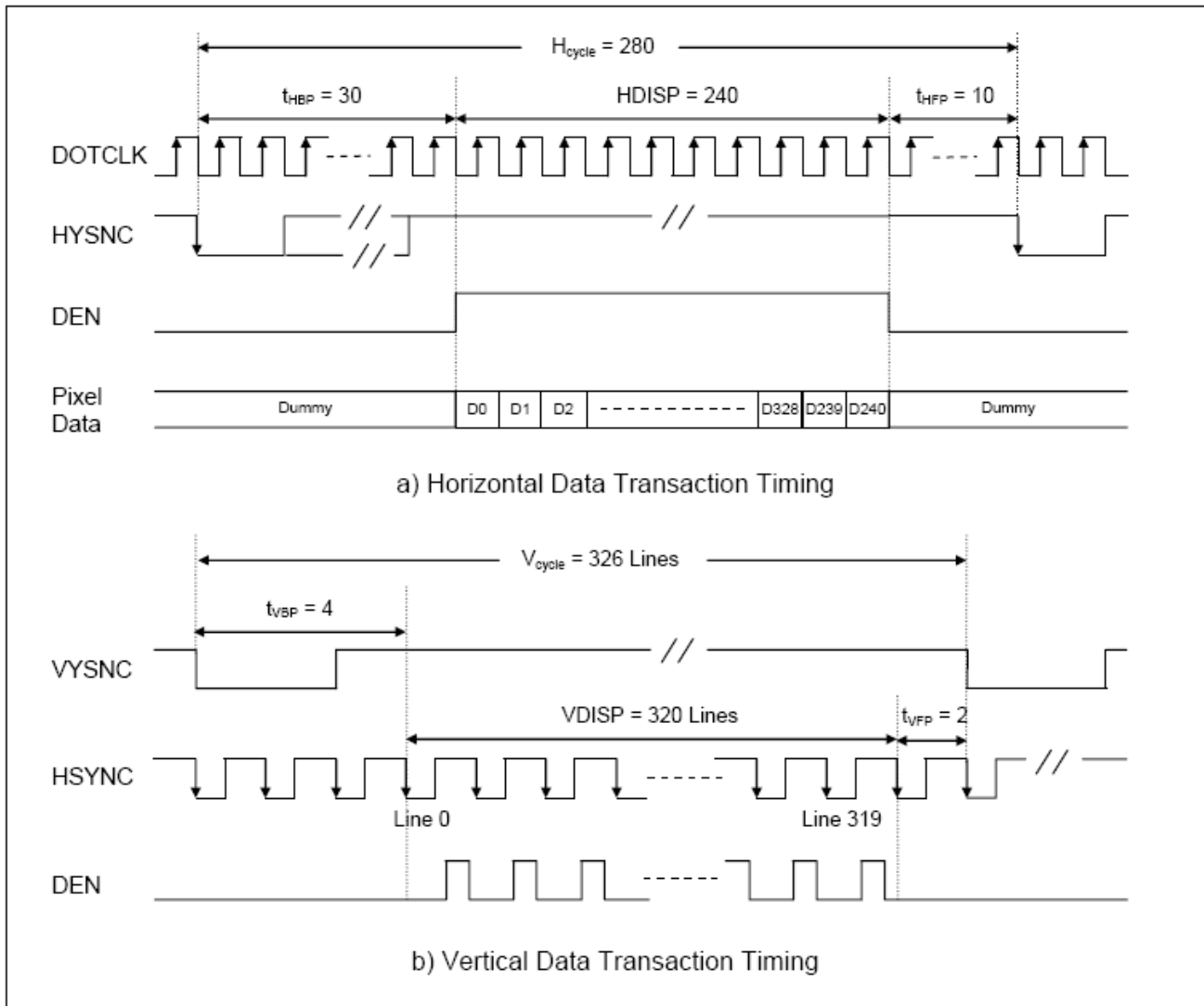


Figure 13-3 – 4 wire Serial Timing Characteristics

Figure 13-4 - Pixel Clock Timing in RGB interface mode



Characteristics	Symbol	Min	Typ	Max	Units
DOTCLK Frequency	f_{DOTCLK}	-	5.5	8.22	MHz
DOTCLK Period	t_{DOTCLK}	122	182	-	nSec
Vertical Sync Setup Time	t_{vsys}	20	-	-	nSec
Vertical Sync Hold Time	t_{vsyh}	20	-	-	nSec
Horizontal Sync Setup Time	t_{hsys}	20	-	-	nSec
Horizontal Sync Hold Time	t_{hsyh}	20	-	-	nSec
Phase difference of Sync Signal Falling Edge	t_{tiv}	0	-	240	t_{DOTCLK}
DOTCLK Low Period	t_{CKL}	61	-	-	nSec
DOTCLK High Period	t_{CKH}	61	-	-	nSec
Data Setup Time	t_{ds}	40	-	-	nSec
Data hold Time	t_{dh}	40	-	-	nSec

Figure 0-5 - Pixel Clock Timing in RGB interface mode


Characteristics	Symbol	Min	Typ	Max	Unit
DOTCLK Frequency	f_{DOTCLK}	-	5.5	8.22	MHz
DOTCLK Period	t_{DOTCLK}	122	182	-	nSec
Horizontal Frequency (Line)	f_H	-	19.6	29.3	kHz
Vertical Frequency (Refresh)	f_V	-	60	90	Hz
Horizontal Back Porch	t_{HBP}	-	30	-	t_{DOTCLK}
Horizontal Front Porch	t_{HFP}	-	10	-	t_{DOTCLK}
Horizontal Data Start Point	t_{HBP}	-	30	-	t_{DOTCLK}
Horizontal Blanking Period	$t_{HBP} + t_{HFP}$	-	40	-	t_{DOTCLK}
Horizontal Display Area	H_{DISP}	-	240	-	t_{DOTCLK}
Horizontal Cycle	H_{cycle}	-	280	-	t_{DOTCLK}
Vertical Back Porch	t_{VBP}	-	4	-	Line
Vertical Front Porch	t_{VFP}	-	2	-	Line
Vertical Data Start Point	t_{VBP}	-	4	-	Line
Vertical Blanking Period	$t_{VBP} + t_{VFP}$	-	6	-	Line
Vertical Display Area	V_{DISP}	-	320	-	Line
Vertical Cycle	V_{cycle}	-	326	-	Line

PS3	PS2	PS1	PS0	Interface Mode
1	1	1	1	3-wire SPI
1	1	1	0	4-wire SPI
1	0	1	1	16-bit 6800 parallel interface
1	0	1	0	8-bit 6800 parallel interface
1	0	0	1	16-bit 8080 parallel interface
1	0	0	0	8-bit 8080 parallel interface
0	1	1	1	18-bits 6800 parallel interface
0	1	1	0	9-bits 6800 parallel interface
0	1	0	1	18-bit 8080 parallel interface
0	1	0	0	9-bit 8080 parallel interface
0	0	1	1	Reserved
0	0	1	0	Reserved
0	0	0	1	18-bit RGB interface + 4-wire SPI

For more information please refer to SSD1289 data sheet.

The TFT panel is different between new module and old module

■ INITIAL CODE

```
//PS3=1;PS2=0;PS1=0;PS0=1;
```

```
//VCC=IOVCC=2.8V;
```

```
M_RESET = 1; Delayms(20);//Delay 20 ms
```

```
M_RESET = 0; Delayms(100);
```

```
M_RESET = 1; Delayms(100);
```

```
Delayms(10);
```

```
WMLCDCOM(0x0028);WMLCDDATA(0x0006);
```

```
WMLCDCOM(0x0000);WMLCDDATA(0x0001);
```

```
Delayms(15);
```

```
WMLCDCOM(0x002B);WMLCDDATA(0x9532);
```

```
WMLCDCOM(0x0003);WMLCDDATA(0xAAAC);
```

```
WMLCDCOM(0x000C);WMLCDDATA(0x0002);
```

```
WMLCDCOM(0x000D);WMLCDDATA(0x000A);
```

```
WMLCDCOM(0x000E);WMLCDDATA(0x2C00);
```

```
WMLCDCOM(0x001E);WMLCDDATA(0x00AA);//different from old code
```

```
WMLCDCOM(0x0025);WMLCDDATA(0x8000);
```

```
Delayms(15);
```

```
WMLCDCOM(0x0001);WMLCDDATA(0x2B3F);
```

```
WMLCDCOM(0x0002);WMLCDDATA(0x0600);
```

```
WMLCDCOM(0x0010);WMLCDDATA(0x0000);
```

```
WMLCDCOM(0x0011);WMLCDDATA(0x60B0);
```

```
Delayms(20);
```

```
WMLCDCOM(0x0005);WMLCDDATA(0x0000);
```

```
WMLCDCOM(0x0006);WMLCDDATA(0x0000);
```

```
WMLCDCOM(0x0016);WMLCDDATA(0xEF1C);
```

```
WMLCDCOM(0x0017);WMLCDDATA(0x0003);
WMLCDCOM(0x0007);WMLCDDATA(0x0233);
WMLCDCOM(0x000B);WMLCDDATA(0x5312);
WMLCDCOM(0x000F);WMLCDDATA(0x0000);
Delaysms(20);
WMLCDCOM(0x0041);WMLCDDATA(0x0000);
WMLCDCOM(0x0042);WMLCDDATA(0x0000);
WMLCDCOM(0x0048);WMLCDDATA(0x0000);
WMLCDCOM(0x0049);WMLCDDATA(0x013F);
WMLCDCOM(0x0044);WMLCDDATA(0xEF00);
WMLCDCOM(0x0045);WMLCDDATA(0x0000);
WMLCDCOM(0x0046);WMLCDDATA(0x013F);
WMLCDCOM(0x004A);WMLCDDATA(0x0000);
WMLCDCOM(0x004B);WMLCDDATA(0x0000);
Delaysms(20);
WMLCDCOM(0x0030);WMLCDDATA(0x0707);
WMLCDCOM(0x0031);WMLCDDATA(0x0704);
WMLCDCOM(0x0032);WMLCDDATA(0x0204);
WMLCDCOM(0x0033);WMLCDDATA(0x0201);
WMLCDCOM(0x0034);WMLCDDATA(0x0203);
WMLCDCOM(0x0035);WMLCDDATA(0x0204);
WMLCDCOM(0x0036);WMLCDDATA(0x0204);
WMLCDCOM(0x0037);WMLCDDATA(0x0502);
WMLCDCOM(0x003A);WMLCDDATA(0x0302);
WMLCDCOM(0x003B);WMLCDDATA(0x0500);
Delaysms(20);
WMLCDCOM(0x0022);
```

■ OLD INITIAL CODE

```
//PS3=1;PS2=0;PS1=0;PS0=1;
//VCC=IOVCC=2.8V;
```

```
M_RESET = 1; Delaysms(20);//Delay 20 ms
M_RESET = 0; Delaysms(100);
M_RESET = 1; Delaysms(100);
```

```
Delaysms(10);
WMLCDCOM(0x0028);WMLCDDATA(0x0006);
WMLCDCOM(0x0000);WMLCDDATA(0x0001);
Delaysms(15);
WMLCDCOM(0x002B);WMLCDDATA(0x9532);
WMLCDCOM(0x0003);WMLCDDATA(0xAAAC);
WMLCDCOM(0x000C);WMLCDDATA(0x0002);
WMLCDCOM(0x000D);WMLCDDATA(0x000A);
WMLCDCOM(0x000E);WMLCDDATA(0x2C00);
WMLCDCOM(0x001E);WMLCDDATA(0x00B8);//different from new code
WMLCDCOM(0x0025);WMLCDDATA(0x8000);
Delaysms(15);
WMLCDCOM(0x0001);WMLCDDATA(0x2B3F);
WMLCDCOM(0x0002);WMLCDDATA(0x0600);
WMLCDCOM(0x0010);WMLCDDATA(0x0000);
WMLCDCOM(0x0011);WMLCDDATA(0x60B0);
```

Delaysms(20);

WMLCDCOM(0x0005);WMLCDDATA(0x0000);
WMLCDCOM(0x0006);WMLCDDATA(0x0000);
WMLCDCOM(0x0016);WMLCDDATA(0xEF1C);
WMLCDCOM(0x0017);WMLCDDATA(0x0003);
WMLCDCOM(0x0007);WMLCDDATA(0x0233);
WMLCDCOM(0x000B);WMLCDDATA(0x5312);
WMLCDCOM(0x000F);WMLCDDATA(0x0000);

Delaysms(20);

WMLCDCOM(0x0041);WMLCDDATA(0x0000);
WMLCDCOM(0x0042);WMLCDDATA(0x0000);
WMLCDCOM(0x0048);WMLCDDATA(0x0000);
WMLCDCOM(0x0049);WMLCDDATA(0x013F);
WMLCDCOM(0x0044);WMLCDDATA(0xEF00);
WMLCDCOM(0x0045);WMLCDDATA(0x0000);
WMLCDCOM(0x0046);WMLCDDATA(0x013F);
WMLCDCOM(0x004A);WMLCDDATA(0x0000);
WMLCDCOM(0x004B);WMLCDDATA(0x0000);

Delaysms(20);

WMLCDCOM(0x0030);WMLCDDATA(0x0707);
WMLCDCOM(0x0031);WMLCDDATA(0x0704);
WMLCDCOM(0x0032);WMLCDDATA(0x0204);
WMLCDCOM(0x0033);WMLCDDATA(0x0201);
WMLCDCOM(0x0034);WMLCDDATA(0x0203);
WMLCDCOM(0x0035);WMLCDDATA(0x0204);
WMLCDCOM(0x0036);WMLCDDATA(0x0204);
WMLCDCOM(0x0037);WMLCDDATA(0x0502);
WMLCDCOM(0x003A);WMLCDDATA(0x0302);
WMLCDCOM(0x003B);WMLCDDATA(0x0500);

Delaysms(20);

WMLCDCOM(0x0022);