SSD2128

Product Preview

480 x 272 RGB TFT LCD Driver
Integrated Power Circuit, Gate and Source Driver

Appendi1: IC Revision history of SSD2128 Specification

Version	Change Items	Effective Date
0.10	1st Release	28-Oct-09

CONTENTS

TABLES

FIGURES

1 GENERAL DESCRIPTION

SSD2128 is an all in one driver that integrated the power circuits, gate driver and source driver into single chip. It can drive a 16.7M/262k a-TFT panel with resolution of 480 x 272 RGB.

SSD2128 embeds DC-DC Converter and Voltage generator to provide all necessary voltage required by the driver with minimum external components. A Common Voltage Generation Circuit is included to drive the TFT-display counter electrode. The driver supports three separated RGB Gamma settings. An Integrated Gamma Control Circuit is also included that can be adjusted by software commands to provide maximum flexibility and optimal display quality.

SSD2128 can be operated down to 2.5V (VCI) and provide different power save modes. It is suitable for any portable battery-driven applications requiring long operation period with compact size.

2 FEATURES

- 480 x 272 RGB single chip controller driver IC for 16.7M/262k amorphous TFT LCD
- RGB color filter arrangement at Gate
- Power Supply
  - VDDIO = 1.6V – 3.3V (I/O Interface)
  - VCI = 2.5V – 3.3V (power supply for internal analog circuit)
- Output Voltages
  - Gate Driver:
    - VGH-GND = 6V ~ 18V
    - VGL-GND = -9V ~ -15V
    - VGH-VGL < 32Vp-p
  - Source Driver:
    - Source = AVDD ~ AVDDM
    - Typical Source Output Voltage variation: ±30 mV
  - VCOMDC drive:
    - VCOMDC from = 0V ~ -2.55V
    - VCOMDC in ~10mV resolution steps
- System Interface
  - Serial Peripheral Interface (SPI), 3 wire (9bit), 4 wire and SPID 24 bit interface
- Video interface
  - 24-bit RGB interface (DEN, DOTCLK, HSYNC, VSYNC, RR[7:0], BB[7:0], GG[7:0])
  - 8-bit serial RGB interface
- Support low power consumption:
  - Low voltage supply
  - Low current sleep mode
  - Charge sharing function for source
- Internal power supply circuit
  - Voltage generator
  - DC-DC converter up to +18/-12 or +15/-15 (VGH - VGL < 32V)
  - AV_{DD} generator of 2x or 3x of V_{CI}
- Support separate RGB gamma control
- Support dynamic backlight control
- Support IPS Panel
- Support DC-VCOM
- Support dot / column inversion
- Support Charge re-cycling at Source
- TFT storage capacitance: Cs on common
- Support source and gate scan direction control
- Built-in 1k bits Non Volatile Memory
- MTP of VCOM and module ID
- SHUT actice HIGH / LOW selectable

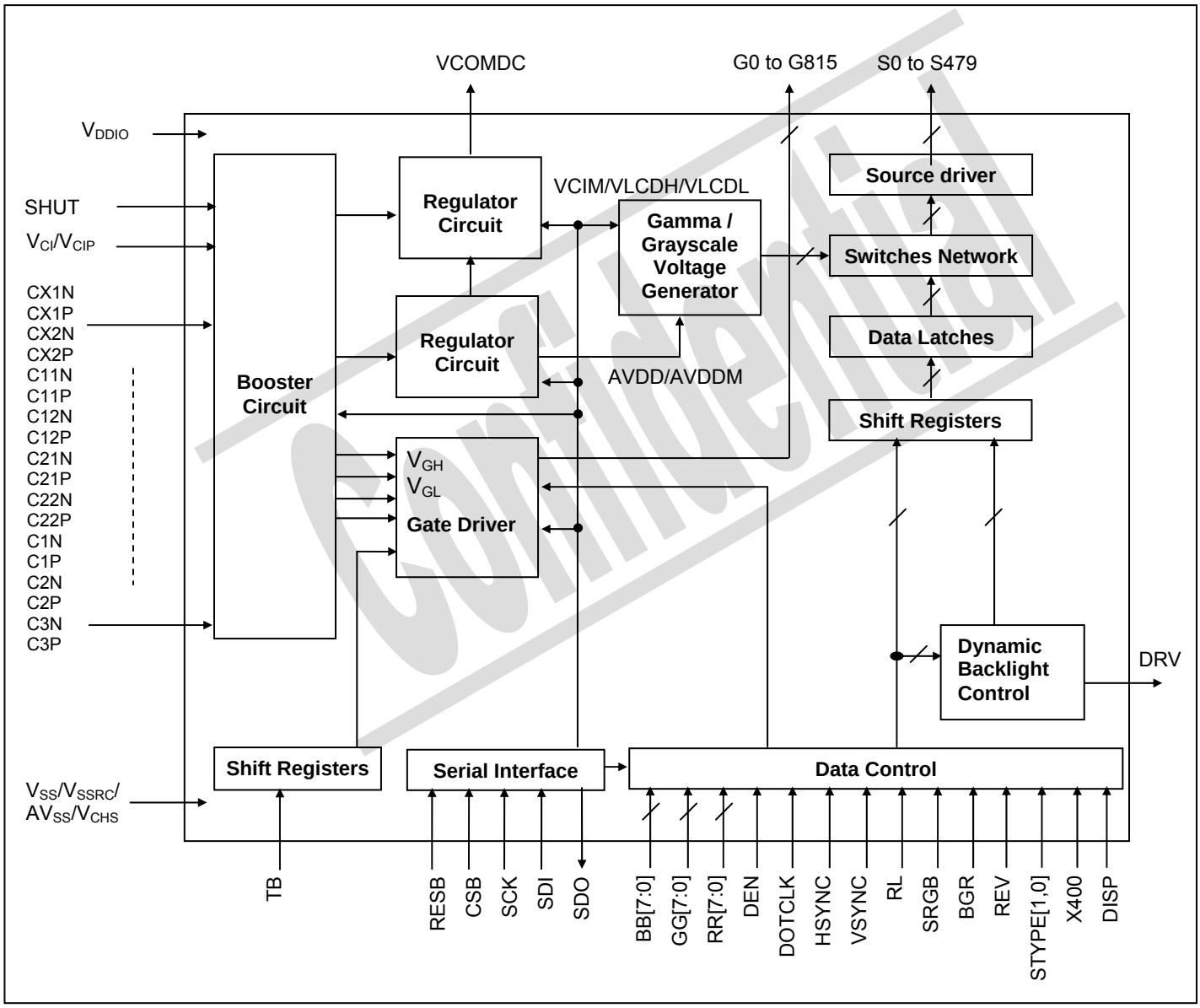
3 ORDERING INFORMATION

Table 3-1: Ordering Information

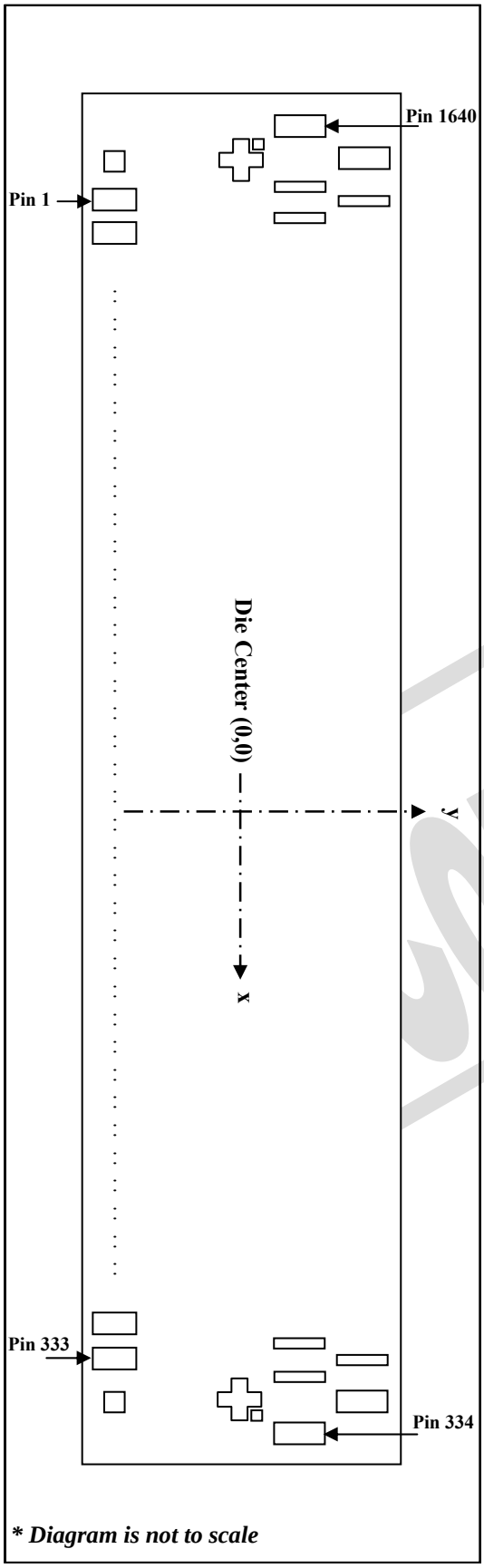
Ordering Part Number	Package Form
SSD2128Z	COG

4 BLOCK DIAGRAM

Figure 4-1: Block Diagram

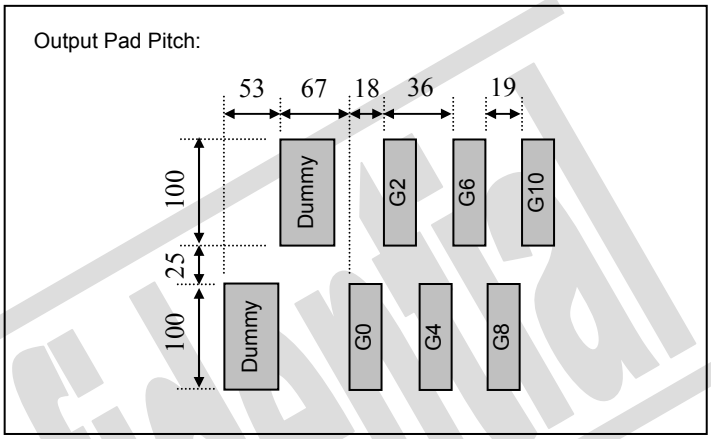


5 DIE PAD FLOOR PLAN



Die Information:

Die Size:	23850± 50 x 700± 50um (after sawing)" μm^2
Die Thickness:	270 ± 25μm
Bump Height:	12 μm (Typ.)
Bump Co-planarity:	≤ 2 μm within die
Bump Size 1:	50 x 80 μm^2 (IO pad, Pad 1-333)
Pad Pitch 1:	70 μm
Bump Size 2:	50 x 100 μm^2 (Dummy pad, Pad 334-335, 1639-1640)
Pad Pitch 2:	53 μm
Bump Size 3:	17 x 100 μm^2 (G/S pad, Pad 336-1638)
Pad Pitch 3:	18 μm



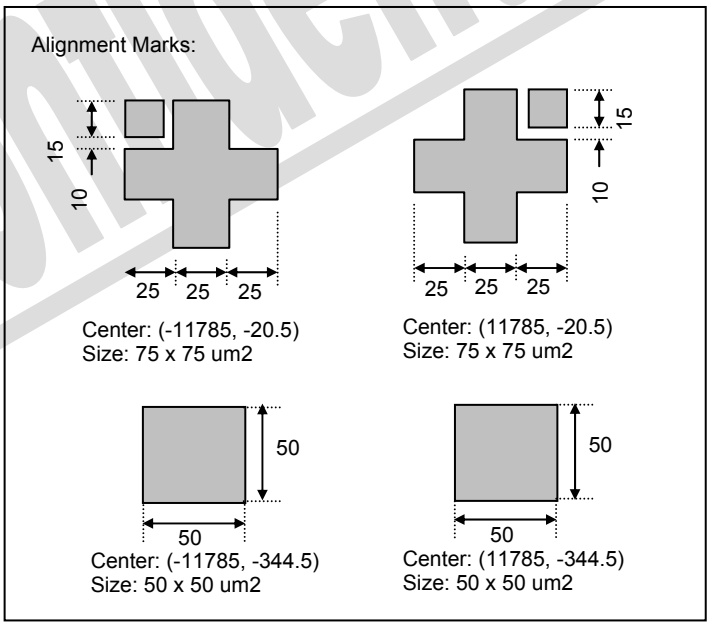


Figure 5-1 - Die Floor Plan (Bump face up)

Table 5-1: SSD2128 Bump Die Pad Coordinates (Bump Centre)

Note: IC material temperature expansion factor is 2.6ppm per degree, customer should take into account during panel design.

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
1	NC	-11620	-344.5	65	VCI	-7140	-344.5	129	C21N	-2660	-344.5	193	CX2N	1820	-344.5
2	NC	-11550	-344.5	66	VCI	-7070	-344.5	130	C21N	-2590	-344.5	194	CX2N	1890	-344.5
3	VLCDH	-11480	-344.5	67	VCI	-7000	-344.5	131	C21N	-2520	-344.5	195	CX2N	1960	-344.5
4	VLCDH	-11410	-344.5	68	VCI	-6930	-344.5	132	C21N	-2450	-344.5	196	NC	2030	-344.5
5	VLCDL	-11340	-344.5	69	VCI	-6860	-344.5	133	C21N	-2380	-344.5	197	VCI	2100	-344.5
6	VLCDL	-11270	-344.5	70	AVDD	-6790	-344.5	134	AVDDM	-2310	-344.5	198	VCI	2170	-344.5
7	AVSS	-11200	-344.5	71	AVDD	-6720	-344.5	135	AVDDM	-2240	-344.5	199	VCI	2240	-344.5
8	AVSS	-11130	-344.5	72	AVDD	-6650	-344.5	136	AVDDM	-2170	-344.5	200	VCI	2310	-344.5
9	AVSS	-11060	-344.5	73	AVDD	-6580	-344.5	137	AVDDM	-2100	-344.5	201	VSS	2380	-344.5
10	AVSS	-10990	-344.5	74	AVDD	-6510	-344.5	138	C22P	-2030	-344.5	202	NC	2450	-344.5
11	VSSRC	-10920	-344.5	75	AVDD	-6440	-344.5	139	C22P	-1960	-344.5	203	NC	2520	-344.5
12	VSSRC	-10850	-344.5	76	AVDD	-6370	-344.5	140	C22P	-1890	-344.5	204	NC	2590	-344.5
13	VCIP	-10780	-344.5	77	AVDD	-6300	-344.5	141	C22P	-1820	-344.5	205	NC	2660	-344.5
14	VCIP	-10710	-344.5	78	AVDD	-6230	-344.5	142	C22N	-1750	-344.5	206	NC	2730	-344.5
15	TESTA	-10640	-344.5	79	AVDD	-6160	-344.5	143	C22N	-1680	-344.5	207	NC	2800	-344.5
16	TESTB	-10570	-344.5	80	AVDD	-6090	-344.5	144	C22N	-1610	-344.5	208	VSS	2870	-344.5
17	VSS	-10500	-344.5	81	AVDD	-6020	-344.5	145	C22N	-1540	-344.5	209	NC	2940	-344.5
18	NC	-10430	-344.5	82	AVDD	-5950	-344.5	146	VCIM	-1470	-344.5	210	NC	3010	-344.5
19	NC	-10360	-344.5	83	C11P	-5880	-344.5	147	VCIM	-1400	-344.5	211	NC	3080	-344.5
20	NC	-10290	-344.5	84	C11P	-5810	-344.5	148	VCIM	-1330	-344.5	212	NC	3150	-344.5
21	NC	-10220	-344.5	85	C11P	-5740	-344.5	149	VCIM	-1260	-344.5	213	NC	3220	-344.5
22	NC	-10150	-344.5	86	C11P	-5670	-344.5	150	VCHS	-1190	-344.5	214	VSS	3290	-344.5
23	NC	-10080	-344.5	87	C11N	-5600	-344.5	151	VCHS	-1120	-344.5	215	VSS	3360	-344.5
24	VGL	-10010	-344.5	88	C11N	-5530	-344.5	152	VCHS	-1050	-344.5	216	VSS	3430	-344.5
25	VGL	-9940	-344.5	89	C11N	-5460	-344.5	153	VCHS	-980	-344.5	217	VSS	3500	-344.5
26	VGL	-9870	-344.5	90	C11N	-5390	-344.5	154	VCOMDC	-910	-344.5	218	NC	3570	-344.5
27	VGL	-9800	-344.5	91	VCHS	-5320	-344.5	155	VCOMDC	-840	-344.5	219	NC	3640	-344.5
28	C3P	-9730	-344.5	92	VCHS	-5250	-344.5	156	VCOMDC	-770	-344.5	220	DRV	3710	-344.5
29	C3P	-9660	-344.5	93	VCHS	-5180	-344.5	157	VCOMDC	-700	-344.5	221	DRV	3780	-344.5
30	C3P	-9590	-344.5	94	VCHS	-5110	-344.5	158	VCOMDC	-630	-344.5	222	DRV	3850	-344.5
31	C3P	-9520	-344.5	95	VCHS	-5040	-344.5	159	VCOMDC	-560	-344.5	223	VCORE	3920	-344.5
32	C3P	-9450	-344.5	96	VCHS	-4970	-344.5	160	VCOMDC	-490	-344.5	224	VCORE	3990	-344.5
33	C3P	-9380	-344.5	97	VCHS	-4900	-344.5	161	VCOMDC	-420	-344.5	225	VCORE	4060	-344.5
34	C3N	-9310	-344.5	98	VCHS	-4830	-344.5	162	CX1P	-350	-344.5	226	VCORE	4130	-344.5
35	C3N	-9240	-344.5	99	VCHS	-4760	-344.5	163	CX1P	-280	-344.5	227	VREGC	4200	-344.5
36	C3N	-9170	-344.5	100	C12P	-4690	-344.5	164	CX1P	-210	-344.5	228	VREGC	4270	-344.5
37	C3N	-9100	-344.5	101	C12P	-4620	-344.5	165	CX1P	-140	-344.5	229	VREGC	4340	-344.5
38	C3N	-9030	-344.5	102	C12P	-4550	-344.5	166	CX1P	-70	-344.5	230	VREGC	4410	-344.5
39	VGH	-8960	-344.5	103	C12P	-4480	-344.5	167	CX1P	0	-344.5	231	AVSS	4480	-344.5
40	VGH	-8890	-344.5	104	C12P	-4410	-344.5	168	CX1N	70	-344.5	232	AVSS	4550	-344.5
41	VGH	-8820	-344.5	105	C12P	-4340	-344.5	169	CX1N	140	-344.5	233	AVSS	4620	-344.5
42	VGH	-8750	-344.5	106	C12N	-4270	-344.5	170	CX1N	210	-344.5	234	VDDIO	4690	-344.5
43	VGH	-8680	-344.5	107	C12N	-4200	-344.5	171	CX1N	280	-344.5	235	VDDIO	4760	-344.5
44	C2P	-8610	-344.5	108	C12N	-4130	-344.5	172	CX1N	350	-344.5	236	VDDIO	4830	-344.5
45	C2P	-8540	-344.5	109	C12N	-4060	-344.5	173	CX1N	420	-344.5	237	DISP	4900	-344.5
46	C2P	-8470	-344.5	110	C12N	-3990	-344.5	174	CX2P	490	-344.5	238	B7	4970	-344.5
47	C2P	-8400	-344.5	111	C12N	-3920	-344.5	175	CX2P	560	-344.5	239	B6	5040	-344.5
48	C2N	-8330	-344.5	112	VCI	-3850	-344.5	176	CX2P	630	-344.5	240	B5	5110	-344.5
49	C2N	-8260	-344.5	113	VCI	-3780	-344.5	177	CX2P	700	-344.5	241	B4	5180	-344.5
50	C2N	-8190	-344.5	114	VCI	-3710	-344.5	178	CX2P	770	-344.5	242	B3	5250	-344.5
51	C2N	-8120	-344.5	115	VCI	-3640	-344.5	179	CX2P	840	-344.5	243	B2	5320	-344.5
52	C1P	-8050	-344.5	116	VCI	-3570	-344.5	180	CX2P	910	-344.5	244	B1	5390	-344.5
53	C1P	-7980	-344.5	117	VCI	-3500	-344.5	181	CX2P	980	-344.5	245	B0	5460	-344.5
54	C1P	-7910	-344.5	118	VCI	-3430	-344.5	182	CX2P	1050	-344.5	246	VSS	5530	-344.5
55	C1P	-7840	-344.5	119	VCI	-3360	-344.5	183	CX2P	1120	-344.5	247	G7	5600	-344.5
56	C1N	-7770	-344.5	120	VCI	-3290	-344.5	184	CX2P	1190	-344.5	248	G6	5670	-344.5
57	C1N	-7700	-344.5	121	VCI	-3220	-344.5	185	CX2N	1260	-344.5	249	G5	5740	-344.5
58	C1N	-7630	-344.5	122	C21P	-3150	-344.5	186	CX2N	1330	-344.5	250	G4	5810	-344.5
59	C1N	-7560	-344.5	123	C21P	-3080	-344.5	187	CX2N	1400	-344.5	251	G3	5880	-344.5
60	VCI	-7490	-344.5	124	C21P	-3010	-344.5	188	CX2N	1470	-344.5	252	G2	5950	-344.5
61	VCI	-7420	-344.5	125	C21P	-2940	-344.5	189	CX2N	1540	-344.5	253	G1	6020	-344.5
62	VCI	-7350	-344.5	126	C21P	-2870	-344.5	190	CX2N	1610	-344.5	254	G0	6090	-344.5
63	VCI	-7280	-344.5	127	C21P	-2800	-344.5	191	CX2N	1680	-344.5	255	VSS	6160	-344.5
64	VCI	-7210	-344.5	128	C21N	-2730	-344.5	192	CX2N	1750	-344.5	256	R7	6230	-344.5

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
257	R6	6300	-344.5	321	Dummy	10780	-344.5	385	G<99>	10836	236.5	449	G<227>	9684	236.5
258	R5	6370	-344.5	322	Dummy	10850	-344.5	386	G<101>	10818	111.5	450	G<229>	9666	111.5
259	R4	6440	-344.5	323	Dummy	10920	-344.5	387	G<103>	10800	236.5	451	G<231>	9648	236.5
260	R3	6510	-344.5	324	Dummy	10990	-344.5	388	G<105>	10782	111.5	452	G<233>	9630	111.5
261	R2	6580	-344.5	325	Dummy	11060	-344.5	389	G<107>	10764	236.5	453	G<235>	9612	236.5
262	R1	6650	-344.5	326	Dummy	11130	-344.5	390	G<109>	10746	111.5	454	G<237>	9594	111.5
263	R0	6720	-344.5	327	Dummy	11200	-344.5	391	G<111>	10728	236.5	455	G<239>	9576	236.5
264	VSS	6790	-344.5	328	Dummy	11270	-344.5	392	G<113>	10710	111.5	456	G<241>	9558	111.5
265	DOTCLK	6860	-344.5	329	Dummy	11340	-344.5	393	G<115>	10692	236.5	457	G<243>	9540	236.5
266	DOTCLK	6930	-344.5	330	Dummy	11410	-344.5	394	G<117>	10674	111.5	458	G<245>	9522	111.5
267	VDDIO	7000	-344.5	331	Dummy	11480	-344.5	395	G<119>	10656	236.5	459	G<247>	9504	236.5
268	HSYNC	7070	-344.5	332	Dummy	11550	-344.5	396	G<121>	10638	111.5	460	G<249>	9486	111.5
269	VSS	7140	-344.5	333	Dummy	11620	-344.5	397	G<123>	10620	236.5	461	G<251>	9468	236.5
270	VSYNC	7210	-344.5	334	Dummy	11821.5	111.5	398	G<125>	10602	111.5	462	G<253>	9450	111.5
271	VDDIO	7280	-344.5	335	Dummy	11768.5	236.5	399	G<127>	10584	236.5	463	G<255>	9432	236.5
272	DEN	7350	-344.5	336	G<1>	11718	111.5	400	G<129>	10566	111.5	464	G<257>	9414	111.5
273	VSS	7420	-344.5	337	G<3>	11700	236.5	401	G<131>	10548	236.5	465	G<259>	9396	236.5
274	SDC	7490	-344.5	338	G<5>	11682	111.5	402	G<133>	10530	111.5	466	G<261>	9378	111.5
275	SDI	7560	-344.5	339	G<7>	11664	236.5	403	G<135>	10512	236.5	467	G<263>	9360	236.5
276	SCK	7630	-344.5	340	G<9>	11646	111.5	404	G<137>	10494	111.5	468	G<265>	9342	111.5
277	CSB	7700	-344.5	341	G<11>	11628	236.5	405	G<139>	10476	236.5	469	G<267>	9324	236.5
278	SDO	7770	-344.5	342	G<13>	11610	111.5	406	G<141>	10458	111.5	470	G<269>	9306	111.5
279	VDDIO	7840	-344.5	343	G<15>	11592	236.5	407	G<143>	10440	236.5	471	G<271>	9288	236.5
280	GPI3	7910	-344.5	344	G<17>	11574	111.5	408	G<145>	10422	111.5	472	G<273>	9270	111.5
281	GPI2	7980	-344.5	345	G<19>	11556	236.5	409	G<147>	10404	236.5	473	G<275>	9252	236.5
282	GPI1	8050	-344.5	346	G<21>	11538	111.5	410	G<149>	10386	111.5	474	G<277>	9234	111.5
283	GPI0	8120	-344.5	347	G<23>	11520	236.5	411	G<151>	10368	236.5	475	G<279>	9216	236.5
284	STYPE1	8190	-344.5	348	G<25>	11502	111.5	412	G<153>	10350	111.5	476	G<281>	9198	111.5
285	STYPE0	8260	-344.5	349	G<27>	11484	236.5	413	G<155>	10332	236.5	477	G<283>	9180	236.5
286	CM	8330	-344.5	350	G<29>	11466	111.5	414	G<157>	10314	111.5	478	G<285>	9162	111.5
287	RESB	8400	-344.5	351	G<31>	11448	236.5	415	G<159>	10296	236.5	479	G<287>	9144	236.5
288	SPID	8470	-344.5	352	G<33>	11430	111.5	416	G<161>	10278	111.5	480	G<289>	9126	111.5
289	REV	8540	-344.5	353	G<35>	11412	236.5	417	G<163>	10260	236.5	481	G<291>	9108	236.5
290	BGR	8610	-344.5	354	G<37>	11394	111.5	418	G<165>	10242	111.5	482	G<293>	9090	111.5
291	TB	8680	-344.5	355	G<39>	11376	236.5	419	G<167>	10224	236.5	483	G<295>	9072	236.5
292	LRX	8750	-344.5	356	G<41>	11358	111.5	420	G<169>	10206	111.5	484	G<297>	9054	111.5
293	SHUT	8820	-344.5	357	G<43>	11340	236.5	421	G<171>	10188	236.5	485	G<299>	9036	236.5
294	GAMAS	8890	-344.5	358	G<45>	11322	111.5	422	G<173>	10170	111.5	486	G<301>	9018	111.5
295	NC	8960	-344.5	359	G<47>	11304	236.5	423	G<175>	10152	236.5	487	G<303>	9000	236.5
296	SRGB	9030	-344.5	360	G<49>	11286	111.5	424	G<177>	10134	111.5	488	G<305>	8982	111.5
297	DENMODE	9100	-344.5	361	G<51>	11268	236.5	425	G<179>	10116	236.5	489	G<307>	8964	236.5
298	X400	9170	-344.5	362	G<53>	11250	111.5	426	G<181>	10098	111.5	490	G<309>	8946	111.5
299	VDDIO	9240	-344.5	363	G<55>	11232	236.5	427	G<183>	10080	236.5	491	G<311>	8928	236.5
300	VSS	9310	-344.5	364	G<57>	11214	111.5	428	G<185>	10062	111.5	492	G<313>	8910	111.5
301	VSS	9380	-344.5	365	G<59>	11196	236.5	429	G<187>	10044	236.5	493	G<315>	8892	236.5
302	VSS	9450	-344.5	366	G<61>	11178	111.5	430	G<189>	10026	111.5	494	G<317>	8874	111.5
303	VSS	9520	-344.5	367	G<63>	11160	236.5	431	G<191>	10008	236.5	495	G<319>	8856	236.5
304	VPP	9590	-344.5	368	G<65>	11142	111.5	432	G<193>	9990	111.5	496	G<321>	8838	111.5
305	VPP	9660	-344.5	369	G<67>	11124	236.5	433	G<195>	9972	236.5	497	G<323>	8820	236.5
306	VPP	9730	-344.5	370	G<69>	11106	111.5	434	G<197>	9954	111.5	498	G<325>	8802	111.5
307	VPP	9800	-344.5	371	G<71>	11088	236.5	435	G<199>	9936	236.5	499	G<327>	8784	236.5
308	NC	9870	-344.5	372	G<73>	11070	111.5	436	G<201>	9918	111.5	500	G<329>	8766	111.5
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311	NC	10080	-344.5	375	G<79>	11016	236.5	439	G<207>	9864	236.5	503	G<335>	8712	236.5
312	NC	10150	-344.5	376	G<81>	10998	111.5	440	G<209>	9846	111.5	504	G<337>	8694	111.5
313	NC	10220	-344.5	377	G<83>	10980	236.5	441	G<211>	9828	236.5	505	G<339>	8676	236.5
314	NC	10290	-344.5	378	G<85>	10962	111.5	442	G<213>	9810	111.5	506	G<341>	8658	111.5
315	NC	10360	-344.5	379	G<87>	10944	236.5	443	G<215>	9792	236.5	507	G<343>	8640	236.5
316	NC	10430	-344.5	380	G<89>	10926	111.5	444	G<217>	9774	111.5	508	G<345>	8622	111.5
317	NC	10500	-344.5	381	G<91>	10908	236.5	445	G<219>	9756	236.5	509	G<347>	8604	236.5
318	NC	10570	-344.5	382	G<93>	10890	111.5	446	G<221>	9738	111.5	510	G<349>	8586	111.5
319	NC	10640	-344.5	383	G<95>	10872	236.5	447	G<223>	9720	236.5	511	G<351>	8568	236.5
320	NC	10710	-344.5	384	G<97>	10854	111.5	448	G<225>	9702	111.5	512	G<353>	8550	111.5

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
513	G<355>	8532	236.5	578	G<485>	7362	111.5	643	G<615>	6192	236.5	708	G<745>	5022	111.5
514	G<357>	8514	111.5	579	G<487>	7344	236.5	644	G<617>	6174	111.5	709	G<747>	5004	236.5
515	G<359>	8496	236.5	580	G<489>	7326	111.5	645	G<619>	6156	236.5	710	G<749>	4986	111.5
516	G<361>	8478	111.5	581	G<491>	7308	236.5	646	G<621>	6138	111.5	711	G<751>	4968	236.5
517	G<363>	8460	236.5	582	G<493>	7290	111.5	647	G<623>	6120	236.5	712	G<753>	4950	111.5
518	G<365>	8442	111.5	583	G<495>	7272	236.5	648	G<625>	6102	111.5	713	G<755>	4932	236.5
519	G<367>	8424	236.5	584	G<497>	7254	111.5	649	G<627>	6084	236.5	714	G<757>	4914	111.5
520	G<369>	8406	111.5	585	G<499>	7236	236.5	650	G<629>	6066	111.5	715	G<759>	4896	236.5
521	G<371>	8388	236.5	586	G<501>	7218	111.5	651	G<631>	6048	236.5	716	G<761>	4878	111.5
522	G<373>	8370	111.5	587	G<503>	7200	236.5	652	G<633>	6030	111.5	717	G<763>	4860	236.5
523	G<375>	8352	236.5	588	G<505>	7182	111.5	653	G<635>	6012	236.5	718	G<765>	4842	111.5
524	G<377>	8334	111.5	589	G<507>	7164	236.5	654	G<637>	5994	111.5	719	G<767>	4824	236.5
525	G<379>	8316	236.5	590	G<509>	7146	111.5	655	G<639>	5976	236.5	720	G<769>	4806	111.5
526	G<381>	8298	111.5	591	G<511>	7128	236.5	656	G<641>	5958	111.5	721	G<771>	4788	236.5
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529	G<387>	8244	236.5	594	G<517>	7074	111.5	659	G<647>	5904	236.5	724	G<777>	4734	111.5
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532	G<393>	8190	111.5	597	G<523>	7020	236.5	662	G<653>	5850	111.5	727	G<783>	4680	236.5
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535	G<399>	8136	236.5	600	G<529>	6966	111.5	665	G<659>	5796	236.5	730	G<789>	4626	111.5
536	G<401>	8118	111.5	601	G<531>	6948	236.5	666	G<661>	5778	111.5	731	G<791>	4608	236.5
537	G<403>	8100	236.5	602	G<533>	6930	111.5	667	G<663>	5760	236.5	732	G<793>	4590	111.5
538	G<405>	8082	111.5	603	G<535>	6912	236.5	668	G<665>	5742	111.5	733	G<795>	4572	236.5
539	G<407>	8064	236.5	604	G<537>	6894	111.5	669	G<667>	5724	236.5	734	G<797>	4554	111.5
540	G<409>	8046	111.5	605	G<539>	6876	236.5	670	G<669>	5706	111.5	735	G<799>	4536	236.5
541	G<411>	8028	236.5	606	G<541>	6858	111.5	671	G<671>	5688	236.5	736	G<801>	4518	111.5
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545	G<419>	7956	236.5	610	G<549>	6786	111.5	675	G<679>	5616	236.5	740	G<809>	4446	111.5
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547	G<423>	7920	236.5	612	G<553>	6750	111.5	677	G<683>	5580	236.5	742	G<813>	4410	111.5
548	G<425>	7902	111.5	613	G<555>	6732	236.5	678	G<685>	5562	111.5	743	G<815>	4392	236.5
549	G<427>	7884	236.5	614	G<557>	6714	111.5	679	G<687>	5544	236.5	744	Dummy	4374	111.5
550	G<429>	7866	111.5	615	G<559>	6696	236.5	680	G<689>	5526	111.5	745	Dummy	4356	236.5
551	G<431>	7848	236.5	616	G<561>	6678	111.5	681	G<691>	5508	236.5	746	Dummy	4338	111.5
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553	G<435>	7812	236.5	618	G<565>	6642	111.5	683	G<695>	5472	236.5	748	S<478>	4302	111.5
554	G<437>	7794	111.5	619	G<567>	6624	236.5	684	G<697>	5454	111.5	749	S<477>	4284	236.5
555	G<439>	7776	236.5	620	G<569>	6606	111.5	685	G<699>	5436	236.5	750	S<476>	4266	111.5
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557	G<443>	7740	236.5	622	G<573>	6570	111.5	687	G<703>	5400	236.5	752	S<474>	4230	111.5
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559	G<447>	7704	236.5	624	G<577>	6534	111.5	689	G<707>	5364	236.5	754	S<472>	4194	111.5
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563	G<455>	7632	236.5	628	G<585>	6462	111.5	693	G<715>	5292	236.5	758	S<468>	4122	111.5
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567	G<463>	7560	236.5	632	G<593>	6390	111.5	697	G<723>	5220	236.5	762	S<464>	4050	111.5
568	G<465>	7542	111.5	633	G<595>	6372	236.5	698	G<725>	5202	111.5	763	S<463>	4032	236.5
569	G<467>	7524	236.5	634	G<597>	6354	111.5	699	G<727>	5184	236.5	764	S<462>	4014	111.5
570	G<469>	7506	111.5	635	G<599>	6336	236.5	700	G<729>	5166	111.5	765	S<461>	3996	236.5
571	G<471>	7488	236.5	636	G<601>	6318	111.5	701	G<731>	5148	236.5	766	S<460>	3978	111.5
572	G<473>	7470	111.5	637	G<603>	6300	236.5	702	G<733>	5130	111.5	767	S<459>	3960	236.5
573	G<475>	7452	236.5	638	G<605>	6282	111.5	703	G<735>	5112	236.5	768	S<458>	3942	111.5
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575	G<479>	7416	236.5	640	G<609>	6246	111.5	705	G<739>	5076	236.5	770	S<456>	3906	111.5
576	G<481>	7398	111.5	641	G<611>	6228	236.5	706	G<741>	5058	111.5	771	S<455>	3888	236.5
577	G<483>	7380	236.5	642	G<613>	6210	111.5	707	G<743>	5040	236.5	772	S<454>	3870	111.5

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
773	S<453>	3852	236.5	838	S<388>	2682	111.5	903	S<323>	1512	236.5	968	S<258>	342	111.5
774	S<452>	3834	111.5	839	S<387>	2664	236.5	904	S<322>	1494	111.5	969	S<257>	324	236.5
775	S<451>	3816	236.5	840	S<386>	2646	111.5	905	S<321>	1476	236.5	970	S<256>	306	111.5
776	S<450>	3798	111.5	841	S<385>	2628	236.5	906	S<320>	1458	111.5	971	S<255>	288	236.5
777	S<449>	3780	236.5	842	S<384>	2610	111.5	907	S<319>	1440	236.5	972	S<254>	270	111.5
778	S<448>	3762	111.5	843	S<383>	2592	236.5	908	S<318>	1422	111.5	973	S<253>	252	236.5
779	S<447>	3744	236.5	844	S<382>	2574	111.5	909	S<317>	1404	236.5	974	S<252>	234	111.5
780	S<446>	3726	111.5	845	S<381>	2556	236.5	910	S<316>	1386	111.5	975	S<251>	216	236.5
781	S<445>	3708	236.5	846	S<380>	2538	111.5	911	S<315>	1368	236.5	976	S<250>	198	111.5
782	S<444>	3690	111.5	847	S<379>	2520	236.5	912	S<314>	1350	111.5	977	S<249>	180	236.5
783	S<443>	3672	236.5	848	S<378>	2502	111.5	913	S<313>	1332	236.5	978	S<248>	162	111.5
784	S<442>	3654	111.5	849	S<377>	2484	236.5	914	S<312>	1314	111.5	979	S<247>	144	236.5
785	S<441>	3636	236.5	850	S<376>	2466	111.5	915	S<311>	1296	236.5	980	S<246>	126	111.5
786	S<440>	3618	111.5	851	S<375>	2448	236.5	916	S<310>	1278	111.5	981	S<245>	108	236.5
787	S<439>	3600	236.5	852	S<374>	2430	111.5	917	S<309>	1260	236.5	982	S<244>	90	111.5
788	S<438>	3582	111.5	853	S<373>	2412	236.5	918	S<308>	1242	111.5	983	S<243>	72	236.5
789	S<437>	3564	236.5	854	S<372>	2394	111.5	919	S<307>	1224	236.5	984	S<242>	54	111.5
790	S<436>	3546	111.5	855	S<371>	2376	236.5	920	S<306>	1206	111.5	985	S<241>	36	236.5
791	S<435>	3528	236.5	856	S<370>	2358	111.5	921	S<305>	1188	236.5	986	S<240>	18	111.5
792	S<434>	3510	111.5	857	S<369>	2340	236.5	922	S<304>	1170	111.5	987	Dummy	0	236.5
793	S<433>	3492	236.5	858	S<368>	2322	111.5	923	S<303>	1152	236.5	988	S<239>	-18	111.5
794	S<432>	3474	111.5	859	S<367>	2304	236.5	924	S<302>	1134	111.5	989	S<238>	-36	236.5
795	S<431>	3456	236.5	860	S<366>	2286	111.5	925	S<301>	1116	236.5	990	S<237>	-54	111.5
796	S<430>	3438	111.5	861	S<365>	2268	236.5	926	S<300>	1098	111.5	991	S<236>	-72	236.5
797	S<429>	3420	236.5	862	S<364>	2250	111.5	927	S<299>	1080	236.5	992	S<235>	-90	111.5
798	S<428>	3402	111.5	863	S<363>	2232	236.5	928	S<298>	1062	111.5	993	S<234>	-108	236.5
799	S<427>	3384	236.5	864	S<362>	2214	111.5	929	S<297>	1044	236.5	994	S<233>	-126	111.5
800	S<426>	3366	111.5	865	S<361>	2196	236.5	930	S<296>	1026	111.5	995	S<232>	-144	236.5
801	S<425>	3348	236.5	866	S<360>	2178	111.5	931	S<295>	1008	236.5	996	S<231>	-162	111.5
802	S<424>	3330	111.5	867	S<359>	2160	236.5	932	S<294>	990	111.5	997	S<230>	-180	236.5
803	S<423>	3312	236.5	868	S<358>	2142	111.5	933	S<293>	972	236.5	998	S<229>	-198	111.5
804	S<422>	3294	111.5	869	S<357>	2124	236.5	934	S<292>	954	111.5	999	S<228>	-216	236.5
805	S<421>	3276	236.5	870	S<356>	2106	111.5	935	S<291>	936	236.5	1000	S<227>	-234	111.5
806	S<420>	3258	111.5	871	S<355>	2088	236.5	936	S<290>	918	111.5	1001	S<226>	-252	236.5
807	S<419>	3240	236.5	872	S<354>	2070	111.5	937	S<289>	900	236.5	1002	S<225>	-270	111.5
808	S<418>	3222	111.5	873	S<353>	2052	236.5	938	S<288>	882	111.5	1003	S<224>	-288	236.5
809	S<417>	3204	236.5	874	S<352>	2034	111.5	939	S<287>	864	236.5	1004	S<223>	-306	111.5
810	S<416>	3186	111.5	875	S<351>	2016	236.5	940	S<286>	846	111.5	1005	S<222>	-324	236.5
811	S<415>	3168	236.5	876	S<350>	1998	111.5	941	S<285>	828	236.5	1006	S<221>	-342	111.5
812	S<414>	3150	111.5	877	S<349>	1980	236.5	942	S<284>	810	111.5	1007	S<220>	-360	236.5
813	S<413>	3132	236.5	878	S<348>	1962	111.5	943	S<283>	792	236.5	1008	S<219>	-378	111.5
814	S<412>	3114	111.5	879	S<347>	1944	236.5	944	S<282>	774	111.5	1009	S<218>	-396	236.5
815	S<411>	3096	236.5	880	S<346>	1926	111.5	945	S<281>	756	236.5	1010	S<217>	-414	111.5
816	S<410>	3078	111.5	881	S<345>	1908	236.5	946	S<280>	738	111.5	1011	S<216>	-432	236.5
817	S<409>	3060	236.5	882	S<344>	1890	111.5	947	S<279>	720	236.5	1012	S<215>	-450	111.5
818	S<408>	3042	111.5	883	S<343>	1872	236.5	948	S<278>	702	111.5	1013	S<214>	-468	236.5
819	S<407>	3024	236.5	884	S<342>	1854	111.5	949	S<277>	684	236.5	1014	S<213>	-486	111.5
820	S<406>	3006	111.5	885	S<341>	1836	236.5	950	S<276>	666	111.5	1015	S<212>	-504	236.5
821	S<405>	2988	236.5	886	S<340>	1818	111.5	951	S<275>	648	236.5	1016	S<211>	-522	111.5
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823	S<403>	2952	236.5	888	S<338>	1782	111.5	953	S<273>	612	236.5	1018	S<209>	-558	111.5
824	S<402>	2934	111.5	889	S<337>	1764	236.5	954	S<272>	594	111.5	1019	S<208>	-576	236.5
825	S<401>	2916	236.5	890	S<336>	1746	111.5	955	S<271>	576	236.5	1020	S<207>	-594	111.5
826	S<400>	2898	111.5	891	S<335>	1728	236.5	956	S<270>	558	111.5	1021	S<206>	-612	236.5
827	S<399>	2880	236.5	892	S<334>	1710	111.5	957	S<269>	540	236.5	1022	S<205>	-630	111.5
828	S<398>	2862	111.5	893	S<333>	1692	236.5	958	S<268>	522	111.5	1023	S<204>	-648	236.5
829	S<397>	2844	236.5	894	S<332>	1674	111.5	959	S<267>	504	236.5	1024	S<203>	-666	111.5
830	S<396>	2826	111.5	895	S<331>	1656	236.5	960	S<266>	486	111.5	1025	S<202>	-684	236.5
831	S<395>	2808	236.5	896	S<330>	1638	111.5	961	S<265>	468	236.5	1026	S<201>	-702	111.5
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833	S<393>	2772	236.5	898	S<328>	1602	111.5	963	S<263>	432	236.5	1028	S<199>	-738	111.5
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Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
1033	S<194>	-828	236.5	1098	S<129>	-1998	111.5	1163	S<64>	-3168	236.5	1228	Dummy	-4338	111.5
1034	S<193>	-846	111.5	1099	S<128>	-2016	236.5	1164	S<63>	-3186	111.5	1229	Dummy	-4356	236.5
1035	S<192>	-864	236.5	1100	S<127>	-2034	111.5	1165	S<62>	-3204	236.5	1230	Dummy	-4374	111.5
1036	S<191>	-882	111.5	1101	S<126>	-2052	236.5	1166	S<61>	-3222	111.5	1231	G<814>	-4392	236.5
1037	S<190>	-900	236.5	1102	S<125>	-2070	111.5	1167	S<60>	-3240	236.5	1232	G<812>	-4410	111.5
1038	S<189>	-918	111.5	1103	S<124>	-2088	236.5	1168	S<59>	-3258	111.5	1233	G<810>	-4428	236.5
1039	S<188>	-936	236.5	1104	S<123>	-2106	111.5	1169	S<58>	-3276	236.5	1234	G<808>	-4446	111.5
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1096	S<131>	-1962	111.5	1161	S<66>	-3132	236.5	1226	S<1>	-4302	111.5	1291	G<694>	-5472	236.5
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Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
1293	G<690>	-5508	236.5	1358	G<560>	-6678	111.5	1423	G<430>	-7848	236.5	1488	G<300>	-9018	111.5
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1315	G<646>	-5904	236.5	1380	G<516>	-7074	111.5	1445	G<386>	-8244	236.5	1510	G<256>	-9414	111.5
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1343	G<590>	-6408	236.5	1408	G<460>	-7578	111.5	1473	G<330>	-8748	236.5	1538	G<200>	-9918	111.5
1344	G<588>	-6426	111.5	1409	G<458>	-7596	236.5	1474	G<328>	-8766	111.5	1539	G<198>	-9936	236.5
1345	G<586>	-6444	236.5	1410	G<456>	-7614	111.5	1475	G<326>	-8784	236.5	1540	G<196>	-9954	111.5
1346	G<584>	-6462	111.5	1411	G<454>	-7632	236.5	1476	G<324>	-8802	111.5	1541	G<194>	-9972	236.5
1347	G<582>	-6480	236.5	1412	G<452>	-7650	111.5	1477	G<322>	-8820	236.5	1542	G<192>	-9990	111.5
1348	G<580>	-6498	111.5	1413	G<450>	-7668	236.5	1478	G<320>	-8838	111.5	1543	G<190>	-10008	236.5
1349	G<578>	-6516	236.5	1414	G<448>	-7686	111.5	1479	G<318>	-8856	236.5	1544	G<188>	-10026	111.5
1350	G<576>	-6534	111.5	1415	G<446>	-7704	236.5	1480	G<316>	-8874	111.5	1545	G<186>	-10044	236.5
1351	G<574>	-6552	236.5	1416	G<444>	-7722	111.5	1481	G<314>	-8892	236.5	1546	G<184>	-10062	111.5
1352	G<572>	-6570	111.5	1417	G<442>	-7740	236.5	1482	G<312>	-8910	111.5	1547	G<182>	-10080	236.5
1353	G<570>	-6588	236.5	1418	G<440>	-7758	111.5	1483	G<310>	-8928	236.5	1548	G<180>	-10098	111.5
1354	G<568>	-6606	111.5	1419	G<438>	-7776	236.5	1484	G<308>	-8946	111.5	1549	G<178>	-10116	236.5
1355	G<566>	-6624	236.5	1420	G<436>	-7794	111.5	1485	G<306>	-8964	236.5	1550	G<176>	-10134	111.5
1356	G<564>	-6642	111.5	1421	G<434>	-7812	236.5	1486	G<304>	-8982	111.5	1551	G<174>	-10152	236.5
1357	G<562>	-6660	236.5	1422	G<432>	-7830	111.5	1487	G<302>	-9000	236.5	1552	G<172>	-10170	111.5

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
1553	G<170>	-10188	236.5	1618	G<40>	-11358	111.5								
1554	G<168>	-10206	111.5	1619	G<38>	-11376	236.5								
1555	G<166>	-10224	236.5	1620	G<36>	-11394	111.5								
1556	G<164>	-10242	111.5	1621	G<34>	-11412	236.5								
1557	G<162>	-10260	236.5	1622	G<32>	-11430	111.5								
1558	G<160>	-10278	111.5	1623	G<30>	-11448	236.5								
1559	G<158>	-10296	236.5	1624	G<28>	-11466	111.5								
1560	G<156>	-10314	111.5	1625	G<26>	-11484	236.5								
1561	G<154>	-10332	236.5	1626	G<24>	-11502	111.5								
1562	G<152>	-10350	111.5	1627	G<22>	-11520	236.5								
1563	G<150>	-10368	236.5	1628	G<20>	-11538	111.5								
1564	G<148>	-10386	111.5	1629	G<18>	-11556	236.5								
1565	G<146>	-10404	236.5	1630	G<16>	-11574	111.5								
1566	G<144>	-10422	111.5	1631	G<14>	-11592	236.5								
1567	G<142>	-10440	236.5	1632	G<12>	-11610	111.5								
1568	G<140>	-10458	111.5	1633	G<10>	-11628	236.5								
1569	G<138>	-10476	236.5	1634	G<8>	-11646	111.5								
1570	G<136>	-10494	111.5	1635	G<6>	-11664	236.5								
1571	G<134>	-10512	236.5	1636	G<4>	-11682	111.5								
1572	G<132>	-10530	111.5	1637	G<2>	-11700	236.5								
1573	G<130>	-10548	236.5	1638	G<0>	-11718	111.5								
1574	G<128>	-10566	111.5	1639	Dummy	-11768.5	236.5								
1575	G<126>	-10584	236.5	1640	Dummy	-11821.5	111.5								
1576	G<124>	-10602	111.5												
1577	G<122>	-10620	236.5												
1578	G<120>	-10638	111.5												
1579	G<118>	-10656	236.5												
1580	G<116>	-10674	111.5												
1581	G<114>	-10692	236.5												
1582	G<112>	-10710	111.5												
1583	G<110>	-10728	236.5												
1584	G<108>	-10746	111.5												
1585	G<106>	-10764	236.5												
1586	G<104>	-10782	111.5												
1587	G<102>	-10800	236.5												
1588	G<100>	-10818	111.5												
1589	G<98>	-10836	236.5												
1590	G<96>	-10854	111.5												
1591	G<94>	-10872	236.5												
1592	G<92>	-10890	111.5												
1593	G<90>	-10908	236.5												
1594	G<88>	-10926	111.5												
1595	G<86>	-10944	236.5												
1596	G<84>	-10962	111.5												
1597	G<82>	-10980	236.5												
1598	G<80>	-10998	111.5												
1599	G<78>	-11016	236.5												
1600	G<76>	-11034	111.5												
1601	G<74>	-11052	236.5												
1602	G<72>	-11070	111.5												
1603	G<70>	-11088	236.5												
1604	G<68>	-11106	111.5												
1605	G<66>	-11124	236.5												
1606	G<64>	-11142	111.5												
1607	G<62>	-11160	236.5												
1608	G<60>	-11178	111.5												
1609	G<58>	-11196	236.5												
1610	G<56>	-11214	111.5												
1611	G<54>	-11232	236.5												
1612	G<52>	-11250	111.5												
1613	G<50>	-11268	236.5												
1614	G<48>	-11286	111.5												
1615	G<46>	-11304	236.5												
1616	G<44>	-11322	111.5												
1617	G<42>	-11340	236.5												

6 Pin Description

SSD2128 Pin Function Description

Key:

I = Input
O =Output
I/O = Bi-directional (input/output)
P = Power pin
GND = System VSS

Table 6-1: Power Supply Pins

Name	Type	Connect to	Function	Description	When not in use
V_{SS}	P	GND	Ground of Power Supply	System ground pin of the IC.	-
A_{VSS}				Grounding for analog circuit.	-
V_{SSRC}				Grounding for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages.	-
V_{CHS}				Grounding for booster circuit.	-
V_{CORE}	P	V_{REGC}	Power for Core Logic	V_{DD} for core use - Connect a capacitor for stabilization	-
V_{DDIO}		System V_{DD}	Power for Interface Logic Pins	Voltage input pin for logic I/O.	-
V_{CI}		Power supply	Power for Analog Circuits	Booster input voltage pin. - Connect to voltage source between 2.5V to 3.3V	-
V_{CIP}		V_{CI}		Voltage supply pin for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages.	-
V_{CIM}	O	Stabilizing capacitor	Booster Output	Negative voltage of V_{CI}	-
AV_{DD}		Stabilizing capacitor	Booster Voltages	Booster voltage and regulated between 5.1V to 6.1V. Controlled by command Power control 2 (R0Ch)	-
AV_{DDM}		Stabilizing capacitor	Booster Voltages	Booster voltage and regulated between -5.1V to -6.1V. Controlled by command Power control 2 (R0Ch)	-
AV_{DDG}		AV_{DD} on FPC	Voltage for analog	Power supply used by on chip analog blocks and V_{GH}/V_{GL} dcdc. Must connect AV_{DD} together	-
VLCDH	O	Stabilizing capacitor	LCD Driving Voltages	The maximum source driver voltage.	-
VLCDL				The minimum source driver voltage.	-
V_{GH}				A positive power output pin for gate driver.	-
V_{GL}				A negative power output pin for gate driver.	-
V_{REGC}	P	Stabilizing capacitor	Regulator output for logic circuits	Regulator output for V_{CORE} use	-
VPP	P	Test Pad	MTP Programming	Power for MTP Program and Erase	Open

CX1P	P	Booster capacitor for VCIM	Booster and Stabilization Capacitors	- Connect a capacitor to CX1N	-
CX1N				- Connect a capacitor to CX1P	-
CX2P	P	Booster capacitor for VCIM	Booster and Stabilization Capacitors	- Connect a capacitor to CX2N	-
CX2N				- Connect a capacitor to CX2P	-
C11P	P	Booster capacitor for AVDD	Booster and Stabilization Capacitors	- Connect a capacitor to C11N	-
C11N				- Connect a capacitor to C11P	-
C12P	P	Booster capacitor for AVDD	Booster and Stabilization Capacitors	- Connect a capacitor to C12N	-
C12N				- Connect a capacitor to C12P	-
C21P	P	Booster capacitor for AVDDM	Booster and Stabilization Capacitors	- Connect a capacitor to C21N	-
C21N				- Connect a capacitor to C21P	-
C22P	P	Booster capacitor for AVDDM	Booster and Stabilization Capacitors	- Connect a capacitor to C22N	-
C22N				- Connect a capacitor to C22P	-
C1P	P	Booster capacitor for VGH	Booster and Stabilization Capacitors	- Connect a capacitor to C1N	-
C1N				- Connect a capacitor to C1P	-
C2P	P	Booster capacitor for VGH	Booster and Stabilization Capacitors	- Connect a capacitor to C2N	-
C2N				- Connect a capacitor to C2P	-
C3P	P	Booster capacitor for VGL	Booster and Stabilization Capacitors	- Connect a capacitor to C3N	-
C3N				- Connect a capacitor to C3P	-

Table 6-2: Interface Logic Pins

Name	Type	Connect to	Function	Description	When not in use
SPID	I	V_{DDIO} or V_{SS}	Serial Interface	ID selection pin for the SPI serial interface. When sending serial data, the "ID" bit must match with the logic stage of this pin. (Refer to Serial Interface block description on Page 54 for details)	-
CSB		MPU		Chip select pin of serial interface.	V_{DDIO}
SDI		MPU		Data input pin in serial mode.	V_{SS}
SDC		MPU		Data/Command pin of serial interface.	V_{SS}
SCK		MPU		Clock input pin in serial mode.	V_{SS}
SDO	O	MPU	Serial Interface	Data output pin in serial mode.	Open
SHUT	I	V_{DDIO} or V_{SS}	Logic Control	Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. - Connect to V_{DDIO} for sleep mode - Connect to V_{SS} for normal operating mode Note: Software can override the setting	V_{DDIO} or V_{SS}
VSYNC	I	MPU	RGB Interface	Frame synchronization signal. Fixed to V_{DDIO} or V_{SS} if not used.	-
HSYNC	I	MPU		Line synchronization signal. Fixed to V_{DDIO} or V_{SS} if not used	-
DOTCLK	I	MPU	Display Timing Signals	Dot-clock signal and oscillator source. External clock must be provided to that pin even at front or black porch non-display period.	-
DEN	I	MPU	Display Enable	Display enable pin from controller.	V_{DDIO}
RR[7:0]	I	MPU	Graphic Display Data	- RR[7:0] : Red Data – 24bit parallel/8bit serial - RR[7:2] : Red Data –18bit parallel/6bit serial - GG[7:0] : Green Data –24bit parallel - GG[7:2] : Green Data –18bit parallel - BB[7:0] : Blue Data –24bit parallel - BB[7:2] : Blue Data –18bit parallel	RR[7:6] or GG[7:6] or BB [7:6] [1] [2]
GG[7:0]					
BB[7:0]					
RESB	I	MPU	System reset	System reset pin. Initialization occurs once this pin is pulled Low, the minimum pulse length is 1ms. A low pulse must be applied after power-on. Connect this pin to VDDIO when not used.	V_{DDIO}
SRGB	I	V_{DDIO} or V_{SS}	RGB interface selection	Determine data input for SSD2128. - Connect to V_{SS} for the operation of parallel RGB mode 18/24 bits. - Connect to V_{DDIO} for the operation of serial RGB mode 6/8 bits. Note: Software can override the setting	-
X400	I	V_{DDIO} or V_{SS}	RGB interface selection	Determine data input for SSD2128. - Connect to V_{SS} for the operation of using full 480 sources - Connect to V_{DDIO} for the operation of using 400 sources at center. First data will appear at S40. Note: Software can override the setting	-

[1] When using the 18-bit parallel interface, RR[1:0] is connected to RR[7:6], GG[1:0] is connected to GG[7:6] and BB[1:0] is connected to BB[7:6].
[2] When using the 6-bit serial interface, RR[1:0] is connected to RR[7:6].

Table 6-3: Interface Logic Pins

Name	Type	Connect to	Function	Description	When not in use
DENMODE	I	V_{DDIO} or V_{SS}	RGB interface selection	Determine data input for SSD2128. - Connect to V_{SS} for the operation of SYNC mode - Connect to V_{DDIO} for the operation of DEN mode Note: Software can override the setting	-
GPI[3:0]	I	User define		General propose pins defined by user	Open
GAMAS	I	V_{DDIO} or V_{SS}	Logic Control	GAMAS controls the default register values	V_{DDIO} or V_{SS}
DISP	I	V_{DDIO} or V_{SS}	Logic Control	Display On / Off Mode Control - Connect to V_{SS}: input data are invalid and write blank data to the data register. The blank data will be gray level 0 for normal black panels, and be gray level 255 for normal white panels - Connect to V_{DDIO}: input data are valid and write to the data register	V_{DDIO}
STYPE0	I	V_{DDIO} or V_{SS}	Serial Interface Selection	STYPE[1:0] = 0x ; SPID type 3 wires SPI STYPE[1:0] = 10 ; standard 3 wires SPI STYPE[1:0] = 11 ; standard 4 wires SPI	-
STYPE1	I	V_{DDIO} or V_{SS}			-
BGR	I	V_{DDIO} or V_{SS}	Panel Mapping controls	Color mapping selection pin. Refer to G0-G815 pin description. Note: Software can override the setting	V_{DDIO} or V_{SS}
REV	I	V_{DDIO} or V_{SS}		Input pin to select the display reversion. - Connect to V_{DDIO} mapping data "0" to maximum pixel voltage for normal white panel - Connect to V_{SS} mapping data "0" to minimum pixel voltage for normal black panel Note: Software can override the setting	V_{DDIO} or V_{SS}
LRX	I	V_{DDIO} or V_{SS}		Select the Source driver data shift direction. - Connect to V_{DDIO} for display first pixel data at S0 - Connect to V_{SS} for display first pixel data at S479 Note: Software can override the setting	V_{DDIO} or V_{SS}
TB	I	V_{DDIO} or V_{SS}		Select the Gate driver scans direction. Note: Software can override the setting	V_{DDIO} or V_{SS}
CM	I	V_{SS}		Input pin to select 16.7M-color - Connect to V_{SS} for 16.7M-color display mode	V_{SS}

Table 6-4: Driver Output Pins

Name	Type	Connect to	Function	Description	When not in use
VCOMDC	O	LCD	LCD Driving Signals	A power supply for the TFT-display common electrode.	Open
G0-G815				Gate driver output pins. These pins output VGH or VGL level. Color filter arrangement depends on BGR pin. G(3n): Display Red if BGR = Low, Blue if BGR = High. G(3n+1): Display Green. G(3n+2): Display Blue if BGR = Low, Red if BGR = High.	Open
S0-S479				Source driver output pins.	Open
DRV	O	PWM Booster	PWM Driving Signals	PWM output driver signal for the boost converter	Open

Table 6-5: Miscellaneous Pins

Name	Type	Connect to	Function	Description	When not in use
NC	-	-	-	These pins must be left open and cannot be connected together	Open
DUMMY	-	-	-	Floating pins and no connection inside the IC. These pins can be shorted together or connect to any signal.	Open
TESTA	I/O	Test Pad on FPC	IC Testing Signal	Test pin of the internal circuit. - Leave this pin open and optional to insert test point in FPC for evaluation.	Open
TESTB					

7 COMMAND TABLE

Table 7-1: Command Table and POR (Power On Reset) values

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R01h	Driver output control (1)	0	1	X400	RL	REV	0	BGR	0	TB	1	0	0	0	0	1	1	1	1
	(XX0Fh)			X	X	X	0	X	0	X	1	0	0	0	0	1	1	1	1
R02h	LCD-Driving-Waveform Control	0	1	0	0	0	DS	B/C	EOR	NW9	NW8	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
	(0C02h)			0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0
R03h	Power control (1)	0	1	DCM3	DCM2	DCM1	DCM0	0	BT2	BT1	BT0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
	(E40Eh)			1	1	1	0	0	1	0	0	0	0	0	0	1	1	1	0
R04h	Driver output control (2)	0	1	DISP2	DISP1	DISP0	0	0	OLO	0	0	FSE7	FSE6	FSE5	FSE4	FSE3	FSE2	FSE1	FSE0
	(2400h)			0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
R0Bh	Frame cycle control	0	1	GO1	GO0	SDT1	SDT0	EQ1	EQ0	PT1	PT0	EQ2	0	0	0	BTP1	BTP0	SDT2	0
	(D804h)			1	1	0	1	1	0	0	0	0	0	0	0	0	1	0	0
R0Dh	Power control (3)	0	1	0	0	0	0	VDL3	VDL2	VDL1	VDL0	0	0	0	0	VDH3	VDH2	VDH1	VDH0
	(0C0Ch)			0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0
R0Fh	Gate scan starting Position	0	1	0	0	0	0	0	0	0	SCN8	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R16h	Pixel per line	0	1	XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
	(EF8Eh) x400=0			1	1	1	0	1	1	1	1	1	0	0	0	1	1	1	0
	(C786h) x400=1			1	1	0	0	0	1	1	1	1	0	0	0	0	1	1	0
R17h	Vertical Porch	0	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
	(0003h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	nMTP	0	VCM7	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
	(0029h)			0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1
R30h	R+ γ control (1)	0	1	RPRP13	RPRP12	RPRP11	RPRP10	RPRP04	RPRP03	RPRP02	RPRP01	RPRP00	0	RVRP05	RVR04	RVRP03	RVRP02	RVRP01	RVRP00
	(A2A0)			1	0	1	0	0	0	1	0	1	0	1	0	0	0	0	0
R31h	R+ γ control (2)	0	1	RSRP03	RSRP02	RSRP01	RSRP00	RPRP43	RPRP42	RPRP41	RPRP40	RPRP33	RPRP32	RPRP31	RPRP30	0	RPRP22	RPRP21	RPRP20
	(FA86)			1	1	1	1	1	0	1	0	1	0	0	0	0	1	1	0
R32h	R+ γ control (3)	0	1	0	RPRP72	RPRP71	RPRP70	0	RPRP63	RPRP62	RPRP61	RPRP60	0	0	0	RPRP53	RPRP52	RPRP51	RPRP50
	(3388)			0	0	1	1	0	0	1	1	1	0	0	0	1	0	0	0
R33h	R+ γ control (4)	0	1	RVRP15	RVR14	RVRP13	RVRP12	RVRP11	RVRP10	0	RPRP94	RPRP93	RPRP92	RPRP91	RPRP90	RPRP83	RPRP82	RPRP81	RPRP80
	(4197)			0	1	0	0	0	0	0	1	1	0	0	1	0	1	1	1
R34h	R- γ control (1)	0	1	RPRN13	RPRN12	RPRN11	RPRN10	RPRN04	RPRN03	RPRN02	RPRN01	RPRN00	0	RVRN05	RVR04	RVRN03	RVRN02	RVRN01	RVRN00
	(C425)			1	1	0	0	0	1	0	0	0	0	1	0	0	1	0	1
R35h	R- γ control (2)	0	1	RSRN03	RSRN02	RSRN01	RSRN00	RPRN43	RPRN42	RPRN41	RPRN40	RPRN33	RPRN32	RPRN31	RPRN30	0	RPRN22	RPRN21	RPRN20
	(F6C7)			1	1	1	1	0	1	1	0	1	1	0	0	0	1	1	1
R36h	R- γ control (3)	0	1	0	RPRN72	RPRN71	RPRN70	0	RPRN63	RPRN62	RPRN61	RPRN60	0	0	0	RPRN53	RPRN52	RPRN51	RPRN50
	(538B)			0	1	0	1	0	0	1	1	1	0	0	0	1	0	1	1
R37h	R- γ control (4)	0	1	RVRN15	RVR14	RVRN13	RVRN12	RVRN11	RVRN10	0	RPRN94	RPRN93	RPRN92	RPRN91	RPRN90	RPRN83	RPRN82	RPRN81	RPRN80
	(3D19)			0	0	1	1	1	1	0	1	0	0	0	1	1	0	0	1
R40h	G+ γ control (1)	0	1	GPRP13	GPRP12	GPRP11	GPRP10	GPRP04	GPRP03	GPRP02	GPRP01	GPRP00	0	GVRP05	GVR04	GVRP03	GVRP02	GVRP01	GVRP00
													0						
R41h	G+ γ control (2)	0	1	GSRP03	GSRP02	GSRP01	GSRP00	GPRP43	GPRP42	GPRP41	GPRP40	GPRP33	GPRP32	GPRP31	GPRP30	0	GPRP22	GPRP21	GPRP20
																0			
R42h	G+ γ control (3)	0	1	0	GPRP72	GPRP71	GPRP70	0	GPRP63	GPRP62	GPRP61	GPRP60	0	0	0	GPRP53	GPRP52	GPRP51	GPRP50
				0				0					0	0	0				
R43h	G+ γ control (4)	0	1	GVRP15	GVR14	GVRP13	GVRP12	GVRP11	GVRP10	0	GPRP94	GPRP93	GPRP92	GPRP91	GPRP90	GPRP83	GPRP82	GPRP81	GPRP80
										0									
R44h	G- γ control (1)	0	1	GPRN13	GPRN12	GPRN11	GPRN10	GPRN04	GPRN03	GPRN02	GPRN01	GPRN00	0	GVRN05	GVR04	GVRN03	GVRN02	GVRN01	GVRN00
													0						
R45h	G- γ control (2)	0	1	GSRN03	GSRN02	GSRN01	GSRN00	GPRN43	GPRN42	GPRN41	GPRN40	GPRN33	GPRN32	GPRN31	GPRN30	0	GPRN22	GPRN21	GPRN20
																0			

R46h	G- γ control (3)	0	1	0	GPRN72	GPRN71	GPRN70	0	GPRN63	GPRN62	GPRN61	GPRN60	0	0	0	GPRN53	GPRN52	GPRN51	GPRN50
				0				0					0	0	0				
R47h	G- γ control (4)	0	1	GVRN15	GVR14	GVRN13	GVRN12	GVRN11	GVRN10	0	GPRN94	GPRN93	GPRN92	GPRN91	GPRN90	GPRN83	GPRN82	GPRN81	GPRN80
										0									
R50h	B+ γ control (1)	0	1	BPRP13	BPRP12	BPRP11	BPRP10	BPRP04	BPRP03	BPRP02	BPRP01	BPRP00	0	BVRP05	BVR04	BVRP03	BVRP02	BVRP01	BVRP00
													0						
R51h	B+ γ control (2)	0	1	BSRP03	BSRP02	BSRP01	BSRP00	BPRP43	BPRP42	BPRP41	BPRP40	BPRP33	BPRP32	BPRP31	BPRP30	0	BPRP22	BPRP21	BPRP20
																0			
R52h	B+ γ control (3)	0	1	0	BPRP72	BPRP71	BPRP70	0	BPRP63	BPRP62	BPRP61	BPRP60	0	0	0	BPRP53	BPRP52	BPRP51	BPRP50
				0				0					0	0	0				
R53h	B+ γ control (4)	0	1	BVRP15	BVR14	BVRP13	BVRP12	BVRP11	BVRP10	0	BPRP94	BPRP93	BPRP92	BPRP91	BPRP90	BPRP83	BPRP82	BPRP81	BPRP80
										0									
R54h	B- γ control (1)	0	1	BPRN13	BPRN12	BPRN11	BPRN10	BPRN04	BPRN03	BPRN02	BPRN01	BPRN00	0	BVRN05	BVR04	BVRN03	BVRN02	BVRN01	BVRN00
													0						
R55h	B- γ control (2)	0	1	BSRN03	BSRN02	BSRN01	BSRN00	BPRN43	BPRN42	BPRN41	BPRN40	BPRN33	BPRN32	BPRN31	BPRN30	0	BPRN22	BPRN21	BPRN20
																0			
R56h	B- γ control (3)	0	1	0	BPRN72	BPRN71	BPRN70	0	BPRN63	BPRN62	BPRN61	BPRN60	0	0	0	BPRN53	BPRN52	BPRN51	BPRN50
				0				0					0	0	0				
R57h	B- γ control (4)	0	1	BVRN15	BVR14	BVRN13	BVRN12	BVRN11	BVRN10	0	BPRN94	BPRN93	BPRN92	BPRN91	BPRN90	BPRN83	BPRN82	BPRN81	BPRN80
										0									
R28h	VCOMDC MTP	0	1	0	0	0	0	0	0	0	0	0	0	0	0	CCB3	CCB2	CCB1	CCB0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: X means hardware defining default setting

Table 7-2: Gamma Registers POR value

Reg#	Register	GAMAS=0	GAMAS=1
R30h	**VRP0**	100000	010010
R30h	**PRP0**	00101	10111
R30h	**PRP1**	1010	0111
R31h	**PRP2**	110	111
R31h	**PRP3**	1000	1011
R31h	**PRP4**	1010	1111
R31h	**SRP0**	1111	1111
R32h	**PRP5**	1000	1010
R32h	**PRP6**	0111	0101
R32h	**PRP7**	011	011
R33h	**PRP8**	0111	011
R33h	**PRP9**	11001	10000
R33h	**VRP1**	010000	110100
R34h	**VRN0**	100101	101110
R34h	**PRN0**	01000	11101
R34h	**PRN1**	1100	1111
R35h	**PRN2**	111	111
R35h	**PRN3**	1100	1101
R35h	**PRN4**	0110	1101
R35h	**SRN0**	1111	1101
R36h	**PRN5**	1011	1010
R36h	**PRN6**	0111	0101
R36h	**PRN7**	101	0100
R37h	**PRN8**	1001	1001
R37h	**PRN9**	10001	01000
R37h	**VRN1**	001111	001001
R03h	**BT[3:0]**	040E	010E
R04h	**OLO**	2400	2400
R0Bh	**BTP[1:0]**	D800	D800
R0Ch	**VRC[2:0], VRM[2:0]**	0055	0055
R0Dh	**VRH[3:0]**	0C0C	0F0F
R1Fh	**VCMR[7:0]**	0032	0026
R16h	**HBP[6:0]**	EF8E	EF8E

8 COMMAND DESCRIPTION

Index (IR)

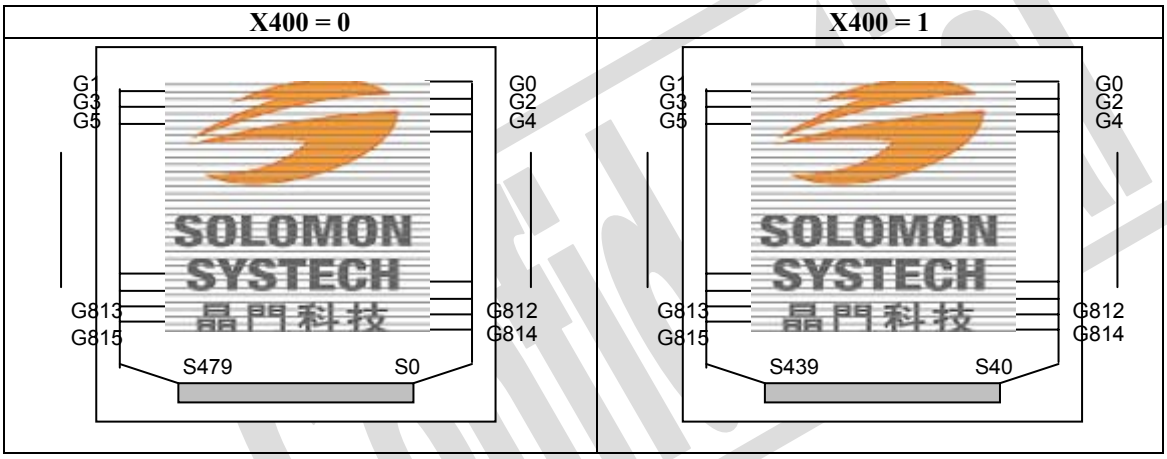
R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index instruction specifies the RAM control indexes (R00h to R7Fh). It sets the register number in the range of 0000000 to 1111111 in binary form. But do not access to Index register and instruction bits which do not have it's own index register.

Driver Output Control (R01h) (POR = XX0Fh)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X400	RL	REV	0	BGR	0	TB	1	0	0	0	0	1	1	1	1
POR		X	X	X	0	X	0	X	1	0	0	0	0	1	1	1	1

X400: When X400="0", full 480 sources are in operation When X400="1", only 400 sources at the center are in operation. First data will appear at S40.



RL: Selects the output shift direction of the source driver of stripe type. When RL = "1", S0 shifts to S480 and 1st pixel color is assigned from S1. When RL = "0", S480 shifts to S0 and 1st pixel color is assigned from S480. Set RL bit and BGR bit when changing the dot order of R, G and B.

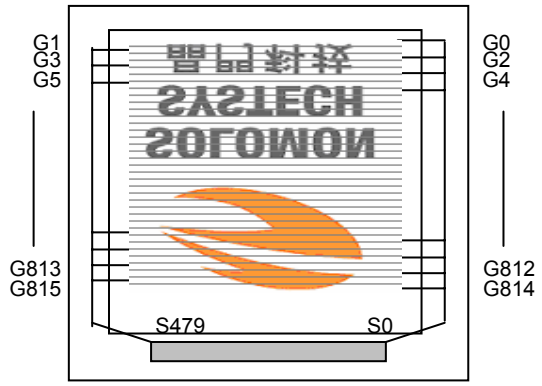
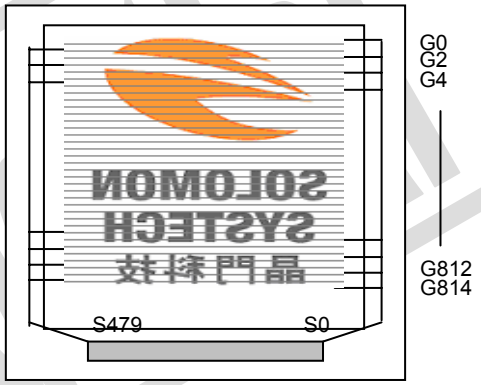
REV: Displays all character and graphics display sections with reversal when REV = "1". Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels. Source output level is indicated below.

REV	RGB data	Source Output level	
REV	RGB data	+ve	-ve
	00000000B	V255	-V255
	:	:	:
1	11111111B	V0	-V0
	00000000B	V0	-V0
	:	:	:
0	11111111B	V255	-V255

BGR: Selects the <R><G><B> arrangement. When BGR = "0" <R><G><B> color is assigned from G0. When BGR = "1" <B><G><R> color is assigned from G0.

TB: Selects the output shift direction of the gate driver. When TB = “1”, G0 shifts to G815. When TB = “0”, G815 shifts to G0.

Note: **The default setting of register bits X400, RL, REV, BGR and TB are defined by the logic stage of corresponding hardware pins. These bits will override the hardware setting once software command was sent to set the bits.**

	TB = 0	TB = 1
RL = 0		
RL = 1		

LCD-Driving-Waveform Control (1) (R02h) (POR = 0C02h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	DS	B/C	EOR	NW9	NW8	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
POR		0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0

DS: Dot Shift. Toggle the polarity of the first gate line. For DS = "0", select the source output without dot shift. For DS = "1", select the source output with dot shift by one third of a gate.

B/C: Select the liquid crystal drive waveform.

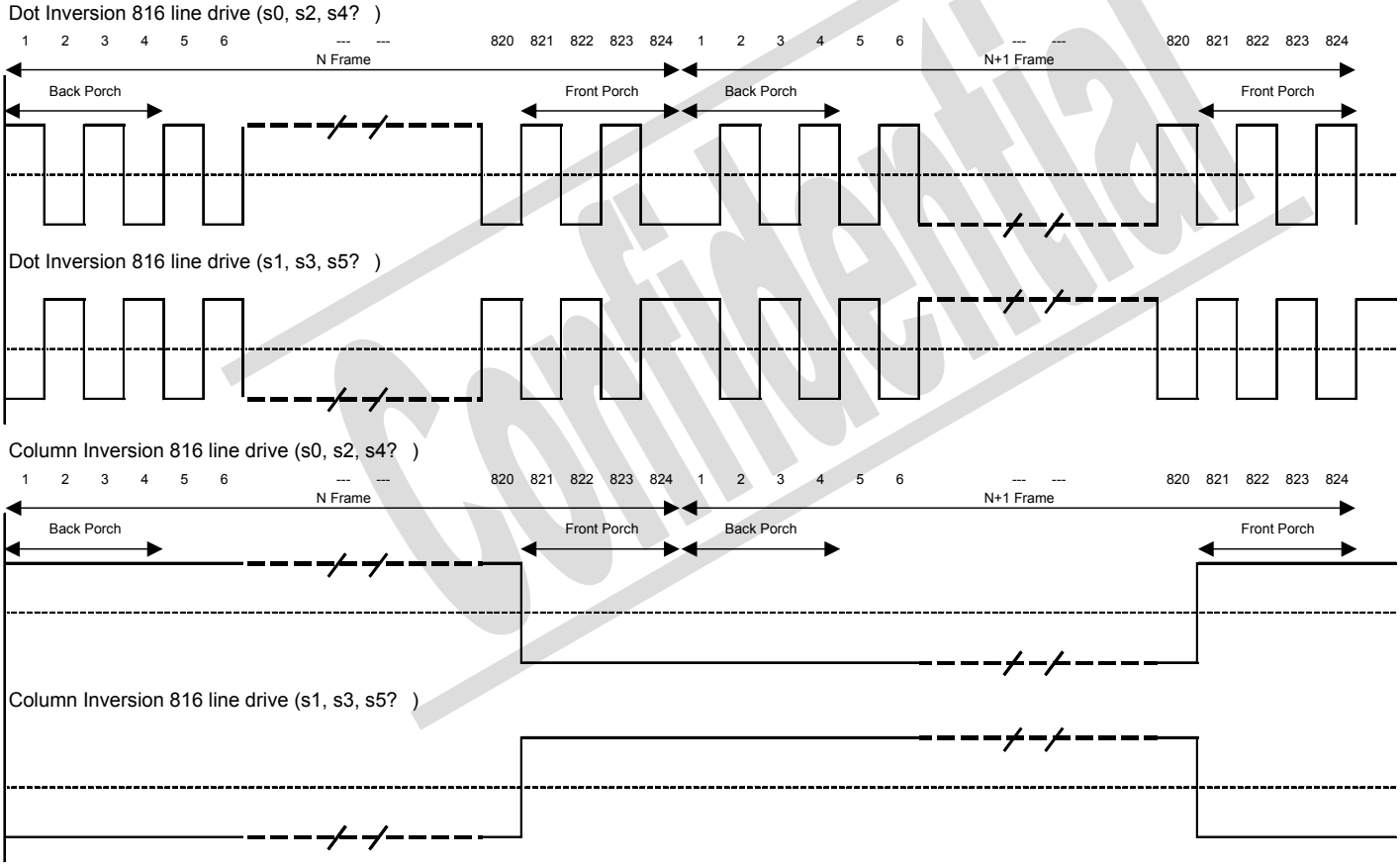
When B/C = 0, column inversion of the LCD driving signal is enabled.

When B/C = 1, a N-line dot inversion waveform is generated and alternates in a N-line equals to NW[9:0]+1.

EOR: When B/C = 1 and EOR = 1, the odd/even frame-select signals and the N-line inversion signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the lines of the LCD driven and the N-lines. When EOR = 0, the polarity counter will not be reset after each frame.

NW9-0: Specify the number of lines that will alternate at the N-line inversion setting (B/C = 1). NW9-0 alternate for every set value + 1 lines.

Figure 8-1: Dot Inversion and Column Inversion



1-line Inversion (Color Pixel Inversion)
B/C = 1, NW[9:0] = 0, DS = 0

		S0	S1	S2	S3	S4	S5
G0	R	+	-	+	-	+	-
	G	-	+	-	+	-	+
	B	+	-	+	-	+	-
G1	R	-	+	-	+	-	+
	G	+	-	+	-	+	-
	B	-	+	-	+	-	+
G2	R	+	-	+	-	+	-
	G	-	+	-	+	-	+
	B	+	-	+	-	+	-

<===>

		S0	S1	S2	S3	S4	S5
G0	R	-	+	-	+	-	+
	G	+	-	+	-	+	-
	B	-	+	-	+	-	+
G1	R	+	-	+	-	+	-
	G	-	+	-	+	-	+
	B	+	-	+	-	+	-
G2	R	-	+	-	+	-	+
	G	+	-	+	-	+	-
	B	-	+	-	+	-	+

1-line Inversion with dot shift
B/C = 1, NW[9:0] = 0, DS = 1

		S0	S1	S2	S3	S4	S5
G0	R	-	+	-	+	-	+
	G	+	-	+	-	+	-
	B	-	+	-	+	-	+
G1	R	+	-	+	-	+	-
	G	-	+	-	+	-	+
	B	+	-	+	-	+	-
G2	R	-	+	-	+	-	+
	G	+	-	+	-	+	-
	B	-	+	-	+	-	+

<===>

		S0	S1	S2	S3	S4	S5
G0	R	+	-	+	-	+	-
	G	-	+	-	+	-	+
	B	+	-	+	-	+	-
G1	R	-	+	-	+	-	+
	G	+	-	+	-	+	-
	B	-	+	-	+	-	+
G2	R	+	-	+	-	+	-
	G	-	+	-	+	-	+
	B	+	-	+	-	+	-

2-line Inversion
B/C = 1, NW[9:0] = 1, DS = 0

		S0	S1	S2	S3	S4	S5
G0	R	+	-	+	-	+	-
	G	+	-	+	-	+	-
	B	-	+	-	+	-	+
G1	R	-	+	-	+	-	+
	G	+	-	+	-	+	-
	B	+	-	+	-	+	-
G2	R	-	+	-	+	-	+
	G	-	+	-	+	-	+
	B	+	-	+	-	+	-

<===>

		S0	S1	S2	S3	S4	S5
G0	R	-	+	-	+	-	+
	G	-	+	-	+	-	+
	B	+	-	+	-	+	-
G1	R	+	-	+	-	+	-
	G	-	+	-	+	-	+
	B	-	+	-	+	-	+
G2	R	+	-	+	-	+	-
	G	-	+	-	+	-	+
	B	-	+	-	+	-	+

2-line Inversion with dot shift
B/C = 1, NW[9:0] = 1, DS = 1

		S0	S1	S2	S3	S4	S5
G0	R	+	-	+	-	+	-
	G	-	+	-	+	-	+
	B	-	+	-	+	-	+
G1	R	+	-	+	-	+	-
	G	+	-	+	-	+	-
	B	-	+	-	+	-	+
G2	R	-	+	-	+	-	+
	G	+	-	+	-	+	-
	B	+	-	+	-	+	-

<===>

		S0	S1	S2	S3	S4	S5
G0	R	-	+	-	+	-	+
	G	+	-	+	-	+	-
	B	+	-	+	-	+	-
G1	R	-	+	-	+	-	+
	G	-	+	-	+	-	+
	B	+	-	+	-	+	-
G2	R	+	-	+	-	+	-
	G	-	+	-	+	-	+
	B	-	+	-	+	-	+

3-line Inversion (Data Pixel Inversion)
B/C = 1, NW[9:0] = 2, DS = 0

		S0	S1	S2	S3	S4	S5
G0	R	+	-	+	-	+	-
	G	+	-	+	-	+	-
	B	+	-	+	-	+	-
G1	R	-	+	-	+	-	+
	G	-	+	-	+	-	+
	B	-	+	-	+	-	+
G2	R	+	-	+	-	+	-
	G	+	-	+	-	+	-
	B	+	-	+	-	+	-

<===>

		S0	S1	S2	S3	S4	S5
G0	R	-	+	-	+	-	+
	G	-	+	-	+	-	+
	B	-	+	-	+	-	+
G1	R	+	-	+	-	+	-
	G	+	-	+	-	+	-
	B	+	-	+	-	+	-
G2	R	-	+	-	+	-	+
	G	-	+	-	+	-	+
	B	-	+	-	+	-	+

3-line Inversion with dot shift
B/C = 1, NW[9:0] = 2, DS = 1

		S0	S1	S2	S3	S4	S5
G0	R	-	+	-	+	-	+
	G	+	-	+	-	+	-
	B	+	-	+	-	+	-
G1	R	+	-	+	-	+	-
	G	-	+	-	+	-	+
	B	-	+	-	+	-	+
G2	R	-	+	-	+	-	+
	G	+	-	+	-	+	-
	B	+	-	+	-	+	-

<===>

		S0	S1	S2	S3	S4	S5
G0	R	+	-	+	-	+	-
	G	-	+	-	+	-	+
	B	-	+	-	+	-	+
G1	R	-	+	-	+	-	+
	G	+	-	+	-	+	-
	B	+	-	+	-	+	-
G2	R	+	-	+	-	+	-
	G	-	+	-	+	-	+
	B	-	+	-	+	-	+

Column Inversion
B/C = 0, DS = 0

		S0	S1	S2	S3	S4	S5
G0	R	+	-	+	-	+	-
	G	+	-	+	-	+	-
	B	+	-	+	-	+	-
G1	R	+	-	+	-	+	-
	G	+	-	+	-	+	-
	B	+	-	+	-	+	-
G2	R	+	-	+	-	+	-
	G	+	-	+	-	+	-
	B	+	-	+	-	+	-

<===>

		S0	S1	S2	S3	S4	S5
G0	R	-	+	-	+	-	+
	G	-	+	-	+	-	+
	B	-	+	-	+	-	+
G1	R	-	+	-	+	-	+
	G	-	+	-	+	-	+
	B	-	+	-	+	-	+
G2	R	-	+	-	+	-	+
	G	-	+	-	+	-	+
	B	-	+	-	+	-	+

Column Inversion with dot shift
B/C = 0, DS = 1

		S0	S1	S2	S3	S4	S5
G0	R	+	-	+	-	+	-
	G	+	-	+	-	+	-
	B	+	-	+	-	+	-
G1	R	+	-	+	-	+	-
	G	+	-	+	-	+	-
	B	+	-	+	-	+	-
G2	R	+	-	+	-	+	-
	G	+	-	+	-	+	-
	B	+	-	+	-	+	-

<===>

		S0	S1	S2	S3	S4	S5
G0	R	-	+	-	+	-	+
	G	-	+	-	+	-	+
	B	-	+	-	+	-	+
G1	R	-	+	-	+	-	+
	G	-	+	-	+	-	+
	B	-	+	-	+	-	+
G2	R	-	+	-	+	-	+
	G	-	+	-	+	-	+
	B	-	+	-	+	-	+

Power control 1 (R03h) (POR = E40Eh)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DCM3	DCM2	DCM1	DCM0	0	BT2	BT1	BT0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
POR		1	1	1	0	0	1	0	0	0	0	0	0	1	1	1	0

DCM3-0: Set the step-up cycle of the negative step-up circuit. When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

DC3	DC2	DC1	DC0	No. of dotclk
0	0	0	0	52 (POR)
0	0	0	1	64
0	0	1	0	70
0	0	1	1	86
0	1	0	0	84
0	1	0	1	104
0	1	1	0	104
0	1	1	1	128
1	0	0	0	208
1	0	0	1	256
1	0	1	1	416
1	0	1	1	512

Note: For 416 dotclk per line, Horizontal line frequency (f_H Typ. 14.8kHz, when dotclk=6.14MHz)
For 512 dotclk per line, Horizontal line frequency (f_H Typ. 16.7kHz, when dotclk=8.54MHz)

For other number of dotclk per line, the Step up frequency will be automatically divided wthin each Fline.

DC3	DC2	DC1	DC0	Step-up cycle
1	1	0	0	Fline × 1 (max dotclk = 512)
1	1	0	1	Fline × 2
1	1	1	0	Fline × 4
1	1	1	1	Fline × 8

BT2-0: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power-supply voltage to be used.

BT2	BT1	BT0	V_{GH} output	V_{GL} output	V_{GH} booster ratio	V_{GL} booster ratio
0	0	0	AVDD x 3	-(VGH - VCI)	+6	-5
0	0	1	AVDD x 3	-(VGH - AVDD)	+6	-4
0	1	0	AVDD x 3	-(AVDD x 3)	+6	-6
0	1	1	AVDD x 2 + VCI	-(VGH)	+5	-5
1	0	0	AVDD x 2 + VCI	-(VGH - VCI)	+5	-4
1	0	1	AVDD x 2 + VCI	-(VGH - AVDD)	+5	-3
1	1	0	AVDD x 2	-(VGH)	+4	-4
1	1	1	AVDD x 2	-(VGH - VCI)	+4	-3

DC3-0: Set the step-up cycle of the positive step-up circuit. When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

DC3	DC2	DC1	DC0	No. of dotclk
0	0	0	0	52 (POR)
0	0	0	1	64
0	0	1	0	70
0	0	1	1	86
0	1	0	0	84
0	1	0	1	104
0	1	1	0	104
0	1	1	1	128
1	0	0	0	208
1	0	0	1	256
1	0	1	1	416
1	0	1	1	512

Note: For 416 dotclk per line, Horizontal line frequency (f_H Typ. 14.8kHz, when dotclk=6.14MHz)
For 512 dotclk per line, Horizontal line frequency (f_H Typ. 16.7kHz, when dotclk=8.54MHz)

For other number of dotclk per line, the Step up frequency will be automatically divided wthin each Fline.

DC3	DC2	DC1	DC0	Step-up cycle
1	1	0	0	Fline × 1 (max dotclk = 512)
1	1	0	1	Fline × 2
1	1	1	0	Fline × 4
1	1	1	1	Fline × 8

AP2-0: Adjust the amount of current from the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current taking into account the power consumption. While there is no display, such as the system is in a sleep mode, AP2-0 can be set to (0,0,0) and shutting down the operational amplifier can reduce the power consumption.

AP2	AP1	AP0	Op-amp power
0	0	0	Least
0	0	1	Small
0	1	0	Small to medium
0	1	1	Medium
1	0	0	Medium to large
1	0	1	Large
1	1	0	Large to Maximum
1	1	1	Maximum

Driver output control (2) (R04h) (POR = 2400h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DISP2	DISP1	DISP0	0	0	OLO	0	0	FSE7	FSE6	FSE5	FSE4	FSE3	FSE2	FSE1	FSE0
POR		0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0

DISP2:0: Display On / Off Mode Select.

DISP2	DISP1	DISP0	Display Mode	Display (NW panel)	Display (NB panel)
0	0	0	If hardware pin DISP = L	Blank Black data	Blank Black data
0	0	1	If hardware pin DISP = L	Blank White data	Blank White data
1	0	0	If hardware pin DISP = H	Blank Black data	Blank Black data
1	0	1	If hardware pin DISP = H	Blank White data	Blank White data
X	1	1	Input data are valid and write to the data register	Input Data	Input Data
0	1	0	Input data are invalid and write blank data to the data register	Blank Black data	Blank Black data
1	1	0	Input data are invalid and write blank data to the data register	Blank White data	Blank White data

OLO: When OLO = "1", all R, G and B gamma registers are set by one set of gamma control, R30h to R37h.
When OLO = "0", R, G and B gamma registers are set separately by registers R30h to R37h, R40h to R47h and R50h to R57h.

FSE7:0: First Slot Source Charge Sharing End Time

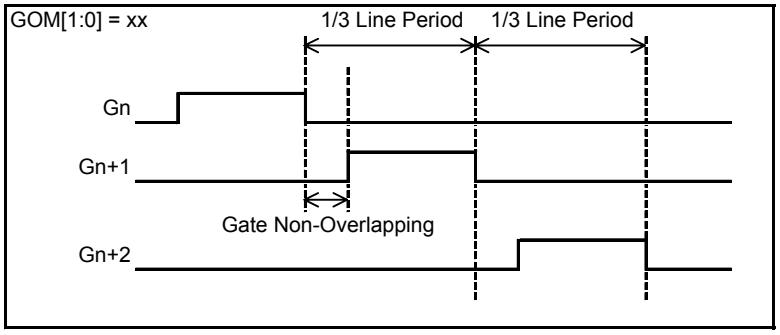
FSE7	FSE6	FSE5	FSE4	FSE3	FSE2	FSE1	FSE0	HSYNC to Source timing
0	0	0	0	0	0	0	0	Follow eq[2:0] definition
0	0	0	0	0	0	0	1	4 dotclk from hsync falling
0	0	0	0	0	0	1	0	6 dotclk from hsync falling
0	0	0	0	0	0	1	1	8 dotclk from hsync falling
:	:	:	:	:	:	:	:	: Step = 2 :
1	1	1	0	0	0	0	0	400 dotclk from hsync falling
1	1	0	0	1	0	0	0	402 dotclk from hsync falling
1	1	0	0	1	0	0	1	Reserved
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	1	1	

Frame Cycle Control (R0Bh) (POR = D804h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	GOM1	GOM0	SDT1	SDT0	EQ1	EQ0	PT1	PT0	EQ2	0	0	0	BTP1	BTP0	SDT2	0
POR		1	1	0	1	1	0	0	0	0	0	0	0	0	1	0	0

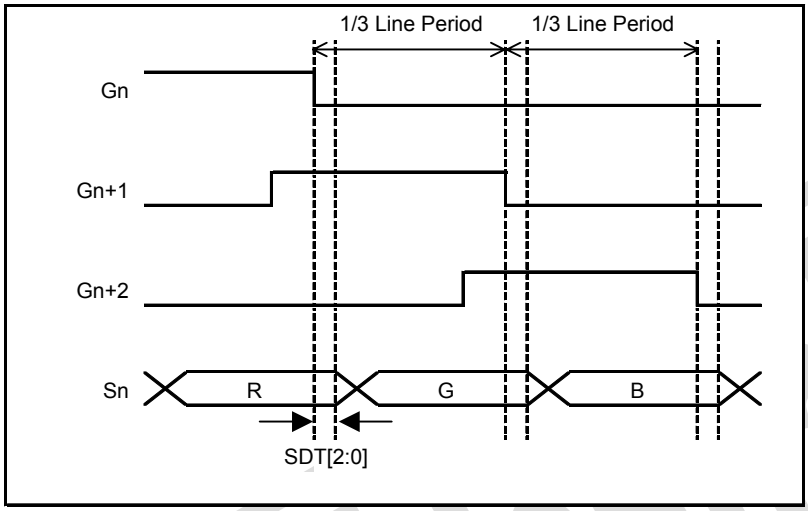
GOM1-0: Sets amount of non-overlap of the gate outputs.

GOM1	GOM0	Gate Output Mode
0	0	Non-overlap: HSYNC_falling + 100 DOTCLK
0	1	Non-overlap: HSYNC _falling + 60 DOTCLK
1	0	Non-overlap: HSYNC _falling + 30 DOTCLK
1	1	Non-overlap: 6 DOTCLK after Source On



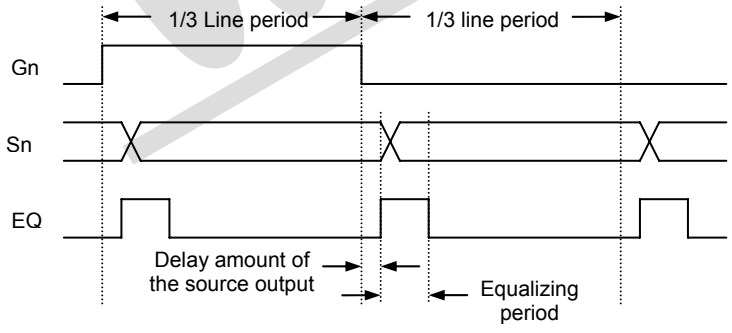
SDT2-0: Set delay amount from the gate output signal falling edge of the source outputs.

SDT2	SDT1	SDT0	Delay amount of the source output
0	0	0	3 DOTCLK
0	0	1	7 DOTCLK
0	1	0	11 DOTCLK
0	1	1	15 DOTCLK
1	0	0	23 DOTCLK
1	0	1	31 DOTCLK
1	1	0	39 DOTCLK
1	1	1	47 DOTCLK



EQ2-0: Sets the equalizing period on source

EQ2	EQ1	EQ0	EQ period
0	0	0	No EQ
0	0	1	8 clock cycle
0	1	0	16 clock cycle
0	1	1	24 clock cycle
1	0	0	32 clock cycle
1	0	1	40 clock cycle
1	1	0	52 clock cycle
1	1	1	63 clock cycle



BTP1-0: Set the Primary booster ratio.

BTP1	BTP0	Primary booster ratio
0	0	Reserved
0	1	2X
1	0	3X
1	1	Reserved

Power Control 3 (R0Dh) (POR = 0C0Ch)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	VDL3	VDL2	VDL1	VDL0	0	0	0	0	VDH3	VDH2	VDH1	VDH0
POR		0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0

VDL3-0: Set amplitude magnification of VLCDL. These bits amplify the VLCDL voltage –1.980 to –3.128 times the Vref voltage set by VDL3-0.

VDL3	VDL2	VDL1	VDL0	VLCDL Voltage
0	0	0	0	Vref x –1.980
0	0	0	1	Vref x –2.078
0	0	1	0	Vref x –2.183
0	0	1	1	Vref x -2.296
0	1	0	0	Vref x -2.399
0	1	0	1	Vref x -2.508
0	1	1	0	Vref x -2.605
0	1	1	1	Vref x -2.707
1	0	0	0	Vref x -2.793
1	0	0	1	Vref x -2.838
1	0	1	0	Vref x -2.883
1	0	1	1	Vref x -2.930
1	1	0	0	Vref x -2.978
1	1	0	1	Vref x -3.027
1	1	1	0	Vref x -3.077
1	1	1	1	Vref x -3.128

Note: Vref is the internal reference voltage equals to 2.0V.

VDH3-0: Set amplitude magnification of VLCDH. These bits amplify the VLCDH voltage 2.023 to 3.158 times the Vref voltage set by VDH3-0.

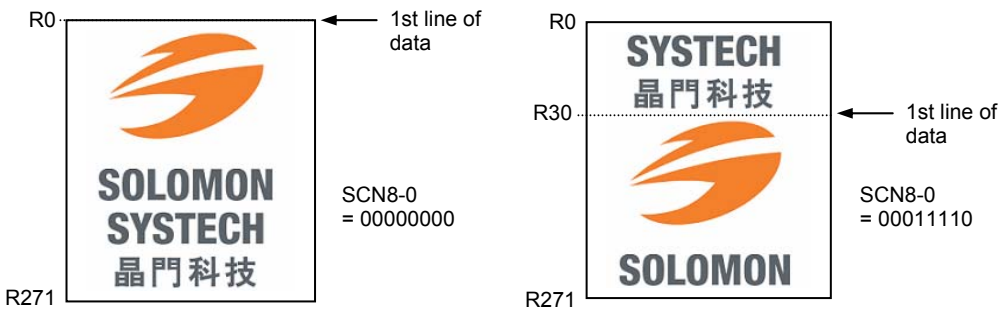
VDH3	VDH2	VDH1	VDH0	VLCDH Voltage
0	0	0	0	Vref x 2.023
0	0	0	1	Vref x 2.093
0	0	1	0	Vref x 2.169
0	0	1	1	Vref x 2.250
0	1	0	0	Vref x 2.338
0	1	0	1	Vref x 2.400
0	1	1	0	Vref x 2.500
0	1	1	1	Vref x 2.576
1	0	0	0	Vref x 2.647
1	0	0	1	Vref x 2.728
1	0	1	0	Vref x 2.813
1	0	1	1	Vref x 2.903
1	1	0	0	Vref x 3.000
1	1	0	1	Vref x 3.051
1	1	1	0	Vref x 3.104
1	1	1	1	Vref x 3.158

Note: Vref is the internal reference voltage equals to 2.0V.

Row Scan Position (R0Fh) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SCN8	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCN8-0: Set the scanning starting position of the gate driver.



Pixel per line (R16h) (POR = EF8Eh when x400=0, POR = C786h when x400=1)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
POR(x400=0)		1	1	1	0	1	1	1	1	1	0	0	0	1	1	1	0
POR(x400=1)		1	1	0	0	0	1	1	1	1	0	0	0	0	1	1	0

Note: Number of dotclk for hsync active low period must be smaller than that of HBP
Only for 24-bit, 18-bit parallel and 8-bit, 6-bit serial interface.

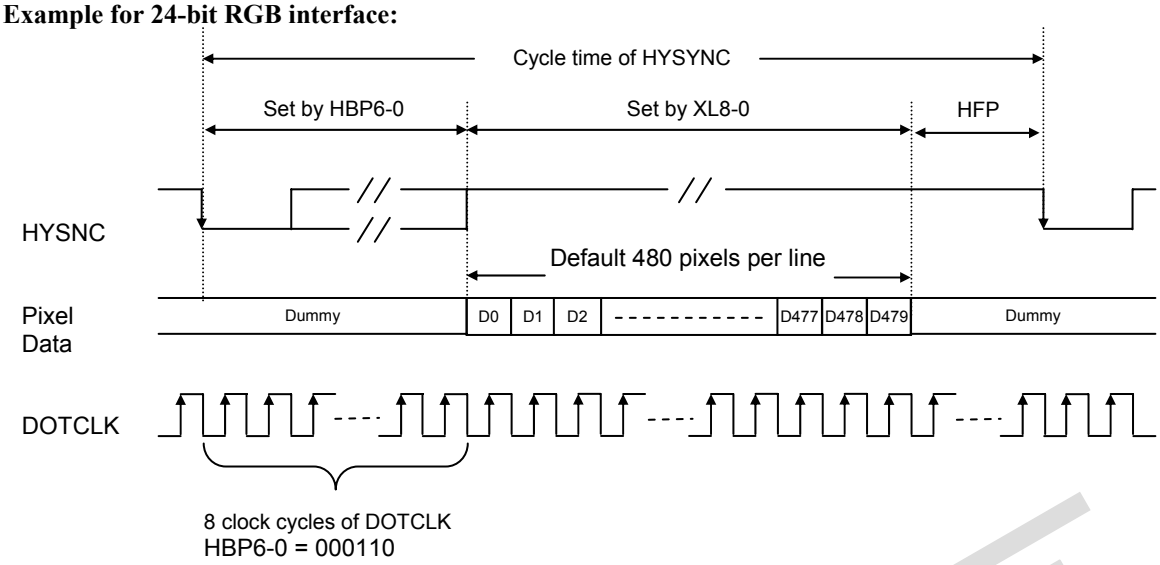
XL8-0: Set the number of valid pixel per line.

XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	No. of pixel per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
				: : :					: Step = 1 :
1	1	0	0	0	1	1	1	0	399
1	1	0	0	0	1	1	1	1	400 (por if x400=1)
				: : :					: Step = 1 :
1	1	1	0	1	1	1	1	0	479
1	1	1	0	1	1	1	1	1	480 (por if x400=0)
1	1	1	1	*	*	*	*	*	Reserved

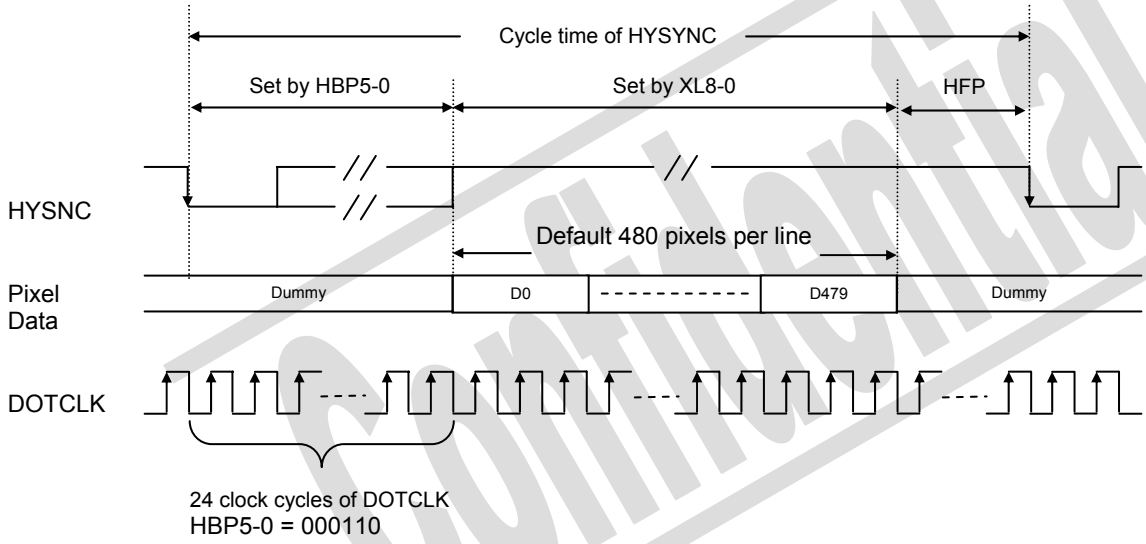
HBP6-0: Set the delay period from falling edge of HSYNC signal to first valid data.

HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle of DOTCLK	
							24-bit RGB	8-bit RGB (without dummy)
0	0	0	0	0	0	0	2	6
0	0	0	0	0	0	1	3	9
0	0	0	0	0	1	0	4	12
0	0	0	0	0	1	1	5	15
0	0	0	0	1	0	0	6	18
0	0	0	0	1	0	1	7	21
0	0	0	0	1	1	0	8 (por if x400=1)	24
0	0	0	0	1	1	1	9	27
0	0	0	1	0	0	0	10	30
0	0	0	1	0	0	1	11	33
0	0	0	1	0	1	0	12	36
0	0	0	1	0	1	1	13	39
0	0	0	1	1	0	0	14	42
0	0	0	1	1	0	1	15	45
0	0	0	1	1	1	0	16 (por if x400=0)	48
			: : :				: Step = 1 :	:Step = 3
1	1		1	1	1	0	128	384
1	1	1	1	1	1	1	129	387

Example for 24-bit RGB interface:



Example for 8-bit RGB interface (without dummy):



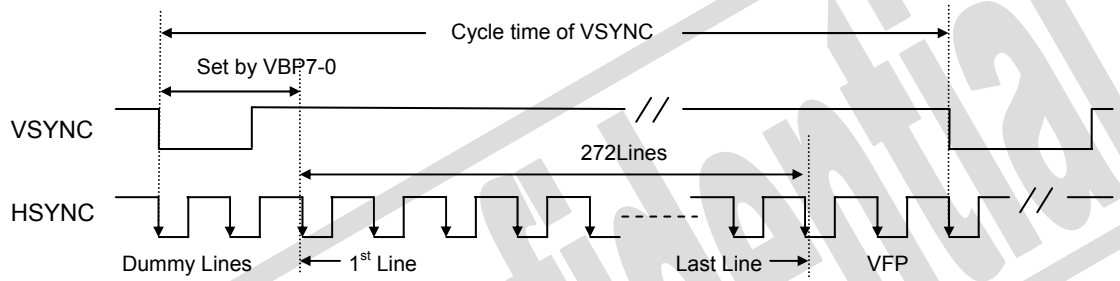
Vertical Porch (R17h) (POR = 0003h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

VBP7-0: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line.

VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
0	0	0	0	0	1	0	0	5
:	:	:	:	:	:	:	:	: Step = 1 :
1	1	0	1	1	1	1	1	224
1	1	1	0	0	0	0	0	225
1	1	1	*	*	*	*	*	Reserved

Example for 24-bit RGB interface:



Power Control 5 (R1Eh) (POR = 0029h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	nMTP	0	VCM7	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
POR		0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1

nMTP: nMTP equals to "0" after power on reset and VCOMDC voltage equals to programmed MTP value. When nMTP set to "1", setting of VCM7-0 becomes valid and voltage of VCOMDC can be adjusted.

VCM7-0: Set the VCOMDC voltage if nMTP = "1". These bits vary the VCOMDC voltage from –2.55V to 0V.

VCM7	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMDC
0	0	0	0	0	0	0	0	-2.55
0	0	0	0	0	0	0	1	-2.54
:	:	:	:	:	:	:	:	: Step = 0.01 :
1	1	1	1	1	1	1	0	-0.01
1	1	1	1	1	1	1	1	0.00

Note: VCOMDC = (-vref/200) xVCM<7:0> where vref = 2.0V

9 EXTENDED COMMAND DESCRIPTION

Reminder – In order to activate extended command, user is required to send R28h-0006 prioir to the extended command in application. See below for further description on the R28h register.

VCOMDC MTP (R28h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	CCB3	CCB2	CCB1	CCB0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CCB3-0: Command Control Bit, the master control of the internal command decoder. This register provides function of software reset and MTP programming.

CCB3	CCB2	CCB1	CCB0	Usage
0	0	0	0	Release Reset or no action
0	1	0	1	Driver initialization
0	1	1	0	Enable extended test command/ Enable for MTP Programming
1	0	0	0	Erase MTP
1	0	1	0	Fire MTP
1	1	1	0	Reset all command bits to default
All other setting				Reserved

10 MTP PROGRAMMING / ERASE

MTP Programming sequence

Remark: * The application setup should be synchronized.
Note1: nMTP must set to “0” to activate the MTP effect.
Note2: VCI is suggested to be 3.3V during fire MTP.

Precaution:

1. All capacitors on MTP machine should be discharged completely before placing the LCD module.
2. The MTP programming voltage should not be applied when placing and removing the LCD module.
3. The MTP programming voltage should not be applied before VDDIO/VDDEXT/VCI.
4. After MTP is finished, the capacitors at VPP and AVDD must be discharged completely before removing the LCD module.

Figure 10-1: MTP programming circuitry

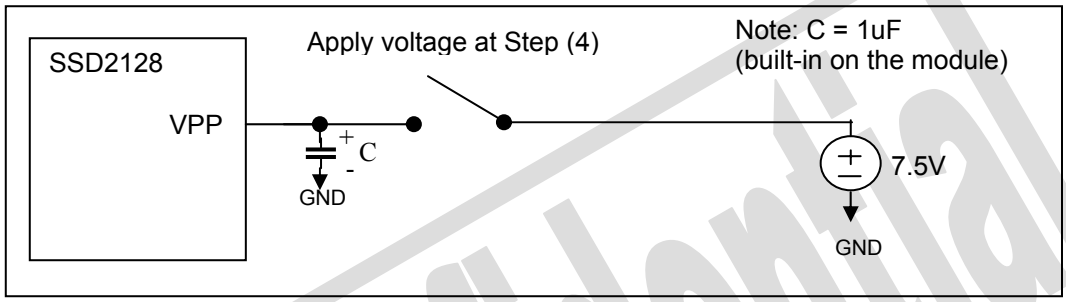
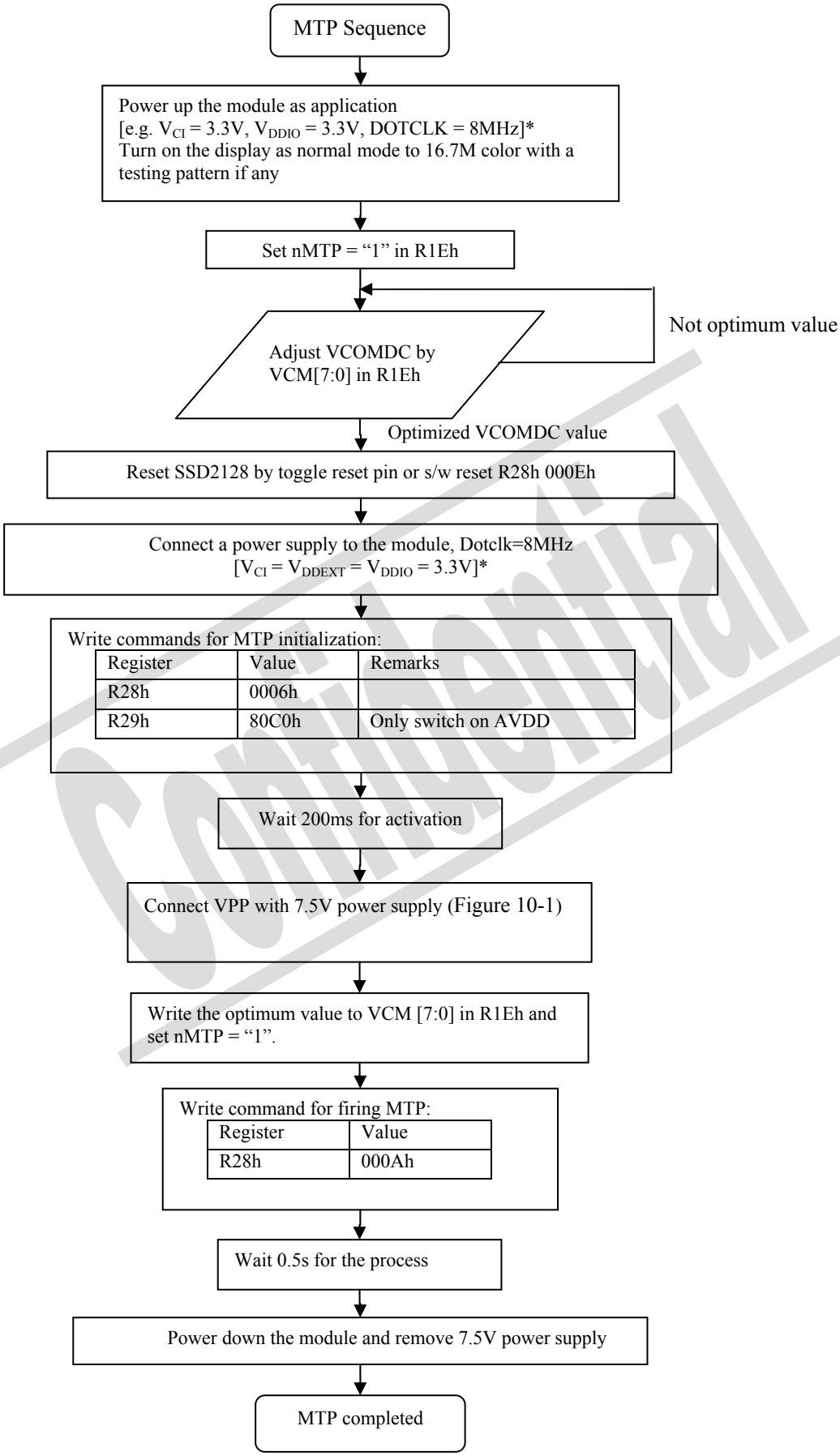


Figure 10-2: MTP Programming Flowchart



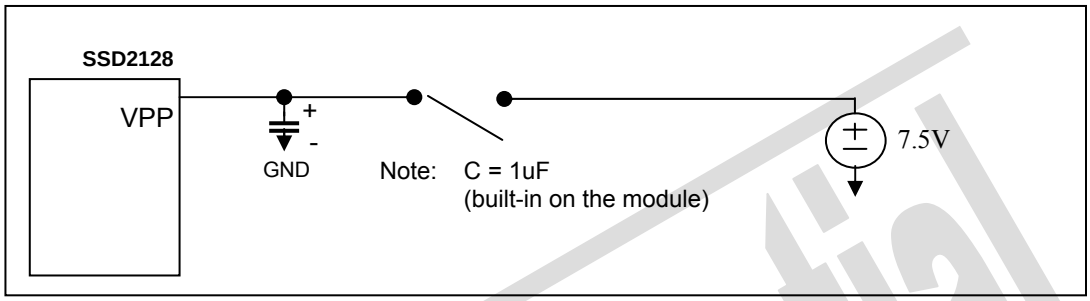
MTP Erase sequence

Remark: * The application setup should be synchronized.

Precaution:

1. All capacitors on MTP machine should be discharged completely before placing the LCD module.
2. The MTP erase voltage should not be applied when placing and removing the LCD module.
3. The MTP erase voltage should not be applied before $V_{DDIO}/V_{DDEXT}/V_{CI}$.
4. After Erasing MTP is finished, the capacitors at VPP and AVDD must be discharged completely before removing the LCD module.

Figure 10-3: MTP Erase circuitry



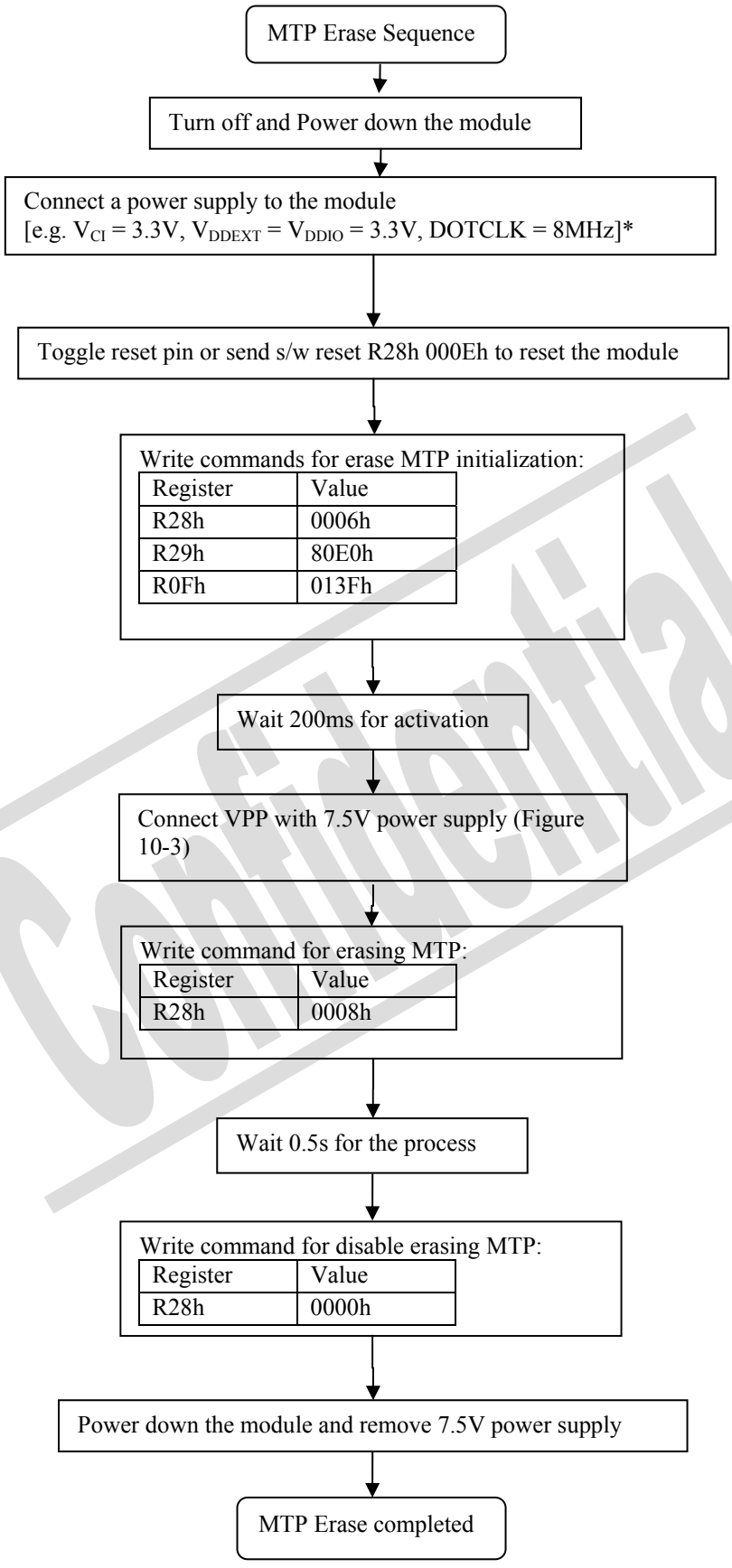
MTP Re-Write cycle

Table 10-1: MTP Re-write cycle

Characteristics	Symbol	Min	Typ	Max	Units
Re-write Cycle	N	-	-	4	Cycle
Power Supply voltage for programming	VPP	7.25	7.5	7.75	V
Power Supply voltage for erase	VPP	7.25	7.5	7.75	V
Program Pixel Clock	t_{PIXCLK}	-	8	-	MHz
Program time	Tprog	-	0.5	-	s
Erase Pixel Clock	t_{PIXCLK}	-	8	-	s
Erase time	Terase	-	0.5	-	s

Note: The suggested value is based on IC evaluation result which does not include ITO resistance.

Figure 10-4: MTP Erase Flowchart



11 GAMMA ADJUSTMENT FUNCTION

The SSD2128 incorporates gamma adjustment function for the 16.7M-color display. Gamma adjustment is implemented by deciding the 12-grayscale levels with micro gradient adjustment and amplitude adjustment register for each of the internal positive and negative polarity with separated register settings for each RGB color. Set up by the liquid crystal panel's specification.

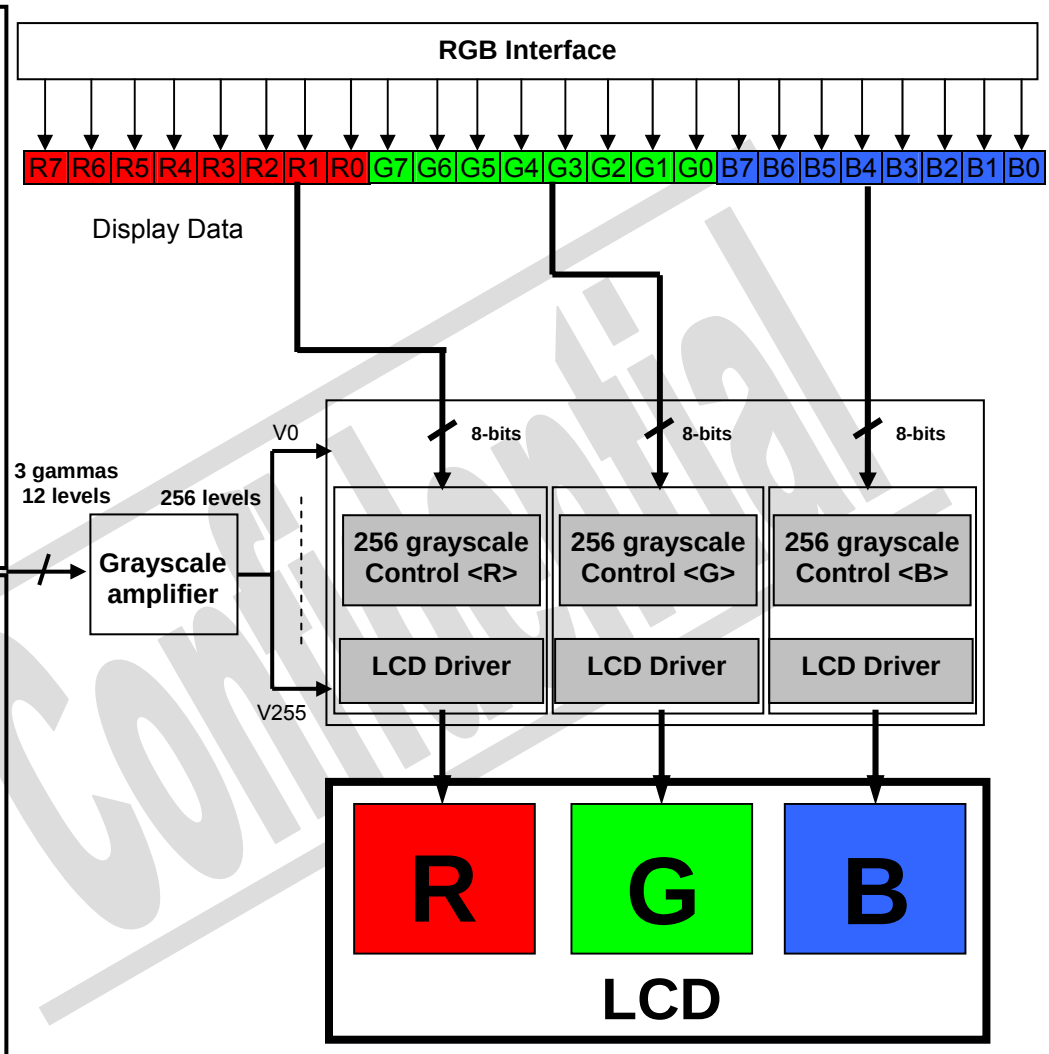
Figure 11-1: Grayscale Control

RED	GREEN	BLUE
VRP00[5:0]	VRP10[5:0]	VRP20[5:0]
VRP01[5:0]	VRP11[5:0]	VRP21[5:0]
PRP00[4:0]	PRP10[4:0]	PRP20[4:0]
PRP01[3:0]	PRP11[3:0]	PRP21[3:0]
PRP02[2:0]	PRP12[2:0]	PRP22[2:0]
PRP03[3:0]	PRP13[3:0]	PRP23[3:0]
PRP04[3:0]	PRP14[3:0]	PRP24[3:0]
PRP05[3:0]	PRP15[3:0]	PRP25[3:0]
PRP06[3:0]	PRP16[3:0]	PRP26[3:0]
PRP07[2:0]	PRP17[2:0]	PRP27[2:0]
PRP08[3:0]	PRP18[3:0]	PRP28[3:0]
VRP09[4:0]	VRP19[4:0]	VRP29[4:0]
SRP00[3:0]	SRP10[3:0]	SRP20[3:0]

Positive polarity register

RED	GREEN	BLUE
VRN00[5:0]	VRN10[5:0]	VRN20[5:0]
VRN01[5:0]	VRN11[5:0]	VRN21[5:0]
PRN00[4:0]	PRN10[4:0]	PRN20[4:0]
PRN01[3:0]	PRN11[3:0]	PRN21[3:0]
PRN02[2:0]	PRN12[2:0]	PRN22[2:0]
PRN03[3:0]	PRN13[3:0]	PRN23[3:0]
PRN04[3:0]	PRN14[3:0]	PRN24[3:0]
PRN05[3:0]	PRN15[3:0]	PRN25[3:0]
PRN06[3:0]	PRN16[3:0]	PRN26[3:0]
PRN07[2:0]	PRN17[2:0]	PRN27[2:0]
PRN08[3:0]	PRN18[3:0]	PRN28[3:0]
VRN09[4:0]	VRN19[4:0]	VRN29[4:0]
SRN00[3:0]	SRN10[3:0]	SRN20[3:0]

Negative polarity register



11.1 Structure of Grayscale Amplifier

Below figure indicates the structure of the grayscale amplifier. It determines 12 levels (VIN0-VIN-11) by the micro gradient adjuster and the amplitude register. Also, dividing these levels with ladder resistors generates V0 to V255.

Figure 11-2: Structure of grayscale amplifier

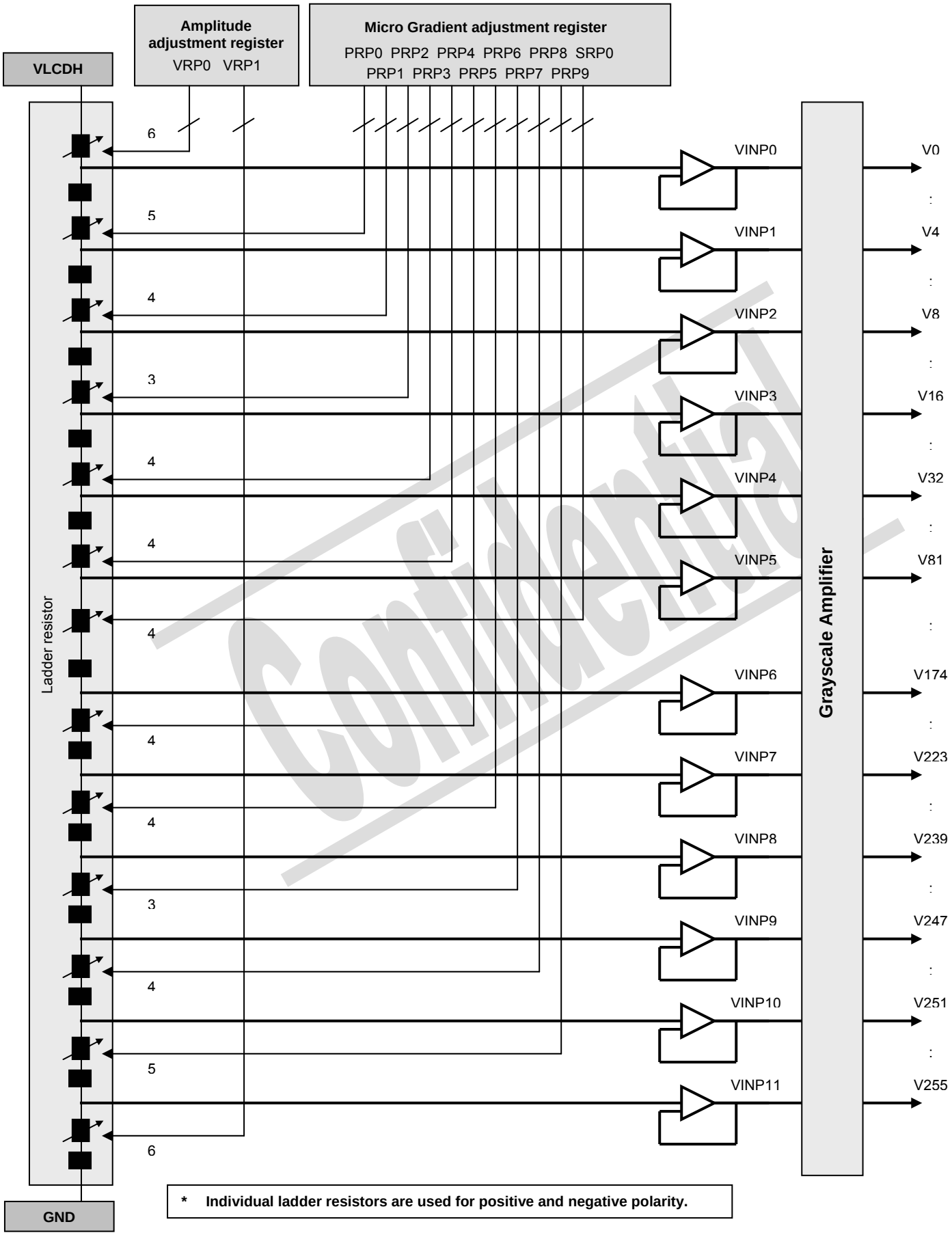
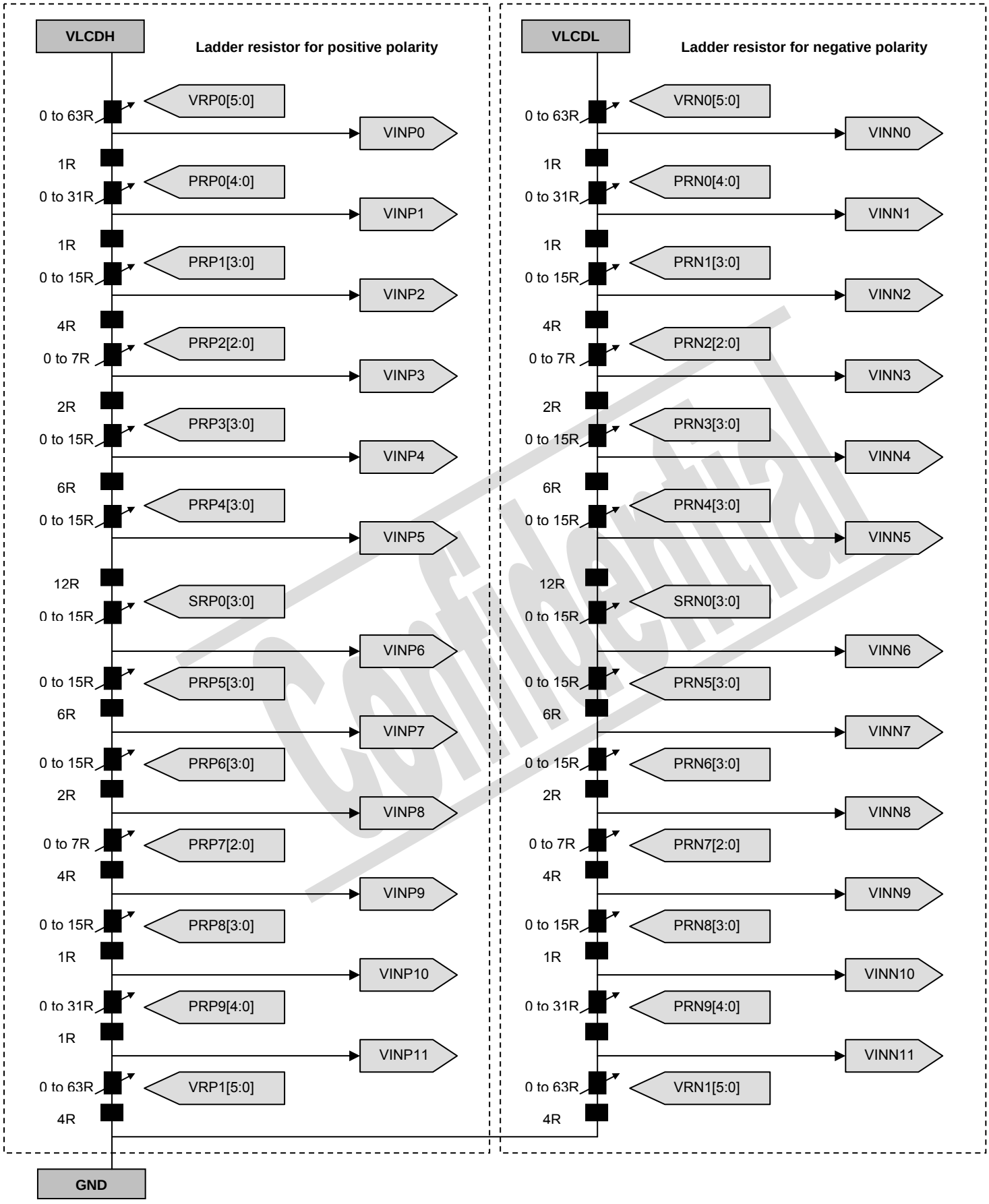


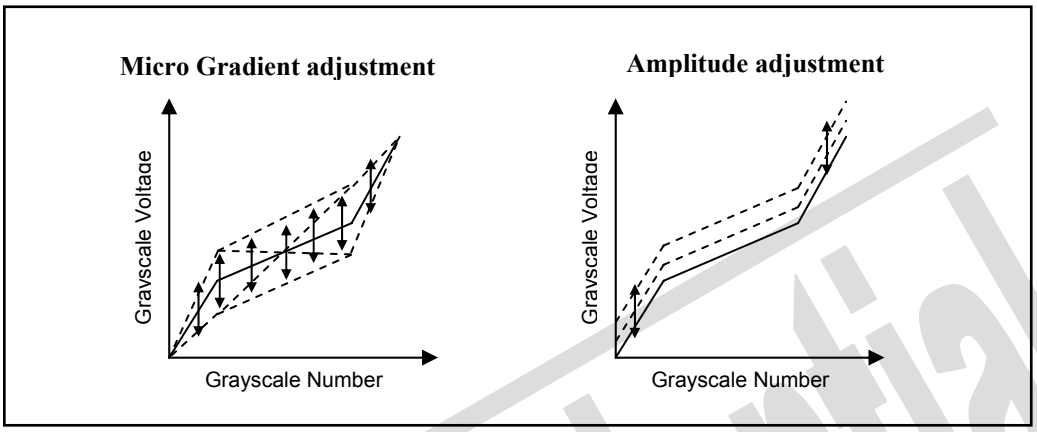
Figure 11-3: Structure of Ladder resistor



11.2 Gamma Adjustment Register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are three types of register groups to adjust gradient and amplitude on number of the grayscale, characteristics of the grayscale voltage. R.G.B. grayscale voltage can be adjusted individually. Following graphics indicates the operation of each adjusting register.

Figure 11-4: Gamma Adjustment Function



Micro gradient adjusting register

The micro gradient-adjusting resistor is to make subtle adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistors in the middle of the ladder resistor by registers (PRP(N)0 - PRP(N)9) and (SRP(N)) for the grayscale voltage generator. Also, there are independent resistors on the positive/negative polarities in order for corresponding to asymmetry drive.

Amplitude adjusting register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistors in the boundary of the ladder resistor by registers (VRP(N)0 / VRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

11.3 Ladder Resistor / Grayscale Amplifier

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors with variable resistors for selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors for amplitude adjustment and micro gradient adjustment.

Variable Resistor
There are 4 types of the variable resistors that are for the gradient and amplitude adjustment. The resistance is set by the resistor (PRP(N)0 - PRP(N)9), (SRP(N)0 / SRP(N)1) and (VRP(N)0 / VRP(N)1) as below.

VRP0,VRN0, VRP1,VRN1	Resistance
000000	0R
000001	1R
000010	2R
: Step = 1R :	
111101	61R
111110	62R
111111	63R

PRP0,PRN0, PRP9,PRN9	Resistance
00000	0R
00001	1R
00010	2R
: Step = 1R :	
11101	29R
11110	30R
11111	31R

PRP1,PRN1, PRP3,PRN3, PRP4,PRN4, PRP5,PRN5, PRP6,PRN6, PRP8,PRN8, SRP0,SRN0	Resistance
0000	0R
0001	1R
0010	2R
: Step = 1R :	
1101	13R
1110	14R
1111	15R

PRP2,PRN2, PRP7,PRN7	Resistance
000	0R
001	1R
010	2R
011	3R
100	4R
101	5R
110	6R
111	7R

Figure 11-5: Gamma Curve for DC-VCOM

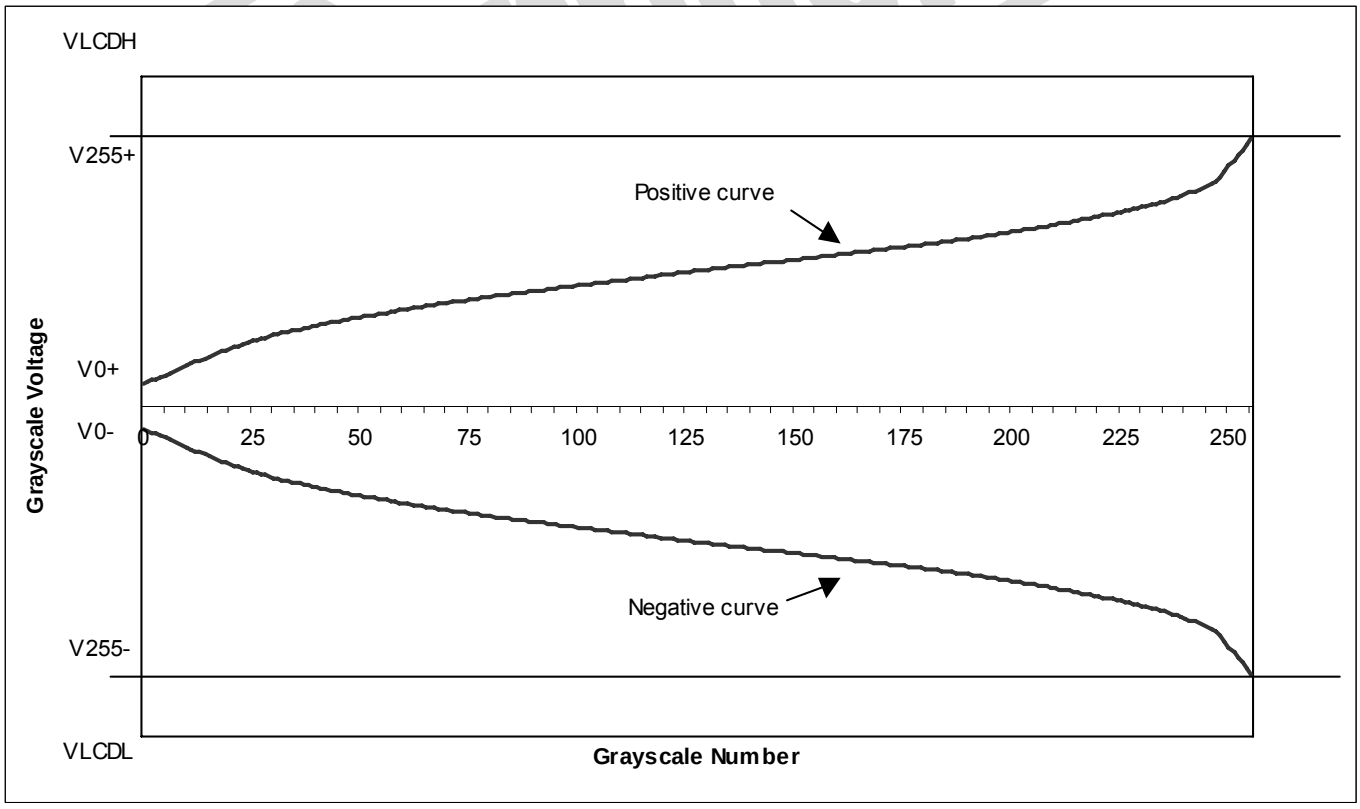


Table 11-1: Grayscale voltage Formula

Grayscale voltage	Formula	Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP(N)0	V43	(V32-V81)*(38/49)+V81	V86	(V81-V174)*(88/93)+V174
V1	(V0-V4)*(3/4)+V4	V44	(V32-V81)*(37/49)+V81	V87	(V81-V174)*(87/93)+V174
V2	(V0-V4)*(2/4)+V4	V45	(V32-V81)*(36/49)+V81	V88	(V81-V174)*(86/93)+V174
V3	(V0-V4)*(1/4)+V4	V46	(V32-V81)*(35/49)+V81	V89	(V81-V174)*(85/93)+V174
V4	VINP(N)1	V47	(V32-V81)*(34/49)+V81	V90	(V81-V174)*(84/93)+V174
V5	(V4-V8)*(3/4)+V8	V48	(V32-V81)*(33/49)+V81	V91	(V81-V174)*(83/93)+V174
V6	(V4-V8)*(2/4)+V8	V49	(V32-V81)*(32/49)+V81	V92	(V81-V174)*(82/93)+V174
V7	(V4-V8)*(1/4)+V8	V50	(V32-V81)*(31/49)+V81	V93	(V81-V174)*(81/93)+V174
V8	VINP(N)2	V51	(V32-V81)*(30/49)+V81	V94	(V81-V174)*(80/93)+V174
V9	(V8-V16)*(7/8)+V16	V52	(V32-V81)*(29/49)+V81	V95	(V81-V174)*(79/93)+V174
V10	(V8-V16)*(6/8)+V16	V53	(V32-V81)*(28/49)+V81	V96	(V81-V174)*(78/93)+V174
V11	(V8-V16)*(5/8)+V16	V54	(V32-V81)*(27/49)+V81	V97	(V81-V174)*(77/93)+V174
V12	(V8-V16)*(4/8)+V16	V55	(V32-V81)*(26/49)+V81	V98	(V81-V174)*(76/93)+V174
V13	(V8-V16)*(3/8)+V16	V56	(V32-V81)*(25/49)+V81	V99	(V81-V174)*(75/93)+V174
V14	(V8-V16)*(2/8)+V16	V57	(V32-V81)*(24/49)+V81	V100	(V81-V174)*(74/93)+V174
V15	(V8-V16)*(1/8)+V16	V58	(V32-V81)*(23/49)+V81	V101	(V81-V174)*(73/93)+V174
V16	VINP(N)3	V59	(V32-V81)*(22/49)+V81	V102	(V81-V174)*(72/93)+V174
V17	(V16-V32)*(15/16)+V32	V60	(V32-V81)*(21/49)+V81	V103	(V81-V174)*(71/93)+V174
V18	(V16-V32)*(14/16)+V32	V61	(V32-V81)*(20/49)+V81	V104	(V81-V174)*(70/93)+V174
V19	(V16-V32)*(13/16)+V32	V62	(V32-V81)*(19/49)+V81	V105	(V81-V174)*(69/93)+V174
V20	(V16-V32)*(12/16)+V32	V63	(V32-V81)*(18/49)+V81	V106	(V81-V174)*(68/93)+V174
V21	(V16-V32)*(11/16)+V32	V64	(V32-V81)*(17/49)+V81	V107	(V81-V174)*(67/93)+V174
V22	(V16-V32)*(10/16)+V32	V65	(V32-V81)*(16/49)+V81	V108	(V81-V174)*(66/93)+V174
V23	(V16-V32)*(9/16)+V32	V66	(V32-V81)*(15/49)+V81	V109	(V81-V174)*(65/93)+V174
V24	(V16-V32)*(8/16)+V32	V67	(V32-V81)*(14/49)+V81	V110	(V81-V174)*(64/93)+V174
V25	(V16-V32)*(7/16)+V32	V68	(V32-V81)*(13/49)+V81	V111	(V81-V174)*(63/93)+V174
V26	(V16-V32)*(6/16)+V32	V69	(V32-V81)*(12/49)+V81	V112	(V81-V174)*(62/93)+V174
V27	(V16-V32)*(5/16)+V32	V70	(V32-V81)*(11/49)+V81	V113	(V81-V174)*(61/93)+V174
V28	(V16-V32)*(4/16)+V32	V71	(V32-V81)*(10/49)+V81	V114	(V81-V174)*(60/93)+V174
V29	(V16-V32)*(3/16)+V32	V72	(V32-V81)*(9/49)+V81	V115	(V81-V174)*(59/93)+V174
V30	(V16-V32)*(2/16)+V32	V73	(V32-V81)*(8/49)+V81	V116	(V81-V174)*(58/93)+V174
V31	(V16-V32)*(1/16)+V32	V74	(V32-V81)*(7/49)+V81	V117	(V81-V174)*(57/93)+V174
V32	VINP(N)4	V75	(V32-V81)*(6/49)+V81	V118	(V81-V174)*(56/93)+V174
V33	(V32-V81)*(48/49)+V81	V76	(V32-V81)*(5/49)+V81	V119	(V81-V174)*(55/93)+V174
V34	(V32-V81)*(47/49)+V81	V77	(V32-V81)*(4/49)+V81	V120	(V81-V174)*(54/93)+V174
V35	(V32-V81)*(46/49)+V81	V78	(V32-V81)*(3/49)+V81	V121	(V81-V174)*(53/93)+V174
V36	(V32-V81)*(45/49)+V81	V79	(V32-V81)*(2/49)+V81	V122	(V81-V174)*(52/93)+V174
V37	(V32-V81)*(44/49)+V81	V80	(V32-V81)*(1/49)+V81	V123	(V81-V174)*(51/93)+V174
V38	(V32-V81)*(43/49)+V81	V81	VINP(N)5	V124	(V81-V174)*(50/93)+V174
V39	(V32-V81)*(42/49)+V81	V82	(V81-V174)*(92/93)+V174	V125	(V81-V174)*(49/93)+V174
V40	(V32-V81)*(41/49)+V81	V83	(V81-V174)*(91/93)+V174	V126	(V81-V174)*(48/93)+V174
V41	(V32-V81)*(40/49)+V81	V84	(V81-V174)*(90/93)+V174	V127	(V81-V174)*(47/93)+V174
V42	(V32-V81)*(39/49)+V81	V85	(V81-V174)*(89/93)+V174	V128	(V81-V174)*(46/93)+V174

Grayscale voltage	Formula	Grayscale voltage	Formula	Grayscale voltage	Formula
V129	(V81-V174)*(45/93)+V174	V172	(V81-V174)*(2/93)+V174	V215	(V174-V223)*(8/49)+V223
V130	(V81-V174)*(44/93)+V174	V173	(V81-V174)*(1/93)+V174	V216	(V174-V223)*(7/49)+V223
V131	(V81-V174)*(43/93)+V174	V174	VINP(N)6	V217	(V174-V223)*(6/49)+V223
V132	(V81-V174)*(42/93)+V174	V175	(V174-V223)*(48/49)+V223	V218	(V174-V223)*(5/49)+V223
V133	(V81-V174)*(41/93)+V174	V176	(V174-V223)*(47/49)+V223	V219	(V174-V223)*(4/49)+V223
V134	(V81-V174)*(40/93)+V174	V177	(V174-V223)*(46/49)+V223	V220	(V174-V223)*(3/49)+V223
V135	(V81-V174)*(39/93)+V174	V178	(V174-V223)*(45/49)+V223	V221	(V174-V223)*(2/49)+V223
V136	(V81-V174)*(38/93)+V174	V179	(V174-V223)*(44/49)+V223	V222	(V174-V223)*(1/49)+V223
V137	(V81-V174)*(37/93)+V174	V180	(V174-V223)*(43/49)+V223	V223	VINP(N)7
V138	(V81-V174)*(36/93)+V174	V181	(V174-V223)*(42/49)+V223	V224	(V223-V239)*(15/16)+V239
V139	(V81-V174)*(35/93)+V174	V182	(V174-V223)*(41/49)+V223	V225	(V223-V239)*(14/16)+V239
V140	(V81-V174)*(34/93)+V174	V183	(V174-V223)*(40/49)+V223	V226	(V223-V239)*(13/16)+V239
V141	(V81-V174)*(33/93)+V174	V184	(V174-V223)*(39/49)+V223	V227	(V223-V239)*(12/16)+V239
V142	(V81-V174)*(32/93)+V174	V185	(V174-V223)*(38/49)+V223	V228	(V223-V239)*(11/16)+V239
V143	(V81-V174)*(31/93)+V174	V186	(V174-V223)*(37/49)+V223	V229	(V223-V239)*(10/16)+V239
V144	(V81-V174)*(30/93)+V174	V187	(V174-V223)*(36/49)+V223	V230	(V223-V239)*(9/16)+V239
V145	(V81-V174)*(29/93)+V174	V188	(V174-V223)*(35/49)+V223	V231	(V223-V239)*(8/16)+V239
V146	(V81-V174)*(28/93)+V174	V189	(V174-V223)*(34/49)+V223	V232	(V223-V239)*(7/16)+V239
V147	(V81-V174)*(27/93)+V174	V190	(V174-V223)*(33/49)+V223	V233	(V223-V239)*(6/16)+V239
V148	(V81-V174)*(26/93)+V174	V191	(V174-V223)*(32/49)+V223	V234	(V223-V239)*(5/16)+V239
V149	(V81-V174)*(25/93)+V174	V192	(V174-V223)*(31/49)+V223	V235	(V223-V239)*(4/16)+V239
V150	(V81-V174)*(24/93)+V174	V193	(V174-V223)*(30/49)+V223	V236	(V223-V239)*(3/16)+V239
V151	(V81-V174)*(23/93)+V174	V194	(V174-V223)*(29/49)+V223	V237	(V223-V239)*(2/16)+V239
V152	(V81-V174)*(22/93)+V174	V195	(V174-V223)*(28/49)+V223	V238	(V223-V239)*(1/16)+V239
V153	(V81-V174)*(21/93)+V174	V196	(V174-V223)*(27/49)+V223	V239	VINP(N)8
V154	(V81-V174)*(20/93)+V174	V197	(V174-V223)*(26/49)+V223	V240	(V239-V247)*(7/8)+V247
V155	(V81-V174)*(19/93)+V174	V198	(V174-V223)*(25/49)+V223	V241	(V239-V247)*(6/8)+V247
V156	(V81-V174)*(18/93)+V174	V199	(V174-V223)*(24/49)+V223	V242	(V239-V247)*(5/8)+V247
V157	(V81-V174)*(17/93)+V174	V200	(V174-V223)*(23/49)+V223	V243	(V239-V247)*(4/8)+V247
V158	(V81-V174)*(16/93)+V174	V201	(V174-V223)*(22/49)+V223	V244	(V239-V247)*(3/8)+V247
V159	(V81-V174)*(15/93)+V174	V202	(V174-V223)*(21/49)+V223	V245	(V239-V247)*(2/8)+V247
V160	(V81-V174)*(14/93)+V174	V203	(V174-V223)*(20/49)+V223	V246	(V239-V247)*(1/8)+V247
V161	(V81-V174)*(13/93)+V174	V204	(V174-V223)*(19/49)+V223	V247	VINP(N)9
V162	(V81-V174)*(12/93)+V174	V205	(V174-V223)*(18/49)+V223	V248	(V47-V251)*(3/4)+V251
V163	(V81-V174)*(11/93)+V174	V206	(V174-V223)*(17/49)+V223	V249	(V247-V251)*(2/4)+V251
V164	(V81-V174)*(10/93)+V174	V207	(V174-V223)*(16/49)+V223	V250	(V247-V251)*(1/4)+V251
V165	(V81-V174)*(9/93)+V174	V208	(V174-V223)*(15/49)+V223	V251	VINP(N)10
V166	(V81-V174)*(8/93)+V174	V209	(V174-V223)*(14/49)+V223	V252	(V251-V255)*(3/4)+V255
V167	(V81-V174)*(7/93)+V174	V210	(V174-V223)*(13/49)+V223	V253	(V251-V255)*(2/4)+V255
V168	(V81-V174)*(6/93)+V174	V211	(V174-V223)*(12/49)+V223	V254	(V251-V255)*(1/4)+V255
V169	(V81-V174)*(5/93)+V174	V212	(V174-V223)*(11/49)+V223	V255	VINP(N)11
V170	(V81-V174)*(4/93)+V174	V213	(V174-V223)*(10/49)+V223		
V171	(V81-V174)*(3/93)+V174	V214	(V174-V223)*(9/49)+V223		

12 MAXIMUM RATINGS

Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{CORE}	Supply voltage for logic	-0.3 to +2.0	V
V_{DDIO}	Supply Voltage for I/O	-0.3 to +4.0	V
V_{CI}	Input Voltage	VSS - 0.3 to 5.0	V
I	Current Drain Per Pin Excluding V_{CORE} and V_{SS}	25	mA
T_A	Operating Temperature	-40 to +85	^oC
T_{stg}	Storage Temperature	-65 to +150	^oC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, strong electric fields, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices. It is advised that proper precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that analog voltages should be constrained to the range $V_{GL} < V_{SS} < V_{DDIO} \leq V_{CI} < V_{GH}$. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DDIO}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

13 DC CHARACTERISTICS

DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, T_A = -40 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DDIO}	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.6	-	3.3	V
V_{CI}	Booster Reference Supply Voltage Range (3)	Recommend Operating Voltage Possible Operating Voltage	2.5	-	3.3	V
$I_{sleep}1$	Sleep mode current (VCI pin)	VDDEXT=VDDIO=3.3V, VCI=3.3V	-	40	100	uA
$I_{sleep}2$	Sleep mode current (VDDIO)		-	45	100	uA
$I_{dp\ x\ 2}$	Operating mode current (VCI x 2 mode)	100pF loading at Source output VDDIO=3.3V, VCI=3.3V	-	15	30	mA
$I_{dp\ x\ 3}$	Operating mode current (VCI x 3 mode)	100pF loading at Source output VDDIO=3.3V, VCI=3.3V	-	25	40	mA
AVDD	AVDD x 2 primary booster efficiency[1]	No panel loading, VCI and VCHS = 10 Ohm	85	91	-	%
			-	-	VCI x 2	V
VGH	Gate driver High Output Voltage Booster efficiency[2]	No panel loading; 4x booster; ITO for C1P, C1N, C2P, C2N,AVDD, VCI and VCHS = 10 Ohm	45.8	77.7	-	%
		No panel loading; 5x booster; ITO for C1P, C1N, C2P, C2N,AVDD, VCI and VCHS = 10 Ohm	54.6	86.5	-	%
		No panel loading; 6x booster; ITO for C1P, C1N, C2P, C2N,AVDD, VCI and VCHS = 10 Ohm	53.9	85.8	-	%
VGL	Gate driver Low Output Voltage Booster efficiency	No panel loading; 3x booster; ITO for C3P, C3N , VGH, VCI and VCHS = 10 Ohm	-	73.6	-	%
			-	-	AVDDM	V
		No panel loading; 4x booster; ITO for C3P, C3N , VGH, VCI and VCHS = 10 Ohm	-	75	-	%
			-	-	AVDDM	V
		No panel loading; 5x booster; ITO for C3P, C3N , VGH, VCI and VCHS = 10 Ohm	52.2	82.4	-	%
		No panel loading; 6x booster; ITO for C3P, C3N , VGH, VCI and VCHS = 10 Ohm	52.9	83.1	-	%
VCOMDC	VCOMDC Output Voltage		VCIM	-	VSS-0.2	V
AVDD	AVDD Source Output Voltage[3]		3.5	-	6.5	V
AVDDM	AVDDM Source Output Voltage		-6.5	-	-3.5	V
VOH1	Logic High Output Voltage	Iout=-100uA	0.9 * V_{DDIO}	-	V_{DDIO}	V
VOL1	Logic Low Output Voltage	Iout=100uA	0	-	0.1 * V_{DDIO}	V
VIH1	Logic High Input voltage		0.7 * V_{DDIO}	-	V_{DDIO}	V
VIL1	Logic Low Input voltage		0	-	0.3 * V_{DDIO}	V
I_{OH}	Logic High Output Current Source	Vout = V_{DDIO}-0.4V	50	-	-	µA
I_{OL}	Logic Low Output Current Drain	Vout = 0.4V	-	-	-50	µA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	µA
I_{II}/I_{IH}	Logic Input Current		-1	-	1	µA
C_{IN}	Logic Pins Input Capacitance		-	5	7.5	pF
R_{SON}	Source drivers output resistance		-	1	-	kΩ
R_{GON}	Gate control signals output resistance		-	500	-	Ω
R_{CON}	VCOM output resistance		-	200	-	Ω
TC	Temperature Coefficient		-	0.012	-	%

Note1: **AV_{DD} efficiency = AV_{DD} /(2 x V_{CI}) x 100%**
Note2: **V_{GH} efficiency = V_{GH}/(V_{CI} x n) x 100%** **(where n = booster factor)**
Note3: **AVDD – VLCDH ≥ 0.1V**
Note4: **|AVDD| ≥ |AVDDM| + 0.2V**

14 Functional Block Description

14.1 Serial Interface

Serial Interface – 4-wire (8 bits)

The clock synchronized serial peripheral interface (SPI) using the chip select line (CSB), serial transfer clock line (SCK), serial input data (SDI). The serial data transfer starts at the falling edge of CSB input and ends at the rising edge of CSB.SDC determinate the data of SDI which is register or data.

Figure 14-1: 4-wire Serial Interface timing diagram

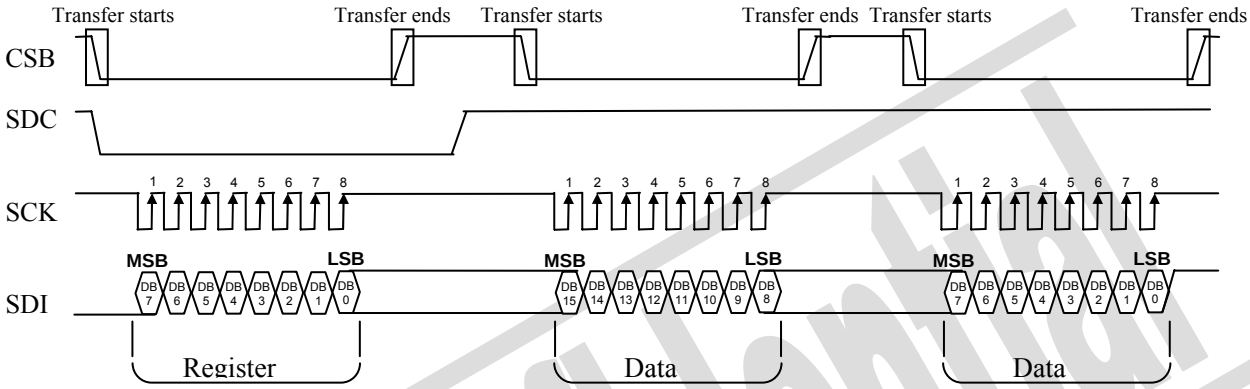
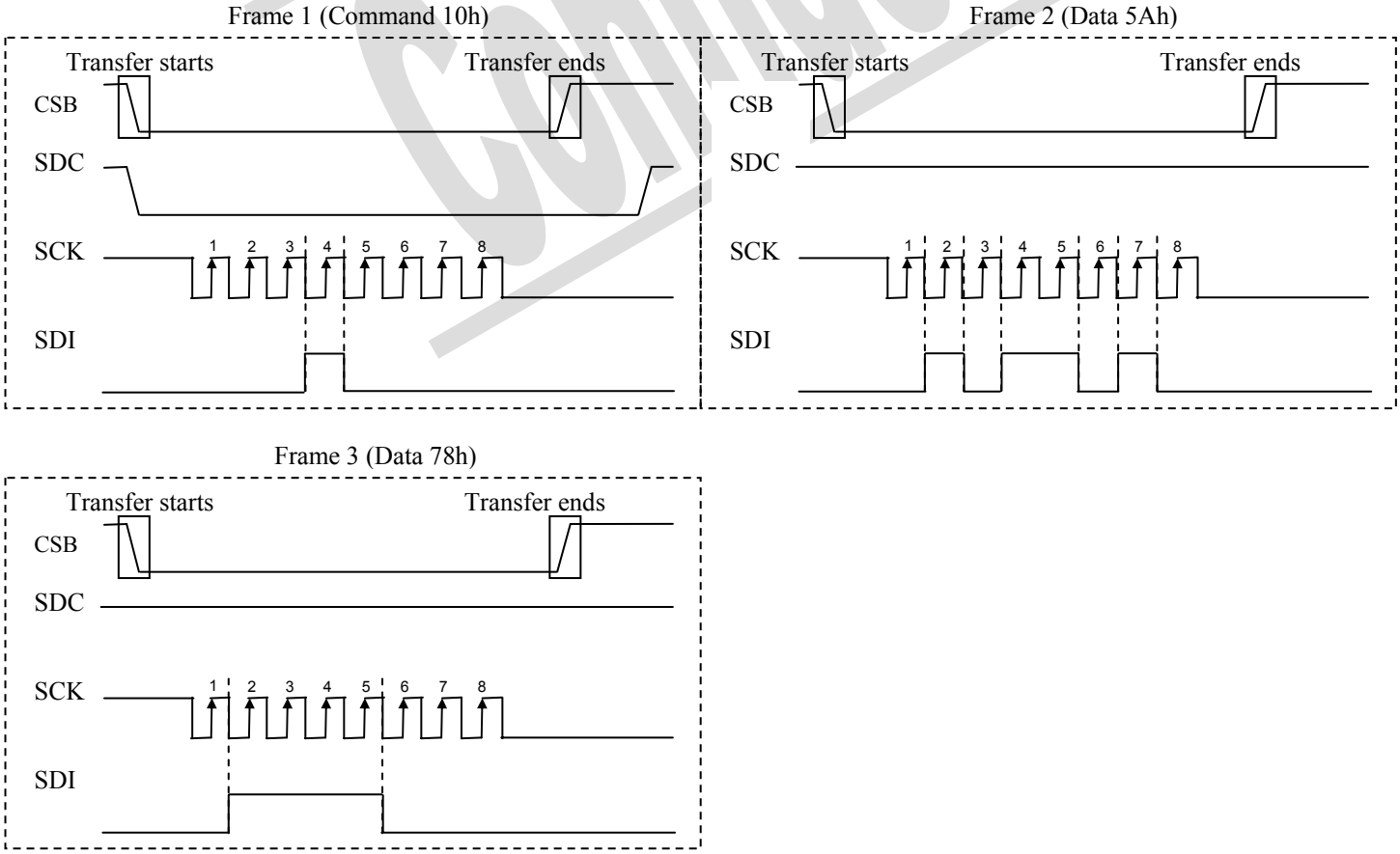


Figure 14-2: Example of 4-wire (8 bits)



Serial Interface – 3-wire (9 bits)

The clock synchronized serial peripheral interface (SPI) using the chip select line (CSB), serial transfer clock line (SCK), serial input data (SDI). The serial data transfer starts at the falling edge of CSB input and ends at the rising edge of CSB. DC bit determinate the data of SDI which is register or data.

Figure 14-3: 3-wire Serial Interface timing diagram

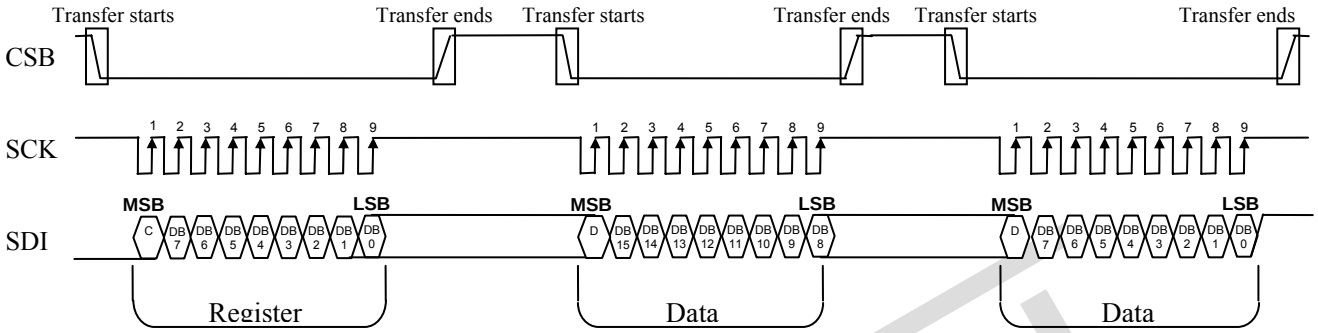
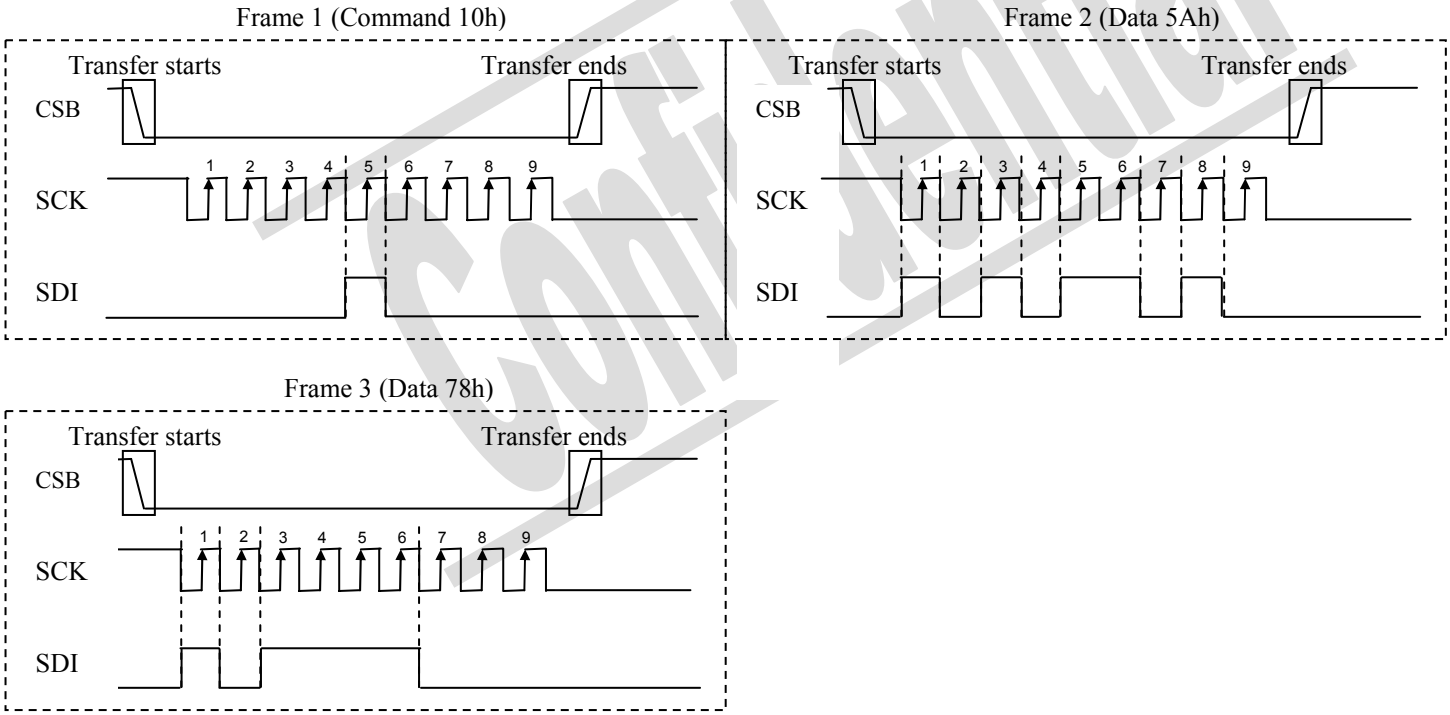


Figure 14-4: Example of 3-wire (9 bits)

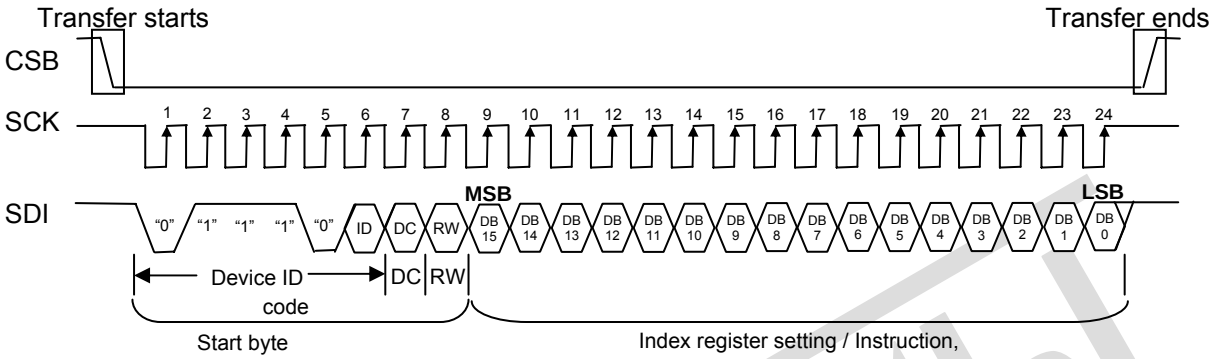


Serial Interface – 3-wire (24 bits)

The clock synchronized serial peripheral interface (SPI) using the chip select line (CSB), serial transfer clock line (SCK), serial input data (SDI), and serial output data (SDO). The serial data transfer starts at the falling edge of CSB input and ends at the rising edge of CSB. DC bit determinate the data of SDI which is register or data. RW bit determinate the read / write operation.

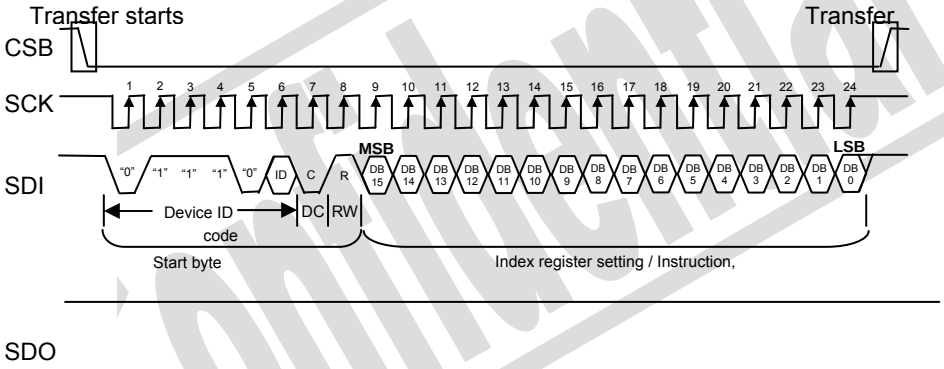
Figure 14-5: 3-wire (24-bit) Serial Interface timing diagram

Write

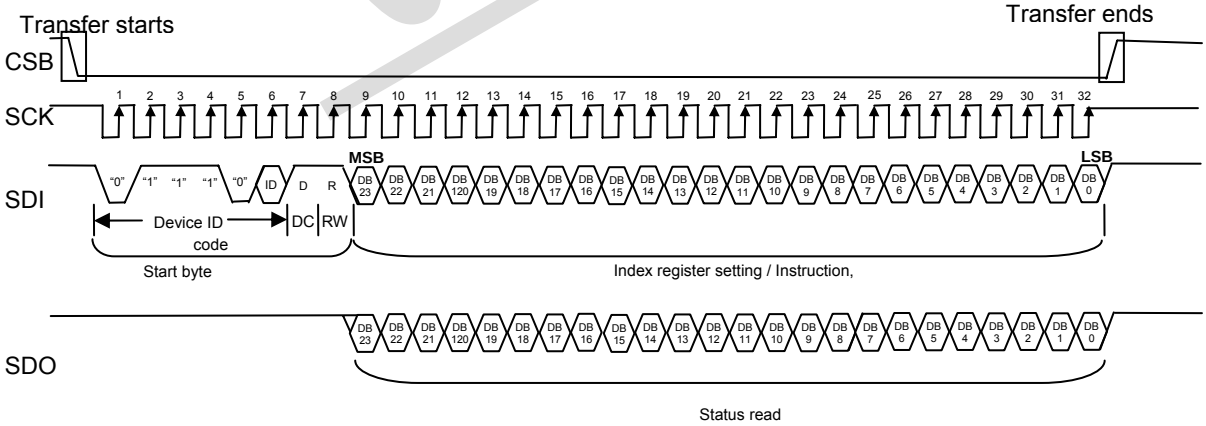


Read

1st step read
- Index register



2nd step read
- Data at SDO



14.2 Data Control

The display data and frame position information from the controller is synchronized with the Gate Drive circuit and shift registered for the Source Driver circuit.

14.3 Booster and Regulator Circuit

These two functional blocks generate the voltage of V_{GH}, $V_{GL,}$ $V_{COMDC,}$ V_{LCDH} and V_{LCDL} which are necessary for operating a TFT LCD.

14.4 Shift Register

The shift registers control the direction of line scanning of source and gate.

14.5 Data Latches

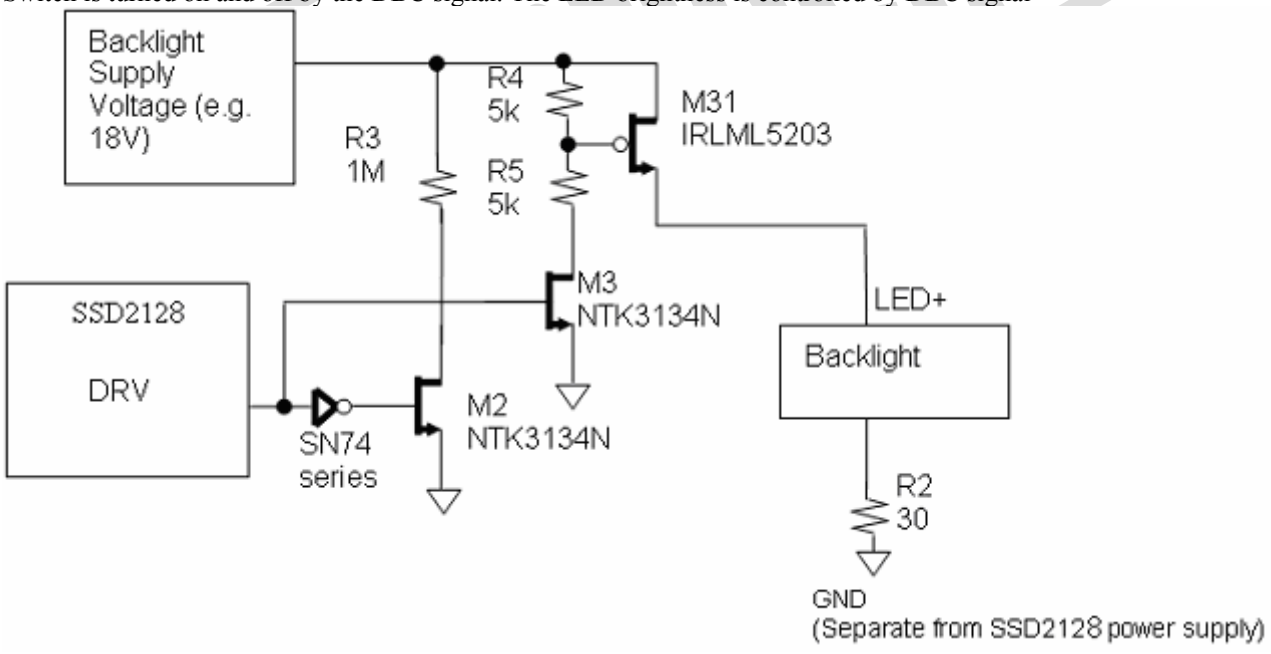
This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the Source Driver to output the required voltage level.

14.6 Reset Circuit

This block is integrated into the Interface Logic which includes Power On Reset circuitry and the hardware reset pin, $\overline{RES}$. Both of these having the same reset function. Once the $\overline{RES}$ pin receives a negative reset pulse, all internal circuitry will start to initialize. The minimum pulse width for completing the reset sequence is 10us. The status of the chip after reset is given in Command Table:

14.7 Dynamic Backlight Control (DBC)

Switch is turned on and off by the DBC signal. The LED brightness is controlled by DBC signal



15 AC CHARACTERISTICS

15.1 Display signal output timing

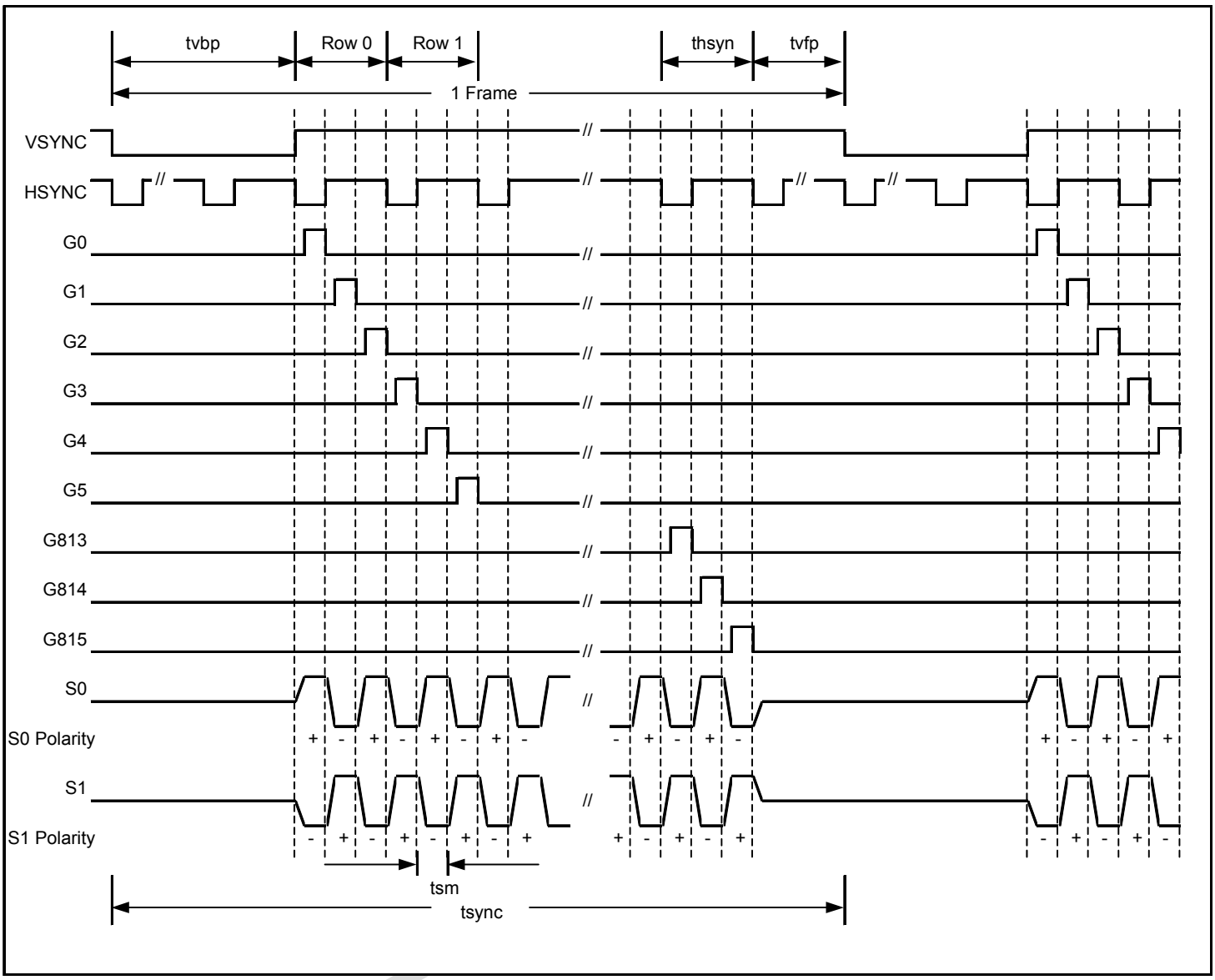
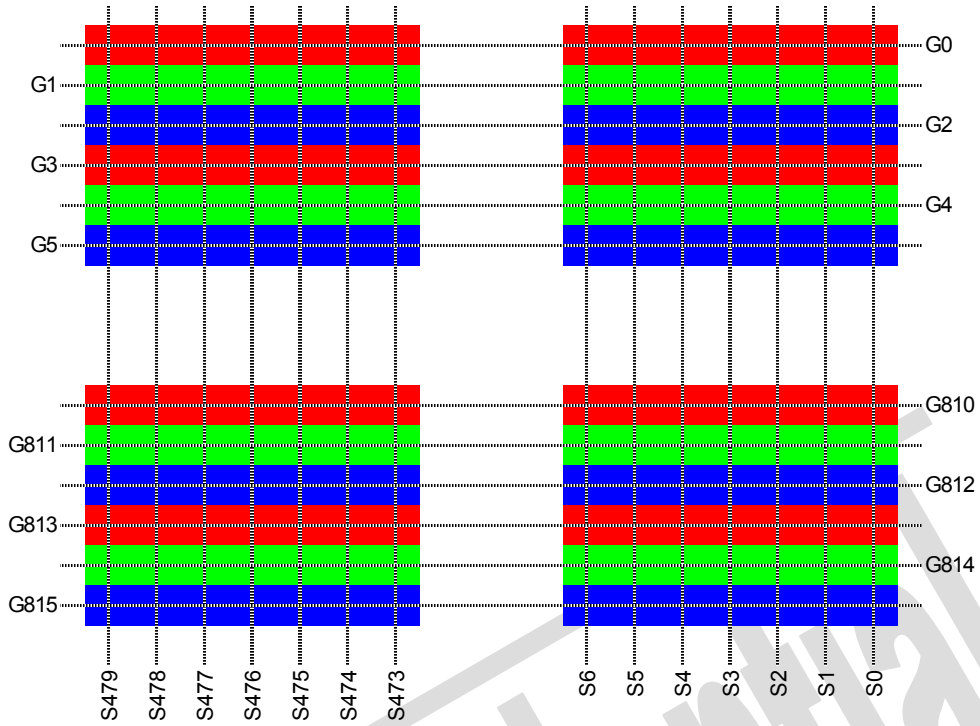


Figure 15-1: Gate and source output timing (Dot inversion, gate non-overlapping)

Symbol	Parameter	Min	Typ	Max	Unit
t_{VSYNC}	1 / Frame Frequency	-	16.7	-	ms
t_{HSYNC}	1 / Line Frequency	-	61.3	-	us
t_{Sm}	1 / Source Frequency	-	20.4	-	us
t_{vbp}	Delay time between each field	-	4	-	us
t_{vfp}	Delay time between each field	-	2	-	us

Figure 15-2- Example of color filter arrangement (X400=0, TB =1, RL = 0)



15.2 SPI Timing

AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 3.3V, T_A = -40 to 85°C)

Serial Peripheral Interface (SPI)

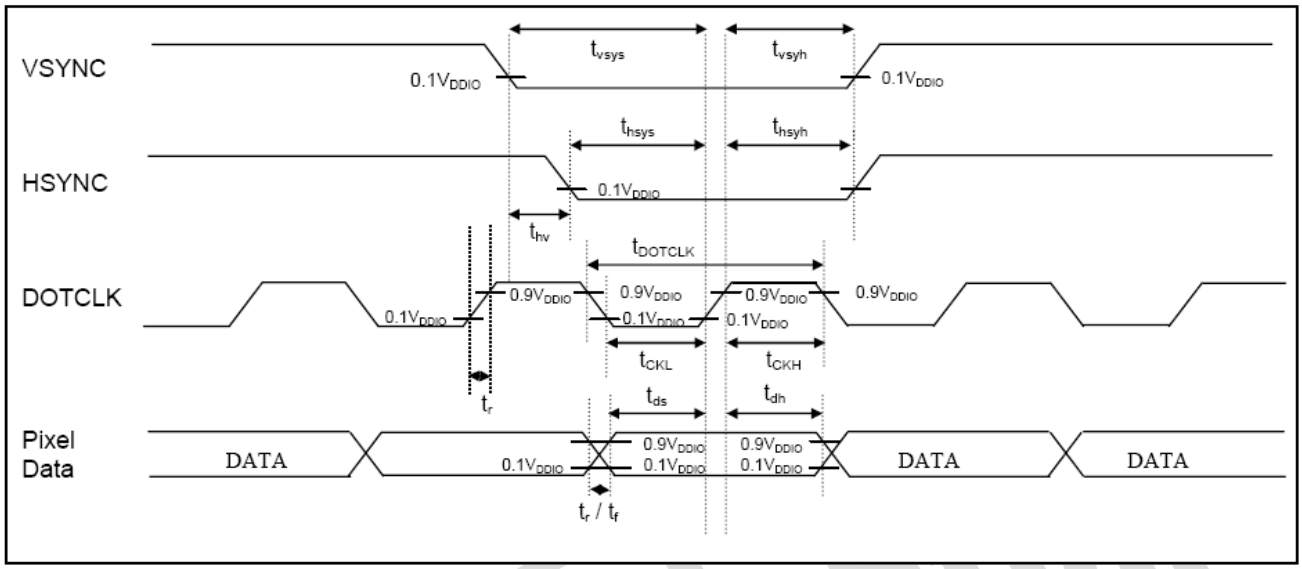


Figure 15-3- Pixel Clock Timing

Characteristics		Symbol	Min	Typ	Max	Units
DOTCLK Frequency	24 bits parallel	f_{DOTCLK}	-	-	14	MHz
	8 bits serial		-	-	-	
DOTCLK Period	24 bits parallel	t_{DOTCLK}	71.4	-	-	nSec
	8 bits serial		-	-	-	
Pixel Clock Period	24 bits parallel	t_{PIXCLK}	-	1	-	t_{DOTCLK}
	8 bits serial		-	3	-	
Pixel Clock Freq.	24 bits parallel	f_{PIXCLK}	-	-	14	MHz
	8 bits serial					
Vertical Sync Setup Time		t_{vsys}	5	-	-	nSec
Vertical Sync Hold Time		t_{vsyh}	5	-	-	nSec
Horizontal Sync Setup Time		t_{hsys}	5	-	-	nSec
Horizontal Sync Hold Time		t_{hsyh}	5	-	-	nSec
Phase difference of Sync Signal Falling Edge		t_{hv}	0	-	480	t_{DOTCLK}
DOTCLK Low Period		t_{CKL}	18	-	-	nSec
DOTCLK High Period		t_{CKH}	18	-	-	nSec
Data Setup Time		t_{ds}	10	-	-	nSec
Data hold Time		t_{dh}	15	-	-	nSec
Reset pulse width		t_{RES}	10	-	-	uSec
Rise / Fall time		t_r / t_f	-	-	25	nSec

Note1: External clock source must be provided to DOTCLK pin of SSD2128Z. The driver will not operate if absent of the clocking signal.
Note2: Tr/Tf apply to all logic input, RGB and SPI signals

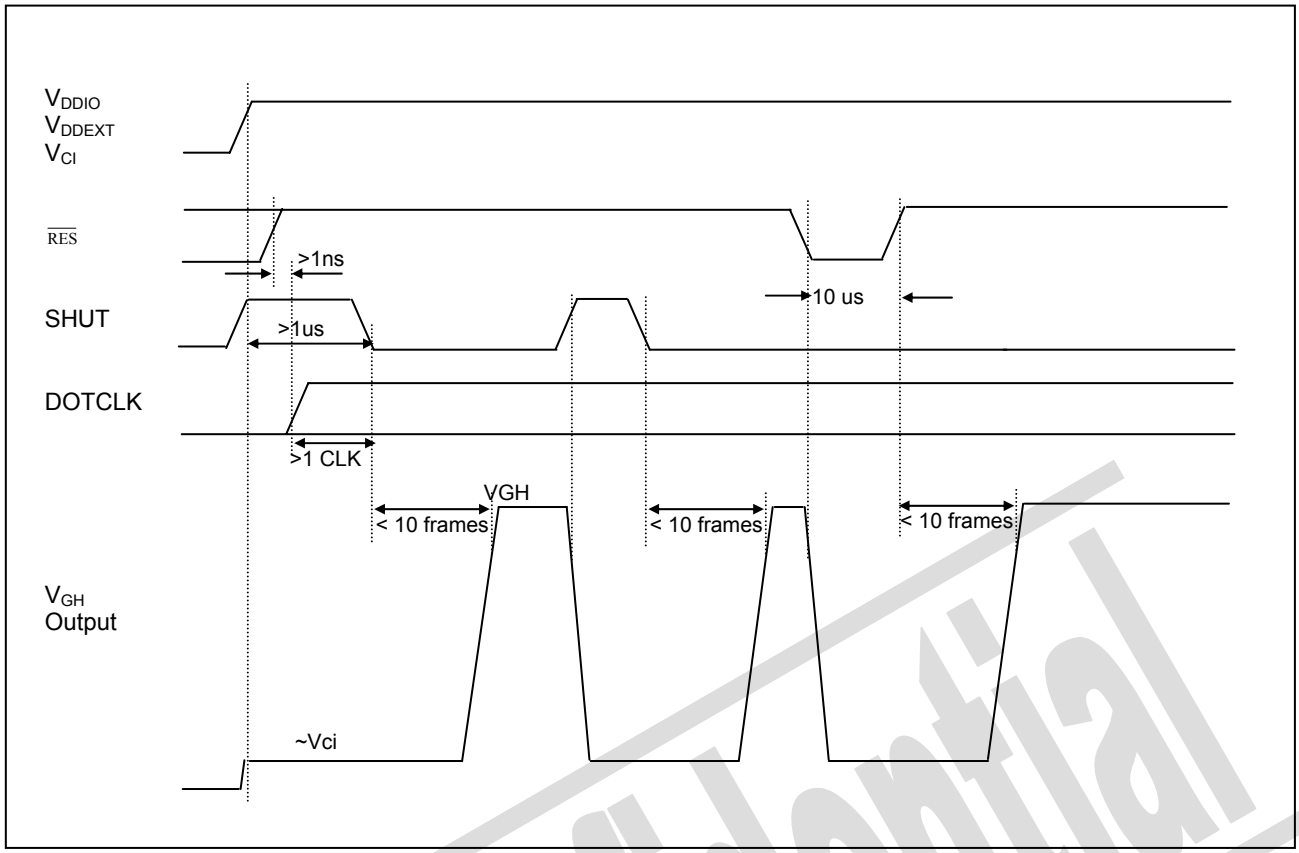


Figure 15-4 VGH Output against SHUT & RESB

Note1: The minimum cycle time of SHUT is 10 + 2 frames.

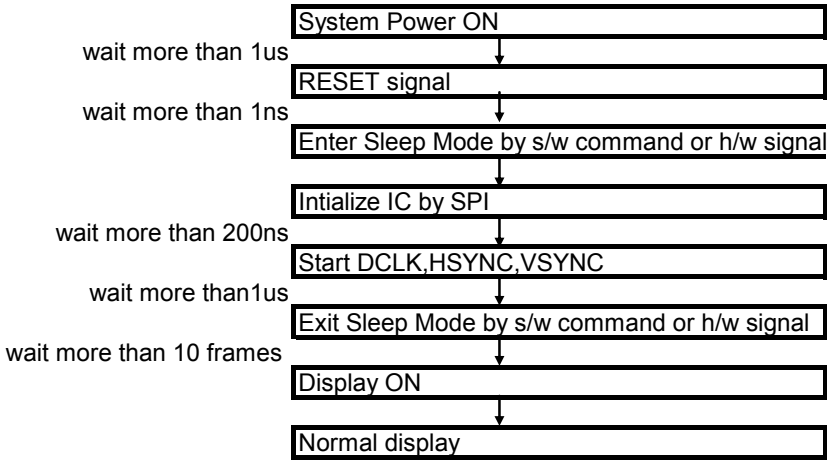
Note2: DOTCLK must be provided for boosting of V_{GH}. The above timing diagram assumed voltages and DOTCLK are continuous supplied after power on.

Note3: V_{GH} will be forced to V_{CI} at the low stage of $\overline{RES}$.

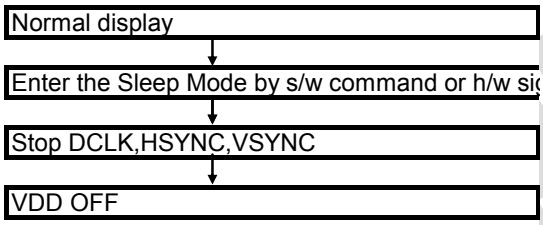
Note4: The minimum pulse width of RESET is 10us.

15.3 Power On/Off Sequence & Vout Timing

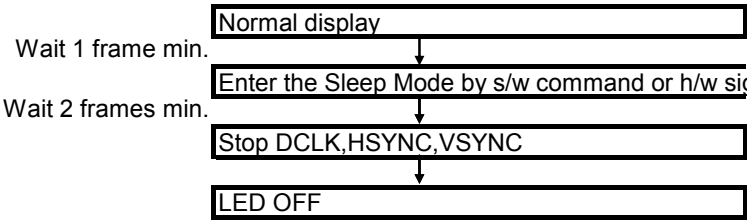
Power Up Sequence



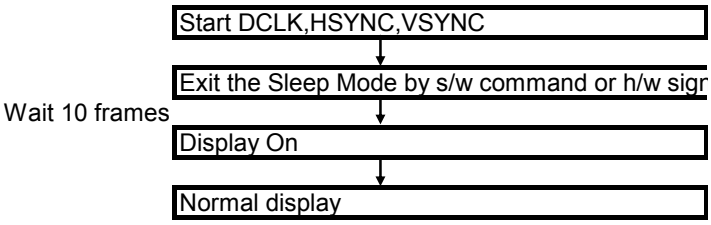
Power Down Sequence



Enter Sleep Mode Sequence



Exit Sleep Mode Sequence



Note: To prevent potential damage to the device, all capacitors must be discharged to below 0.5V before the driver is removed from, or before the driver is attached to those components.

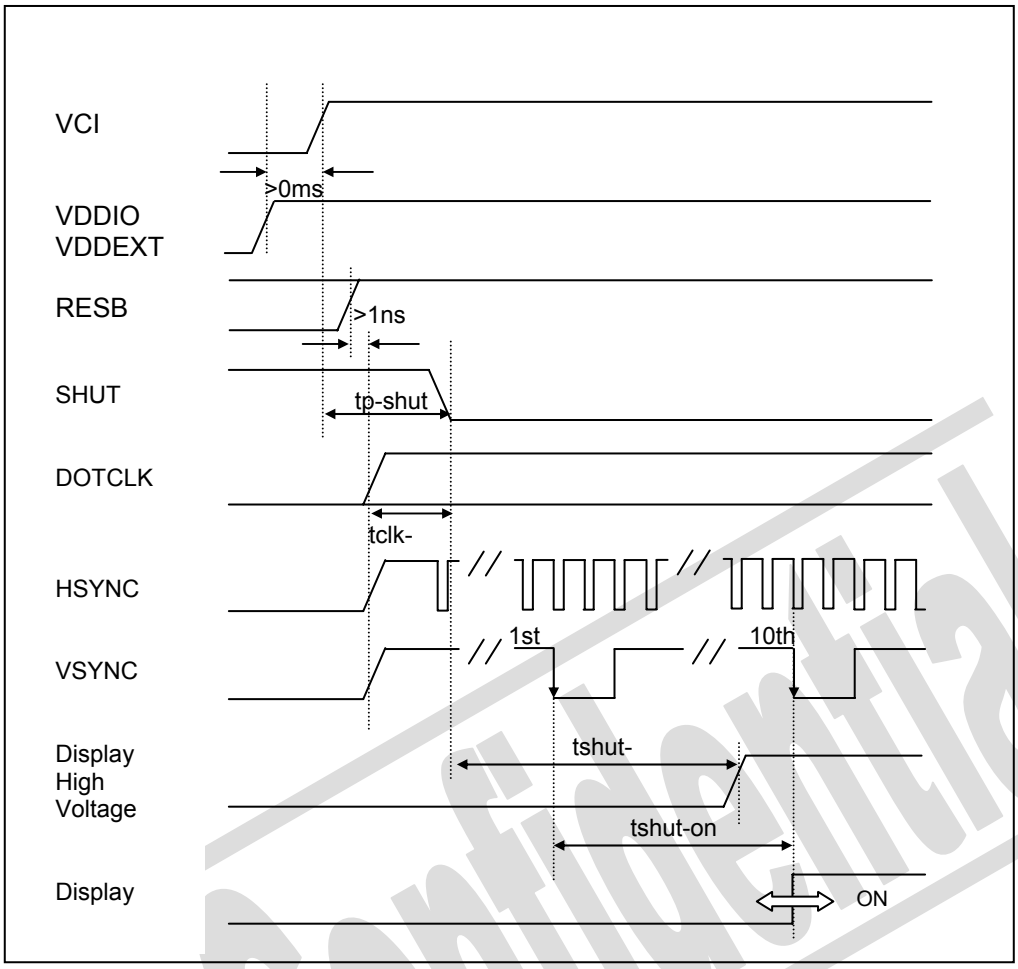


Figure 15-5 - Power Up Sequence

Characteristics	Symbol	Min	Typ	Max	Units
V_{DDEXT} / V_{DDIO} on to falling edge of SHUT	tp-shut	1	-	-	µsec
DOTCLK	tclk-shut	1	-	-	clk
Falling edge of SHUT to LCD power on	tshut-lcd	-	-	167	msec
Falling edge of SHUT to display start	tshut-on	-	-	10	frame
-- 1 line: 512 clk -- 1 frame: 278 line -- DOTCLK = 8.5MHz		-	167	-	msec

Note1: It is necessary to input DOTCLK before the falling edge of SHUT.

Note2: Display starts at 10th falling edge of VSTNC after the falling edge of SHUT.

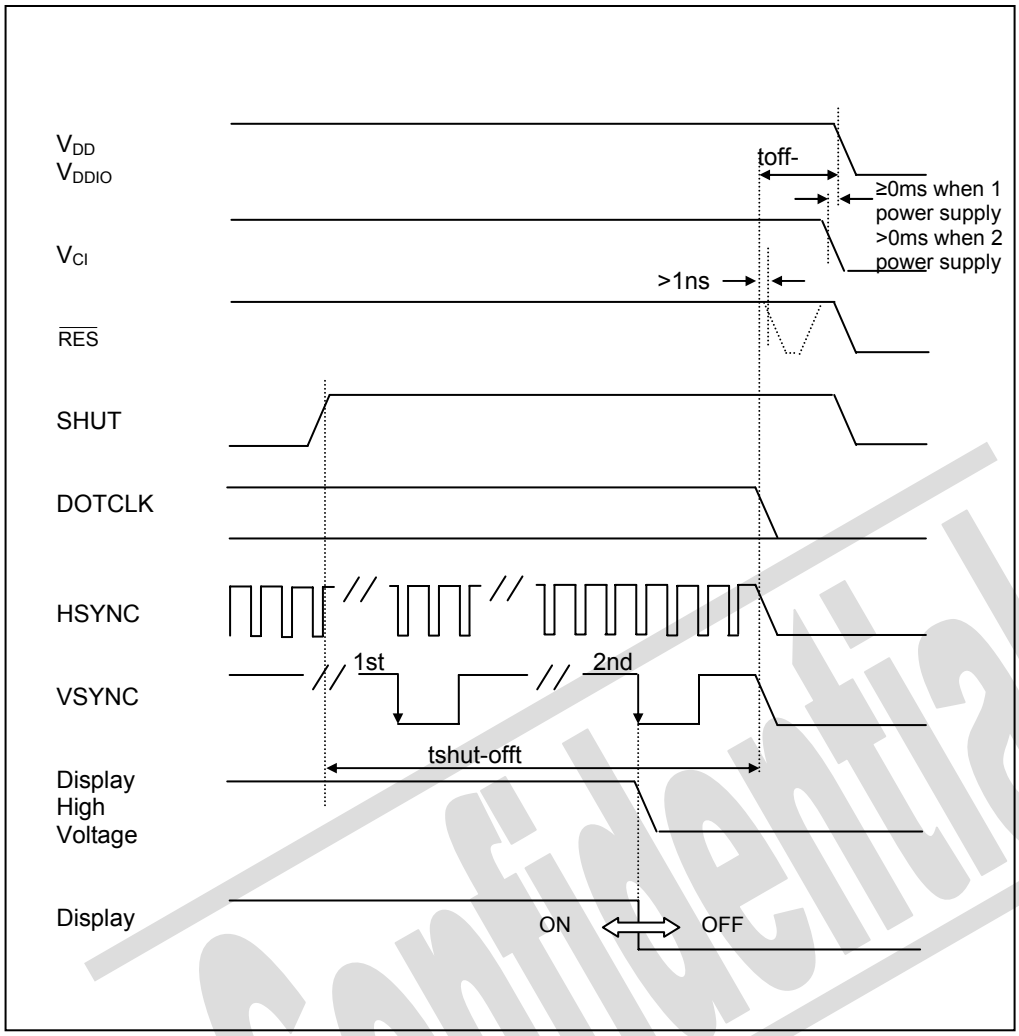


Figure 15-6 - Power Down Sequence

Characteristics	Symbol	Min	Typ	Max	Units
Rising edge of SHUT to display off -- 1 line: 512 clk -- 1 frame: 278 line -- DOTCLK = 8.5 MHz	tshut-off	2	-	-	frame
		33.4	-	-	msec
Input-signal-off to V_{DDEXT} / V_{DDIO} off	toff-vdd	1	-	-	µsec

Note1: DOTCLK must be maintained at lease 2 frames after the rising edge of SHUT.

Note2: Display become off at the 2nd falling edge of VSTNC after the falling edge of SHUT.

Note3: If RESET signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

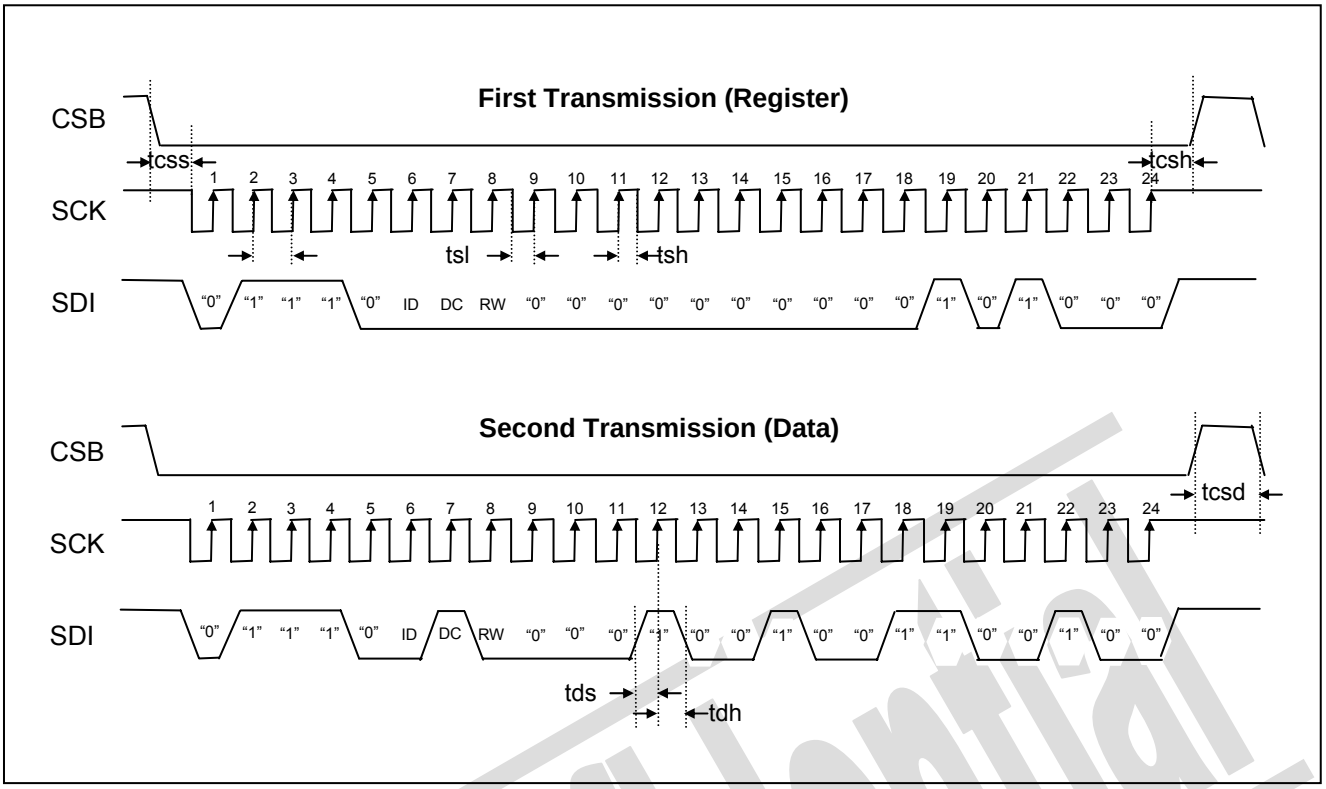


Figure 15-7 - SPI Interface Timing Diagram & Transaction Example

Characteristics	Symbol	Min	Typ	Max	Units
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	nsec
Clock Low Width	tsl	25	-	-	nsec
Clock High Width	tsh	25	-	-	nsec
Chip Select Setup Time	tcss	5	-	-	nsec
Chip Select Hold Time	tcsh	10	-	-	nsec
Chip Select High Delay Time	tcsd	20	-	-	nsec
Data Setup Time	tds	5	-	-	nsec
Data Hold Time	tdh	15	-	-	nsec

Note1: SPID pin connected to VSS.

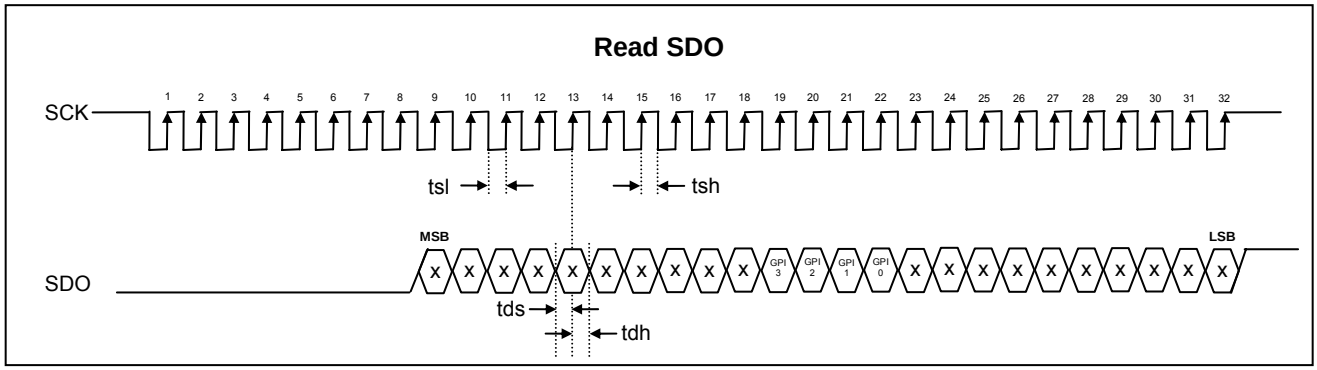


Figure 15-8 - SPI Interface Timing Diagram & Transaction Example (read cycle)

Characteristics	Symbol	Min	Typ	Max	Units
Serial Clock Frequency	fclk	-	1	-	MHz
Serial Clock Cycle Time	tclk	-	1	-	usec
Clock Low Width	tsl	-	500	-	nsec
Clock High Width	tsh	-	500	-	nsec
SDO Setup Time	tds	-	250	-	nsec
SDO Hold Time	tdh	-	250	-	nsec

15.4 8-bit Serial Interface

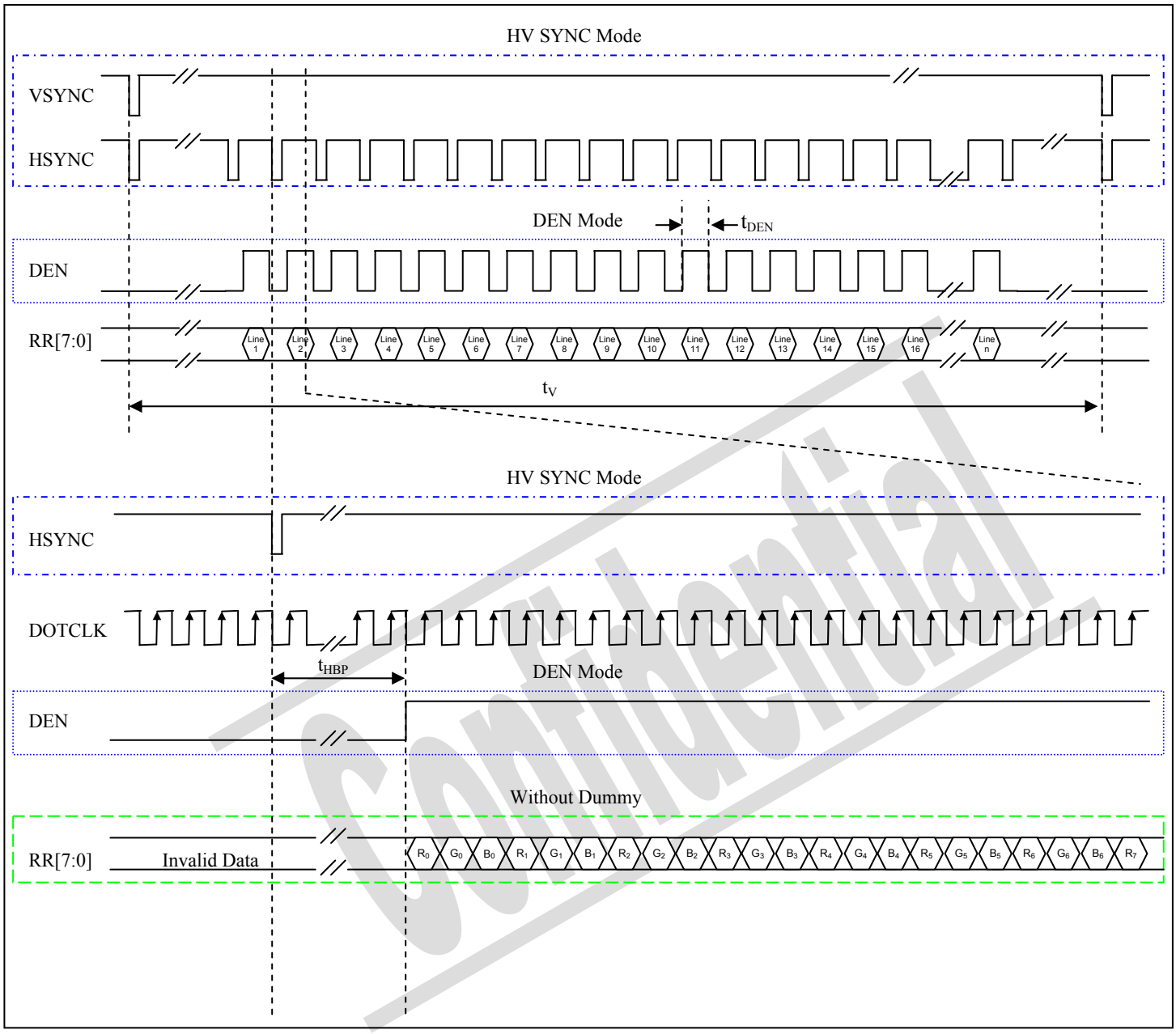


Figure 15-9 – 8-bit Serial Interface Timing Diagram & Transaction Example

Characteristics		Symbol	HV SYNC Mode Without Dummy	Units
Serial Clock Frequency		$1/t_{DOTCLK}$	25.62	MHz
Horizontal	One Line Period	t_H	1536	t_{DOTCLK}
	Active Data Period	t_{data}	1440	t_{DOTCLK}
	Horizontal Back Porch	t_{HBP}	48	t_{DOTCLK}
	Horizontal Front Porch	t_{HFP}	48	t_{DOTCLK}
Vertical	One Field Period	t_V	278	t_H
	Active Line period	t_{AL}	272	t_H
	Vertical Back Porch	t_{VBP}	4	t_H
	Vertical Front Porch	t_{VFP}	2	t_H

Characteristics		Symbol	DEN Mode	Units
Serial Clock Frequency		$1/t_{DOTCLK}$	25.62	MHz
Horizontal	One Line Period	t_H	1536	t_{DOTCLK}
	Active Data Period	t_{data}	1440	t_{DOTCLK}
	Data Enable Period	t_{DEN}	1440	t_{DOTCLK}
Vertical	One Field Period	t_V	278	t_H
	Active Line period	t_{AL}	272	t_H
	Vertical Back Porch	t_{VBP}	4	t_H
	Vertical Front Porch	t_{VFP}	2	t_H

15.5 24-bit RGB Interface

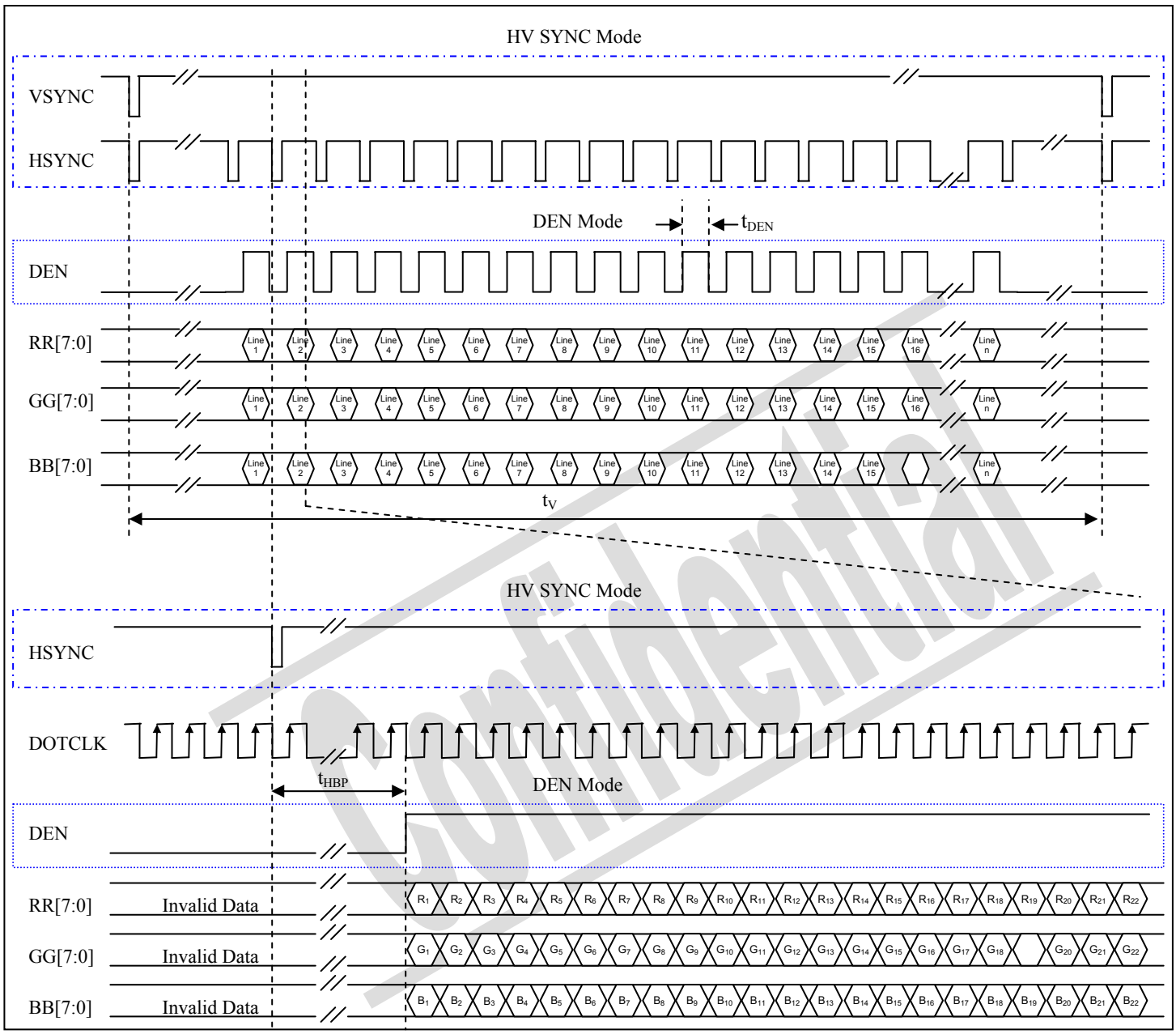


Figure 15-10 – 24-bit Serial Interface Timing Diagram & Transaction Example

Characteristics		Symbol	HV SYNC Mode	Units
Serial Clock Frequency		$1/t_{DOTCLK}$	8.54	MHz
Horizontal	One Line Period	t_H	512	t_{DOTCLK}
	Active Data Period	t_{data}	480	t_{DOTCLK}
	Horizontal Back Porch	t_{HBP}	16	t_{DOTCLK}
	Horizontal Front Porch	t_{HFP}	16	t_{DOTCLK}
Vertical	One Field Period	t_V	278	t_H
	Active Line period	t_{AL}	272	t_H
	Vertical Back Porch	t_{VBP}	4	t_H
	Vertical Front Porch	t_{VFP}	2	t_H

Characteristics		Symbol	DEN Mode	Units
Serial Clock Frequency		$1/t_{DOTCLK}$	8.74	MHz
Horizontal	One Line Period	t_H	512	t_{DOTCLK}
	Active Data Period	t_{data}	480	t_{DOTCLK}
	Data Enable Period	t_{DEN}	480	t_{DOTCLK}
Vertical	One Field Period	t_V	278	t_H
	Active Line period	t_{AL}	272	t_H
	Vertical Back Porch	t_{VBP}	4	t_H
	Vertical Front Porch	t_{VFP}	2	t_H

16 Application Circuit

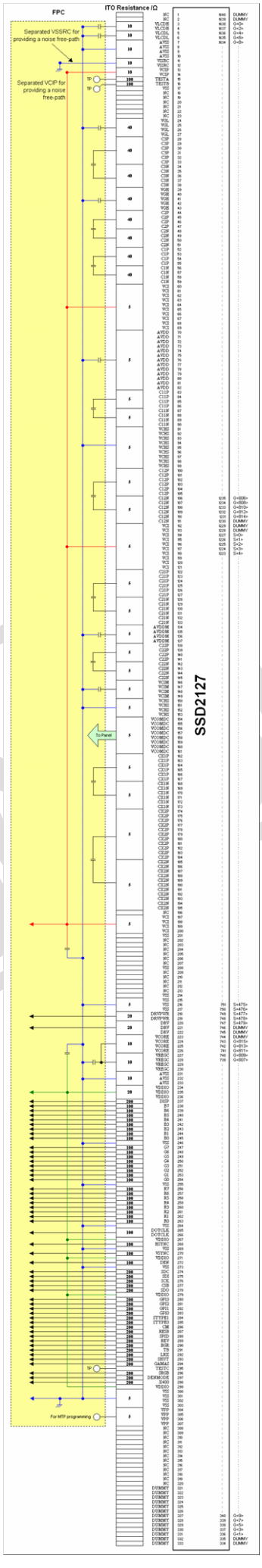


Figure 16-1 – SSD2128 Application Circuit

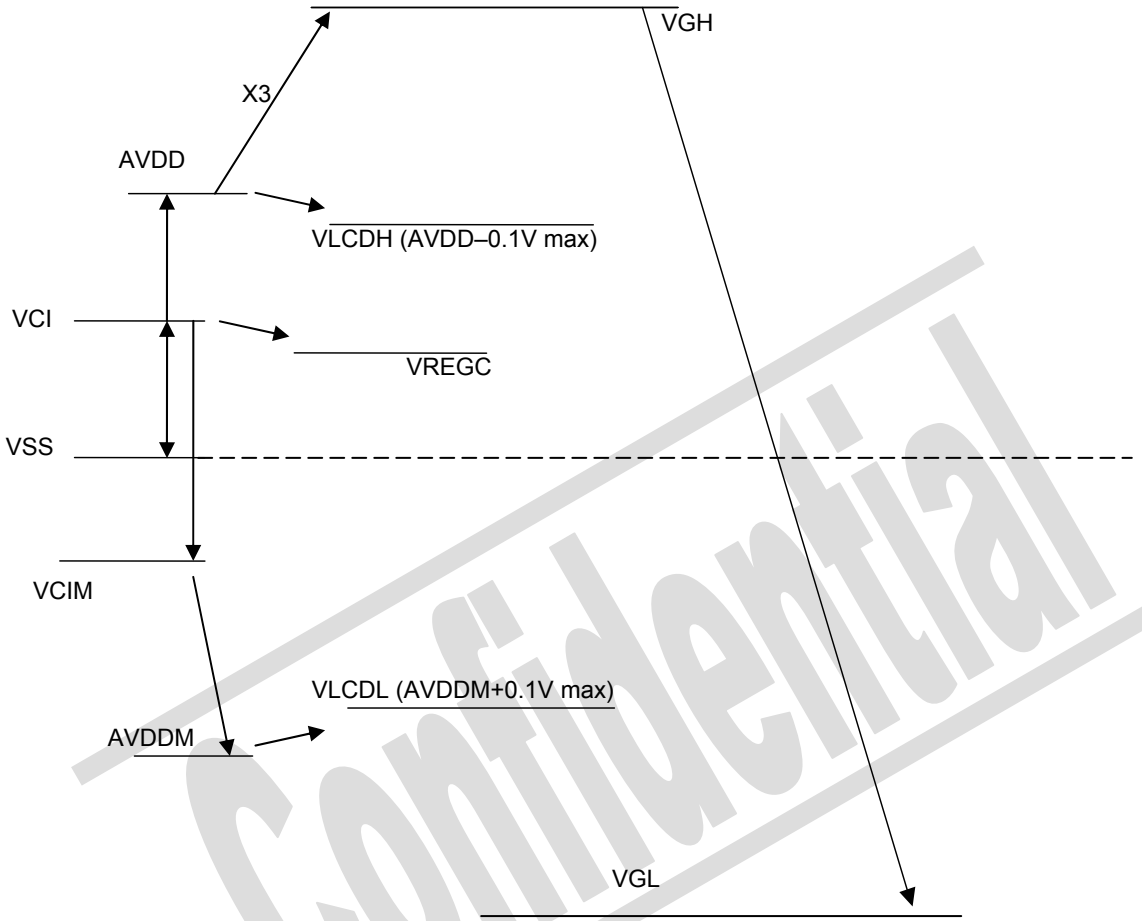
External Capacitors				
	Connection	**Cap Value**	**Voltage**	**Polarity**
C1	VLCDH-VSS	2.2uF	6.3V	+ve
C2	VLCDL-VSS	2.2uF	6.3V	-ve
C3	VGL-VSS	2.2uF	16V	-ve
C4	C3P-C3N	0.22uF	16V	
C5	VGH-VSS	2.2uF	16V	+ve
C6	C2P-C2N	0.22uF	16V	
C7	C1P-C1N	0.22uF	16V	
C8	AVDD-VSS	2.2uF	16V	+ve
C9	C11P-C11N	0.22uF	16V	
C10	C12P-C12N	0.22uF	16V	
C11	C21P-C21N	0.22uF	16V	
C12	AVDDM-VSS	2.2uF	16V	-ve
C13	C22P-C22N	0.22uF	16V	
C14	VCIM-VSS	2.2uF	6.3V	-ve
C15	CX1P-CX1N	0.22uF	6.3V	
C16	CX2P-CX2N	0.22uF	6.3V	
C17	VCI-VSS	2.2uF	6.3V	+ve
C18	VDDIO-VSS	2.2uF	6.3V	+ve

POWER	**Recommended ITO Resistance**	**Voltage drop per 1mA loading**
VLCDH	10 Ω	NA
VLCDL	10 Ω	NA
VGH	40 Ω	NA
VGL	40 Ω	NA
AVDD	5 Ω	0.056V
AVDDM	5 Ω	0.145V
VCIM	5 Ω	0.067V
VCOMDC	5 Ω	NA
CX1N	5 Ω	NA
CX1P	5 Ω	NA
CX2N	5 Ω	NA
CX2P	5 Ω	NA
C11N	5 Ω	NA
C11P	5 Ω	NA
C12N	5 Ω	NA
C12P	5 Ω	NA
C21N	5 Ω	NA
C21P	5 Ω	NA
C22N	5 Ω	NA
C22P	5 Ω	NA
C1N	40 Ω	NA
C1P	40 Ω	NA
C2N	40 Ω	NA
C2P	40 Ω	NA
C3N	40 Ω	NA
C3P	40 Ω	NA

* The voltage drop per 1mA loading is estimated with the recommended ITO resistance.

17 SSD2128Z OUTPUT VOLTAGE RELATIONSHIP

Figure 17-1- LCD Driving Voltage Relationship

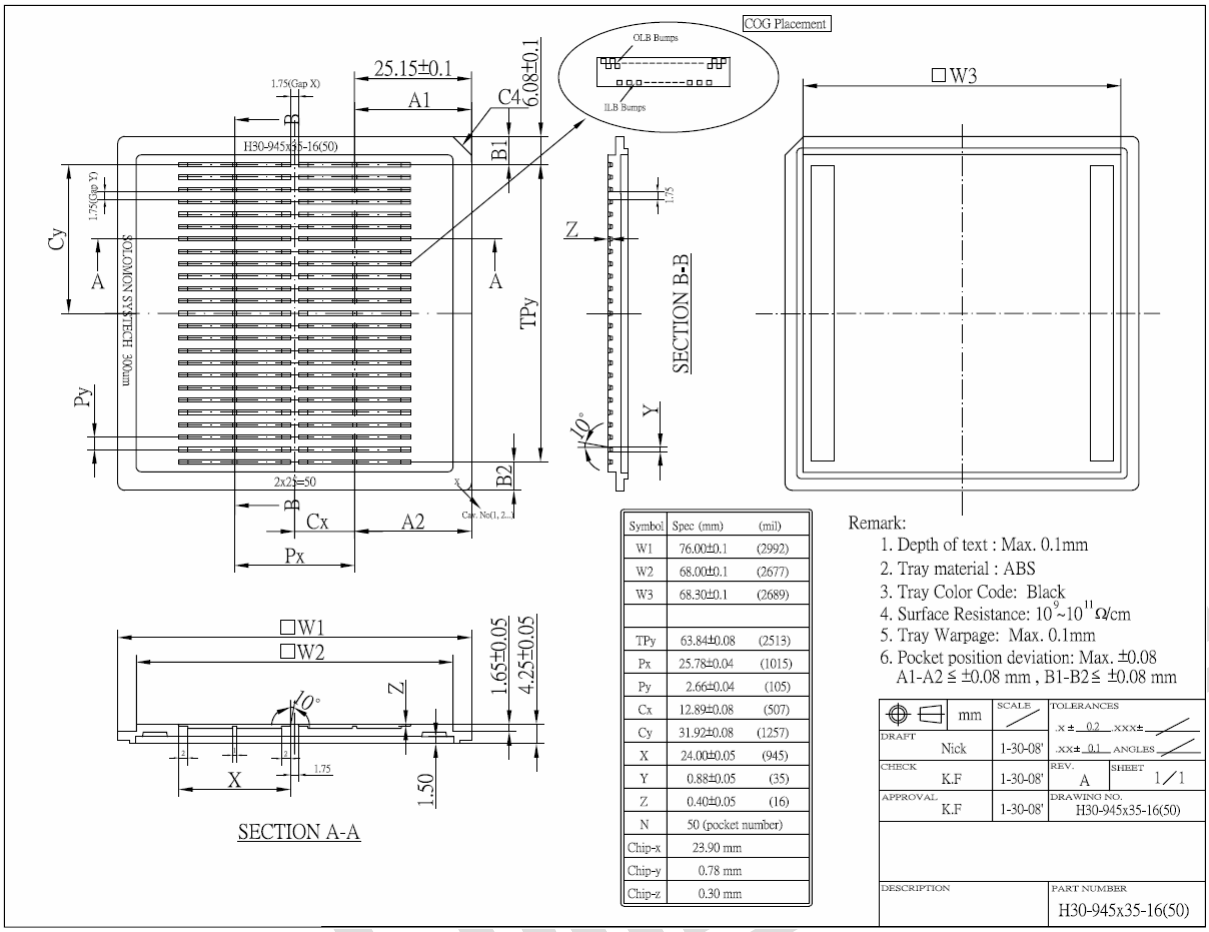


Note: The above voltages level assumed 100% efficiency of the internal booster. There has no voltage drop due to resistance from ITO trace of the panel.

18 PACKAGE INFORMATION

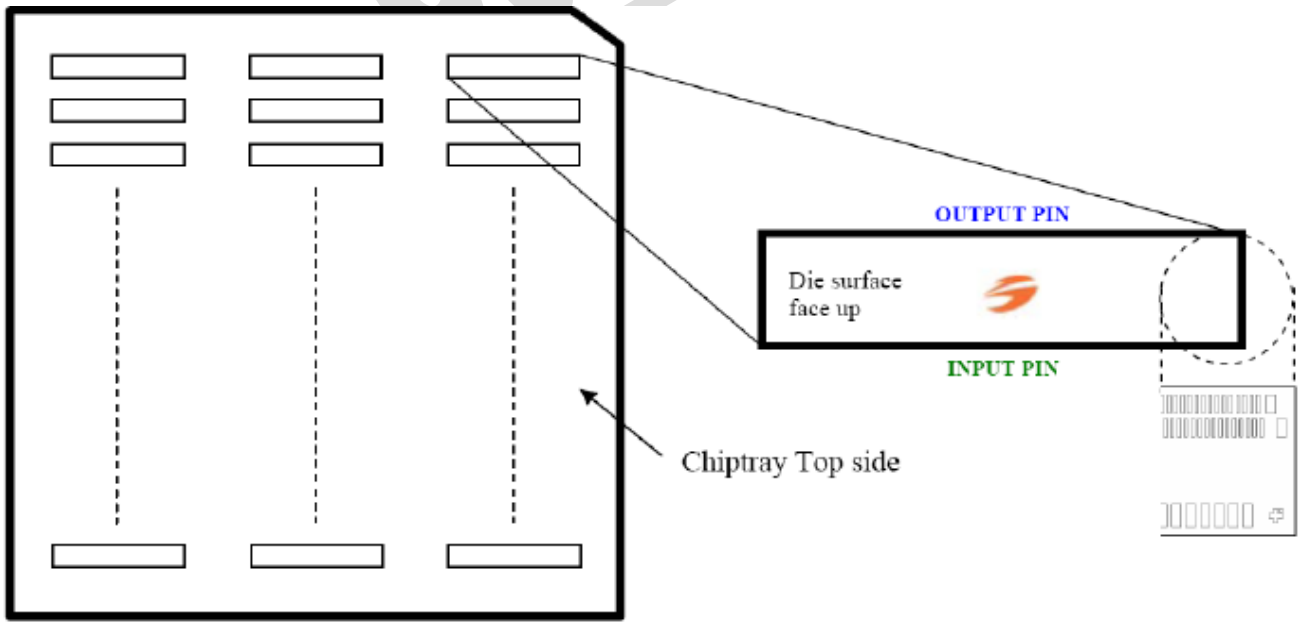
18.1 Die Tray Dimension

Figure 18-1- Die Tray Information



Symbol	Spec (mm)	(mil)
W1	76.00±0.1	(2992)
W2	68.00±0.1	(2677)
W3	68.30±0.1	(2689)
TPy	63.84±0.08	(2513)
Px	25.78±0.04	(1015)
Py	2.66±0.04	(105)
Cx	12.89±0.08	(507)
Cy	31.92±0.08	(1257)
X	24.00±0.05	(945)
Y	0.88±0.05	(35)
Z	0.40±0.05	(16)
N	50 (pocket number)	
Chip-x	23.90 mm	
Chip-y	0.78 mm	
Chip-z	0.30 mm	

18.2 IC Orientation



The product(s) listed in this datasheet comply with Directive 2002/95/EC of the European Parliament and of the council of 27 January 2004 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People's Republic of China Electronic Industry Standard SJ/T 11363-2006 "Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)". Hazardous Substances test report is available upon request.

http://www.solomon-systech.com